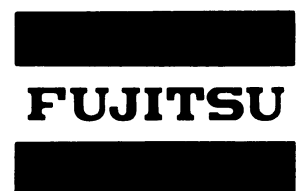


M2298 K/N

Fixed Disk Unit

Customer Engineering Manual



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Preface

This manual has been prepared for customer engineers directly involved with maintaining the M2298 fixed disk unit.

The information is provided in 10 sections:

- Section 1:** General Description
- Section 2:** Operation
- Section 3:** Installation
- Section 4:** Theory of Operation
- Section 5:** Trouble Shooting Guide
- Section 6:** Maintenance
- Section 7:** Spare Parts List
- Section 8:** IC Detail
- Section 9:** Parts and Illustration Catalog
- Section 10:** Schematics

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Section 1

General Description

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1. GENERAL DESCRIPTION

1.1 GENERAL DESCRIPTION

1.1.1 General Description

The M2298 Fixed Disk Unit (FDU) is a high performance, random access storage device with a storage capacity of 671MB.

The basic components of these units are Disk Enclosure, spindle drive motor and brake, read/write PCB, driver/receiver interface circuitry and function-related logic PCB's. The Disk Enclosure (DE) consists of Contact Start/Stop (CSS) heads and media, rotary actuator linear motor and filters all contained in a sealed cover. The M2298 series has attained performance equal to those of large storage units in a small, low price package.

The M2298 FDU contains a Modified SMD interface, thereby allowing the drives to be added to an existing disk configuration allowing substantial savings over removable media drives. By standardizing on this interface, development time for controllers and software will be substantially reduced.

The M2298 series may be mounted horizontally or vertically. They are designed to be mounted in a standard 19 inch rack or built into a system cabinet. Up to eight drives can be daisy-chained together.

1.1.2 Features

(1) High Reliability

- a) Winchester type technology contact-start-stop (CSS) heads and media are employed.
- b) The rotary actuator features low power consumption, no head loading mechanism and no head adjustment.
- c) The heads, media and rotary actuator are sealed in a closed-loop air system.
- d) Head positioning is performed by a servo track-following method utilizing servo data written on the bottom disk surface.
- e) Within the sealed disk enclosure (DE), the electric parts and assemblies are minimized.
- f) The head IC (HIC) is mounted near each data and servo head. The HIC improves the signal-to-noise ratio for increased data integrity.

(2) High Storage Capacity

The M2298 has an unformatted 671MB storage capacity which has been obtained by five platters, using the highly reliable Winchester technology.

(3) Maintainability

The M2298 requires no periodic preventive maintenance.

(4) Small Size and Light Weight

The M2298 can be installed in a 19" standard cabinet at 6-pitches. The weight of the unit is approximately 45 kg (100 lbs).

(5) Vertical Mount Capability

The FDU may be installed in a vertical direction when installed in a system.

(6) Dual Port option

Each M2298 model can be connected with two controllers when a dual port option is provided.

This option is available as a separate printed circuit board which is mounted on the PCB chassis.

1.2 SPECIFICATIONS

1.2.1 Operational Specification

Table 1.2.1 Operational Specification

Unformatted Storage Capacity	671,088,640B
Cylinder/Unit	1,024
Track/Cylinder	16
Number of Platters	5
Unformatted Track Capacity	40,960B
Single Track Positioning Time	6 ms
Average Positioning Time	27 ms
Maximum Positioning Time	55 ms
Rotational Speed	2,722 rpm
Average Latency Time	11.02 ms
Bit Density	13,000 BPI (8,600 FRPI)
Track Density	793 TPI
Transfer Rate	1,859 KB/s
Recording Code	MFM
Interface Code	RLL (2 by 7)
Start Time	40 sec nominal
Stop Time	30 sec nominal

1.2.2 Physical Specification

Table 1.2.2 Physical Specification

Characteristics	Condition	Specification
Dimension*	Height	9.8" (250mm)
	Width	16.4" (416mm)
	Depth	25.6" (650mm)
Weight	(Without options)	Approx. 100 lbs (45Kg)
Temperature	Operating	5°C to 40°C (41°F to 104°F)
	Non-operating	-40°C to 60°C (-40°F to 140°F)
	Gradient	Less than 15°C/Hr (Less than 27°F/Hr)
Relative Humidity	Operating	20% to 80%
	Non-operating	5% to 95% (without condensation)
Vibration	Operating	0.2G max (5 Hz to 50 Hz) 1.0G max (50 Hz to 500 Hz)
	Non-operating	0.4G (5Hz to 50Hz) (1.0G (50Hz to 500Hz)
Shock	Operating	Less than 2.0G (10ms)
	Non-operating	Less than 10G (10ms)
Altitude	Operating	10,000 feet
	Non-operating	40,000 feet

*Note: Same dimension with or without dual port feature.

1.2.3 Power Source Specifications

(1) AC Power Requirement

Table 1.2.3 AC Power Requirement

	AC Voltage	Frequency	Run Current	Start Current
K model	100V $\pm 10\%$	50/60Hz $+1\%$ -3%	2.5A max	9.0A max
	115V $+15\%$ -10%	60Hz $\pm 1\%$	3.0A max	10.5A max
N model	AC220V $+22V$ $-25V$	50Hz $+1\%$ -2%	2.0A max	5.0A max
	AC 100V $+32V$ $-10V$		0.3A max	
	AC240V $+24V$ -27	50Hz $+1\%$ -2%	2.0A max	5.0A max
	AC 100V $+32V$ $-10V$		0.3A max	

SEE
NOTE

SEE
NOTE

Note The M2298K is rated for AC100V/115V input, the M2298N, however, is rated for AC220V/240V (spindle motor) and for AC100V (blower).

(2) DC Power Requirement

The M2298 requires the following DC powers as described in Table 1.2.4

Table 1.2.4 DC Power Source Specifications

Voltage	Load Current	
	Basic Unit	Basic Unit with dual port option
+ 5V $\pm 5\%$	4.2A max	5.15A max
+ 12V $\pm 5\%$	0.43A max	0.43A max
-12V $\pm 5\%$	2.9A max	3.28A max
+ 24V $\pm 20\%$	3.8A max*	3.8A max*

The DC power load currents of +5V, +12 and -12V are stable, the load current of +24V, however, is fluctuated by the seek operation as shown in Figure 1.2.1.

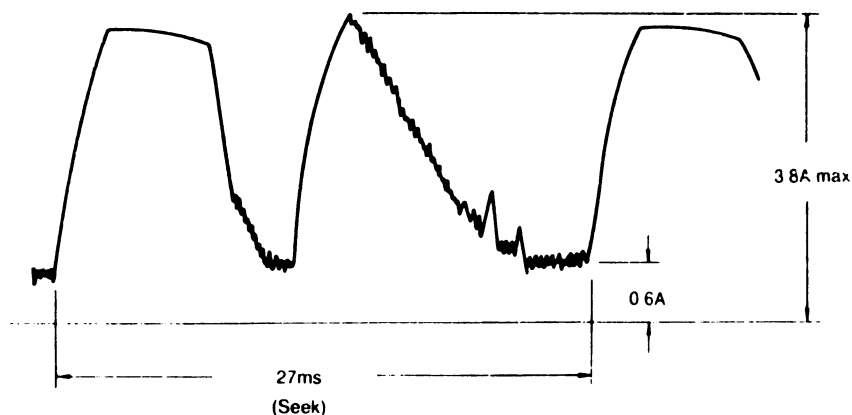
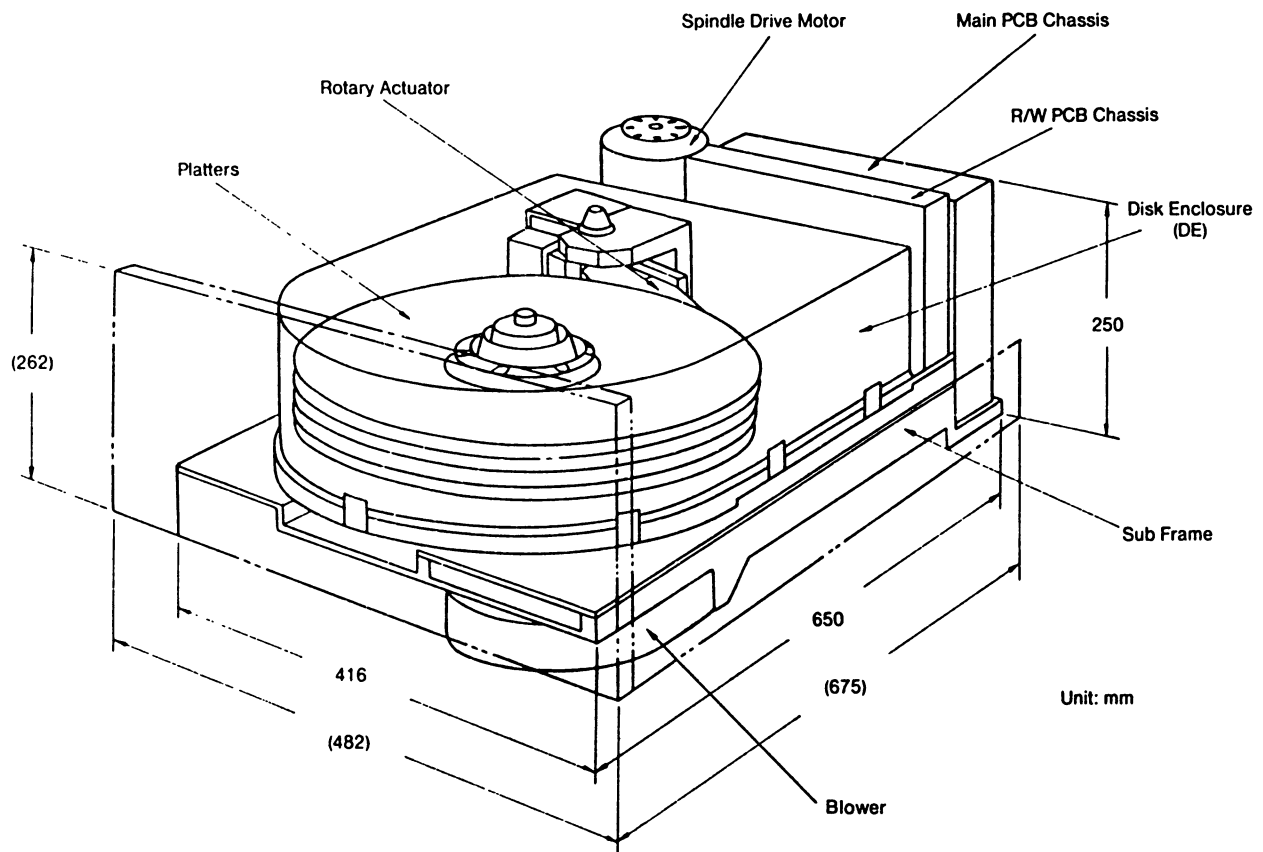


Figure 1.2.1 +24V Load Current (Worst case)

1.3 CONFIGURATION

1.3.1 Basic Configuration

The basic configuration of this unit is given in Figure 1.3.1 and its block diagram is given in Figure 1.3.2.



Note: The dimensions in parenthesis are for the FDU with a front panel and rack mount sliders.

Figure 1.3.1 Basic Configuration

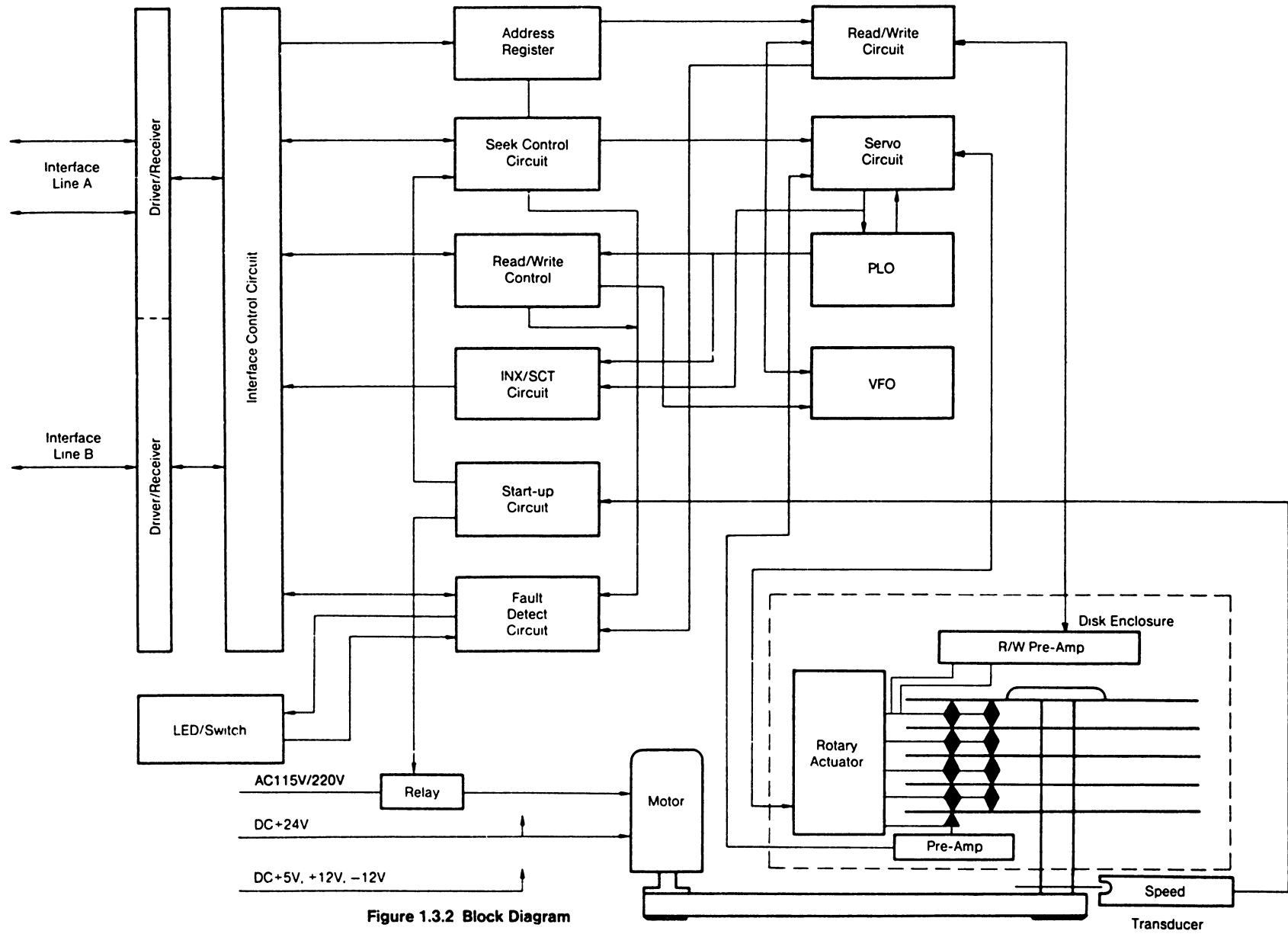



Figure 1.3.2 Block Diagram

1.3.2 Options

Table 1.3.1 Options List

Name	Specification	Remarks
Power supply	B14L-5105-0179A	Connector type 100V/115V
Power supply	B14L-5105-0180A	Connector type 208V/220V/240V
Operator Panel	B03B-4540-E352A	19" rack mount type without Slide rails.
Operator Panel and Slide rails	B03B-4540-E353A	19" rack mount type with short slide (Slide rail 24"-drawing length 29")
Operator Panel and Slide rails	B03B-4540-E354A	19" rack mount type with short slide/without Front Panel, Operator Switch and cable
Slide rail kit	B030-4540-V450A	Kit of Slide rails, Brackets, Nut Bars and Screws.
Dual Port Unit	B03B-4540-E901A	Printed circuit board and mounting plates.
Rubber shock mount	B30L-1920-0002A	Built-in type (vertical)
Cable*	B660-1065-T006A	Interface cable "A"
Cable**	B660-1065-T008A	Interface cable "B"
Terminator A	B16B-4870-0010A	A cable line terminator

Notes: * Cable length (L) can be specified from 1m to 30m in 20 inch increments.
 ** Cable length (L) can be specified from 1m to 5m in 500mm increments.

Example: B660-1065-T008A#L3R503 (for 3.5m)
 3.50 x 10³ mm

Section 2

Operation

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2. OPERATION

2.1 GENERAL DESCRIPTION

The M2298 Fixed Disk Unit can be mounted in a 19 inch rack or built into a system cabinet. An operator panel (with slide rails) is available as an option.

The GBRM Printed-Circuit-Board (PCB Chassis) of the M2298 Fixed Disk Unit is equipped with Maintenance Aid LED's, Device Check Clear switch and File Protect switch.

Powering up/down and the functions of the control panel indicators (LED) and switches will be described in this section. The optional operator panel will be described as well as the functions of the LED's and switches.

2.2 POWERING UP/DOWN

The M2298 Fixed Disk Unit is not equipped with a power ON/OFF switch. Therefore, powering up/down of the Fixed Disk Unit is usually performed by a powering up/down of the system.

However, when the disk unit is equipped with an optional power supply, powering up/down may be performed by turning the power switch ON and OFF in Local mode at the power supply or by sending Pick/Hold signals from the control unit with the power supply in Remote mode.

2.3 CONTROL AND INDICATORS

2.3.1 Operator Panel (option)

The operator panel (front panel) is optional, however, an example will be given and the functions of the LED's and switches will be described here.

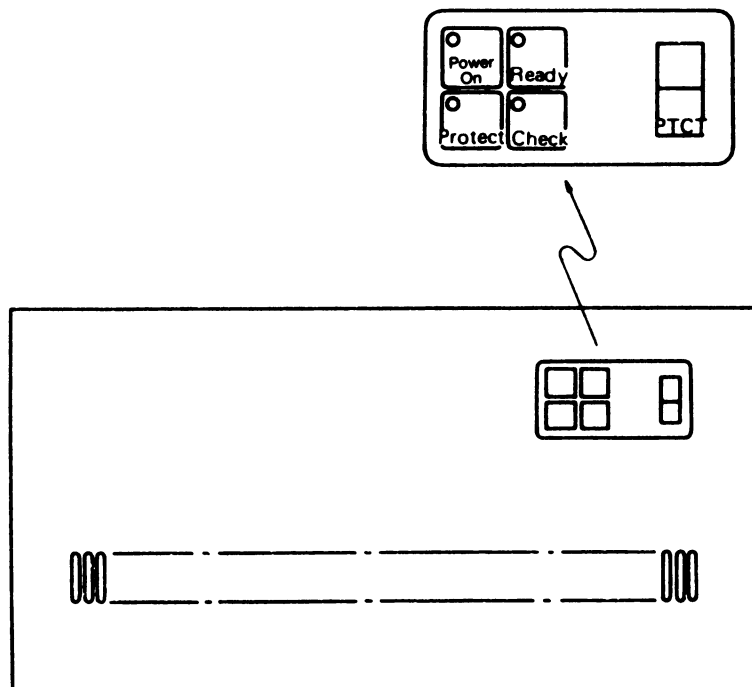


Figure 2.3.1 Operator Panel

- (1) Power On indicator: Red
This LED lights up when the power is turned on
- (2) Ready indicator: Red
This LED indicates the initial seek has been performed or indicates the termination

- of a Seek or RTZ operation.
- (3) **Check indicator: Red**
This LED indicates any fault condition.
 - (4) **Protect indicator: Red**
This LED indicates that writing is inhibited
 - (5) **PTCT switch: White**
This key inhibits the write operation.
 - (6) **Check Clear switch (check): Gray (flat key)**
This key resets a Device Check status.

2.3.2 PCB Chassis

The unit contains a PCB chassis with Maintenance Aid Display (LED's), a Device Check Clear switch and File-protect switch.

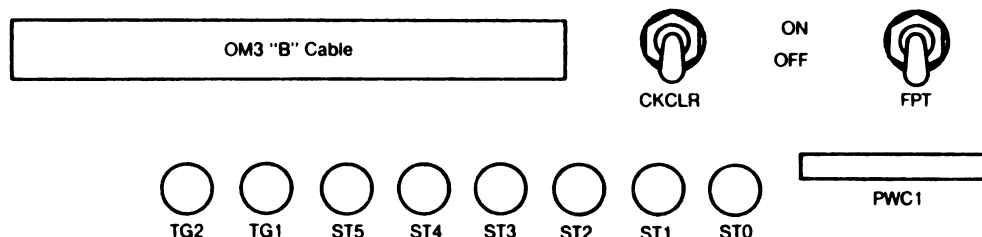


Figure 2.3.2 Maintenance Aid Display and Switches

- (1) **CKCLR (Check Clear) switch: (momentary)**
- (2) **FPT (File Protect) switch**
This switch inhibits the write operation. When an optional operator panel is installed on the unit, this switch should be in the OFF position
- (3) **TG 1, 2 (StatusTag 1, 2) LED's: Red**
Two LED's indicate four basic disk conditions in binary coded decimal, which are Not-Ready status, Device-Check status, Unit status and Seek-Check status.
- (4) **ST0 to ST5 (Status 0 to 5) LED's: Red**
Six status conditions are displayed for each Status Tag 1 and 2 combination as shown in Table 2.3.1.

Table 2.3.1 Maintenance Aid Display Conditions

TG	Tag Decode 0	Tag Decode 1	Tag Decode 2	Tag Decode 3
ST	Not Ready	Device check	Unit Status	Seek Check
0	Power Ready	Control Check 1	Unit Selected	RTZ or Seek Timeout
1	Channel Ready	Control Check 2	Fixed Sector Mode	Seek Guard Band
2	Speed OK	Read/Write Check 1	On Cylinder	Linear Mode Guard Band
3	Start 1	Read/Write Check 2	File Protected	RTZ Outer Guard Band
4	Start 2	Read/Write Check 3	Busy	Over Track Crossing Pulse
5	Initial Seek Timeout	Read/Write Check 4	Access Head Selected	Illegal Cylinder

- (1) **Not Ready Status**
 - (a) **Power Ready**
Indicates that +5V, ± 12 V DC power is up to nominal voltage.
 - (b) **Channel Ready**
Indicates the Channel Ready signal is true.

- (c) Speed OK
Indicates that the rotational speed is up to 2,177 RPM (80%).
 - (d) Start 1
Indicates that the Start Counter has output the GBENB (Guard Band Enable) signal
 - (e) Start 2
Indicates that the Start Counter has output the STARTP (Start Pulse) to initiate the initial Seek sequence
 - (f) Initial Seek Time Out
Indicates that the Initial Seek sequence was not accomplished within 704 ms after the STARTP signal.
- (2) Device Check Status
- (a) Control Check 1
Indicates that a read/write instruction was issued during Busy Status.
 - (b) Control Check 2
Indicates that Write Gate was issued during a fault condition.
 - (c) Read/Write Check 1
Indicates that Write Gate was issued during an off-track status or VCM-overheating has occurred.
 - (d) Read/Write Check 2
Indicates that write current to the data head did not flow during a write operation or that write current flows without a write gate command.
 - (e) Read/Write Check 3
Indicates that Write Gate was issued during file-protected status.
 - (f) Read/Write Check 4
Indicates that Read or Write Gate was issued during multi-head-selected condition.
- (3) Unit Status
- (a) Unit Selected
Indicates that the unit is selected.
 - (b) Fixed Sector Mode
Indicates the fixed sector mode is selected.
 - (c) On Cylinder
Indicates On Cylinder status.
 - (d) File Protected
Indicates Write-protected status.
 - (e) Busy
Indicates that the heads are in motion.
 - (f) Access head Selected
Indicates that an access head is selected. (always on)
- (4) Seek Check Status
- (a) RTZ Time Out
Indicates that an RTZ sequence was not terminated within 704 ms.
 - (b) Seek Guard Band
Indicates that a Guard Band was detected during a direct seek operation.
 - (c) Linear Mode Guard Band
Indicates that a guard band was detected during a linear mode operation.
 - (d) RTZ Outer Guard Band
Indicates that an outer guard band was detected during an RTZ operation.
 - (e) Over Track Crossing Pulse
Indicates that the head overshoot the new cylinder address during setting time (1.5ms).
 - (f) Illegal Cylinder (always off)
This status does not exist in M2298.

2.3.3 Dual Port Option

The Dual Port Option has the operational switches and LEDs as shown in Figure 2.3.3. It is operated and observed from the top side.

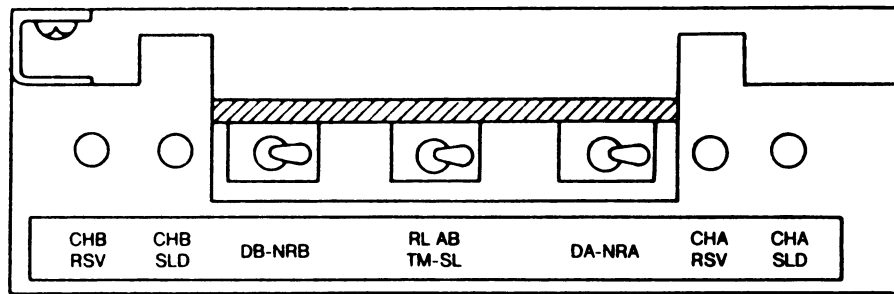


Figure 2.3.3 Switches and Indicators of Dual Port Option

- (1) CHASLD LED (green)
Indicates that this unit is selected by the channel-A controller.
- (2) CHARSV LED (orange)
Indicates that this unit is reserved by the channel-A controller.
- (3) CHBSLD LED (green)
Indicates that this unit is selected by the channel-B controller.
- (4) CHBRSV LED (orange)
Indicates that this unit is reserved by the channel-B controller.
- (5) DA-NRA switch
DB (Disable A): Selected to disconnect the unit from the channel-A controller and disable it to send and receive all interface signals.
NRA (Normal A): Selected to connect the unit to the channel-A controller and enable it to send and receive interface signals.
- (6) DB-NRB switch
DB (Disable B): Selected to disconnect the unit from the channel-B controller and disable it to send and receive all interface signals.
NRB (Normal B): Selected to connect the unit to the channel-B controller and enable it to send and receive interface signals.
- (7) RLTM-ABSL switch
RLTM Side: If this is switched to RLTM (Release Timer) side, the reserved condition is released from the unit side.
ABSL side: If this is switched to ABSL (Absolute) side, the reserved condition is released from the controller side.

2.4 OPTIONAL POWER SUPPLY UNIT

Two types of optional power supply unit are available with FDU M2298 for USA and European versions. Refer to Table 1.3.1.

The front view of the power supply unit is shown in Figure 2.4.1.

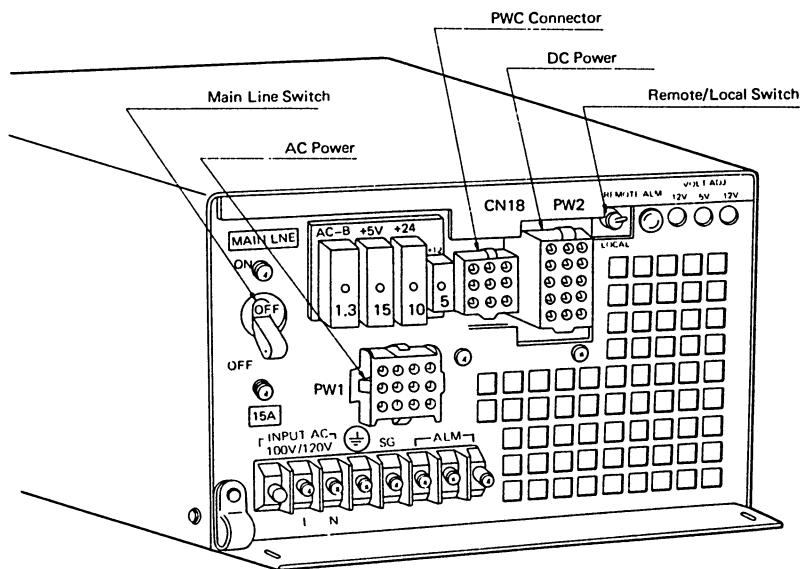
- (1) Main line switch
This switch controls application of site AC power to the power supply unit. Turning on the switch applies power to fans, spindle motor and DC power supply.
- (2) Remote/local switch
This switch controls whether the drive can be powered up from the power supply unit (Local mode), or the control unit through the FDU M2298 (Remote mode). In the Local mode, the power is applied to the disk drive when the Main Line Switch is turned on.

In the Remote mode, AC power to the fan, +5V DC and $\pm 12V$ DC are supplied to the unit by turning on the Main Line Switch and then disk drive motor power and +24V DC are supplied when Pick/Hold signals from the control unit are grounded.

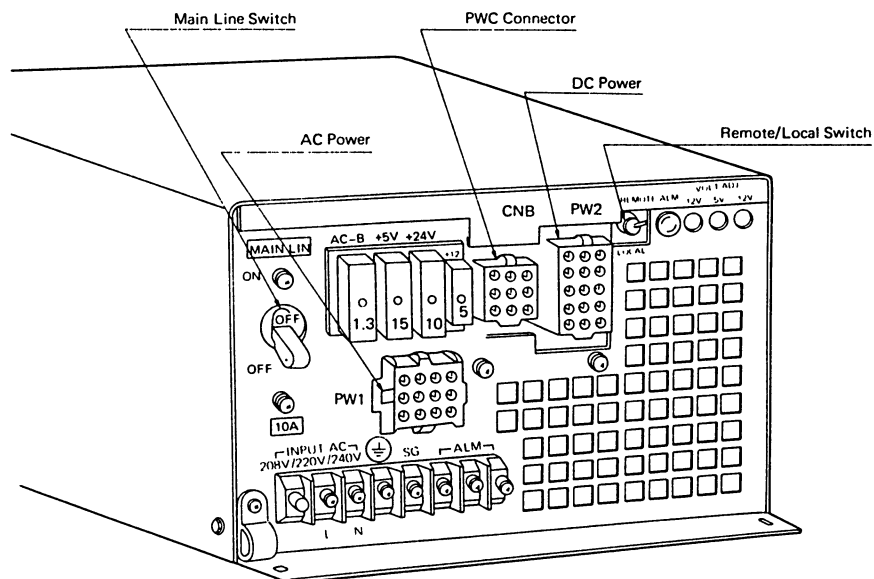
(3) Alarm lamp

Alarm lamp indicates the following power malfunction has occurred on the power supply unit or the disk unit.

- (a) +5V DC: Over-current, Over-voltage and Non-voltage
- (b) $\pm 12V$ DC: Over-current and Non-voltage
- (c) +24V DC: Fuse-blown
- (d) AC input: Over-current
- (e) Internal Fan: Thermal-switch
- (f) AC output to disk unit fan: Over-current (European version)
- (g) Disk unit fan: Thermal-switch



(1) USA Version Power Supply Unit (B14L-5105-0179A)



(2) European Version Power Supply Unit (B14L-5105-0180A)

Figure 2.4.1 Optional Power Supply Unit

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Section 3

Installation

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3. INSTALLATION

3.1 GENERAL DESCRIPTION

Unpacking, installation, and cabling of the unit when shipped separately, and work precautions when the unit is shipped as a system will be described in this section.

3.2 UNPACKING

M2298 units are shipped in a double construction carton. (An exterior view of the carton is shown in Figure 3.2.1.) Store and open the carton on a flat surface.

The outer carton is held in place with plastic securing clips which allow for reuse of the shipping container without damage due to tape or other adhesive materials. These plastic clips (4 on the top, 4 on the bottom) are removed by squeezing the two vertical pieces in the center. While squeezing, pull out from their retainers. Remove only the 4 clips in the top portion of the outer carton. Retain these with the other parts of the shipping carton for future use.

After removing the securing clips, remove the top portion of the outer carton. Next cut the foil liner (if present) and remove the tape from the inner carton. Fold back the flaps of this inner carton and remove the cushion material. Open the plastic bag and remove the drive by grasping under the subframe. DO NOT use the spindle motor, PCB chassis or disk enclosure for leverage in removing the drive.

Moreover, move the unit slowly and carefully so that it is not subjected to shock.

Caution: When the difference in the storage (or shipping) environment and the unpacking environment exceeds 20°C (36°F), the carton should be allowed to stand at the unpacking site for more than 3 hours prior to unpacking to avoid condensation.

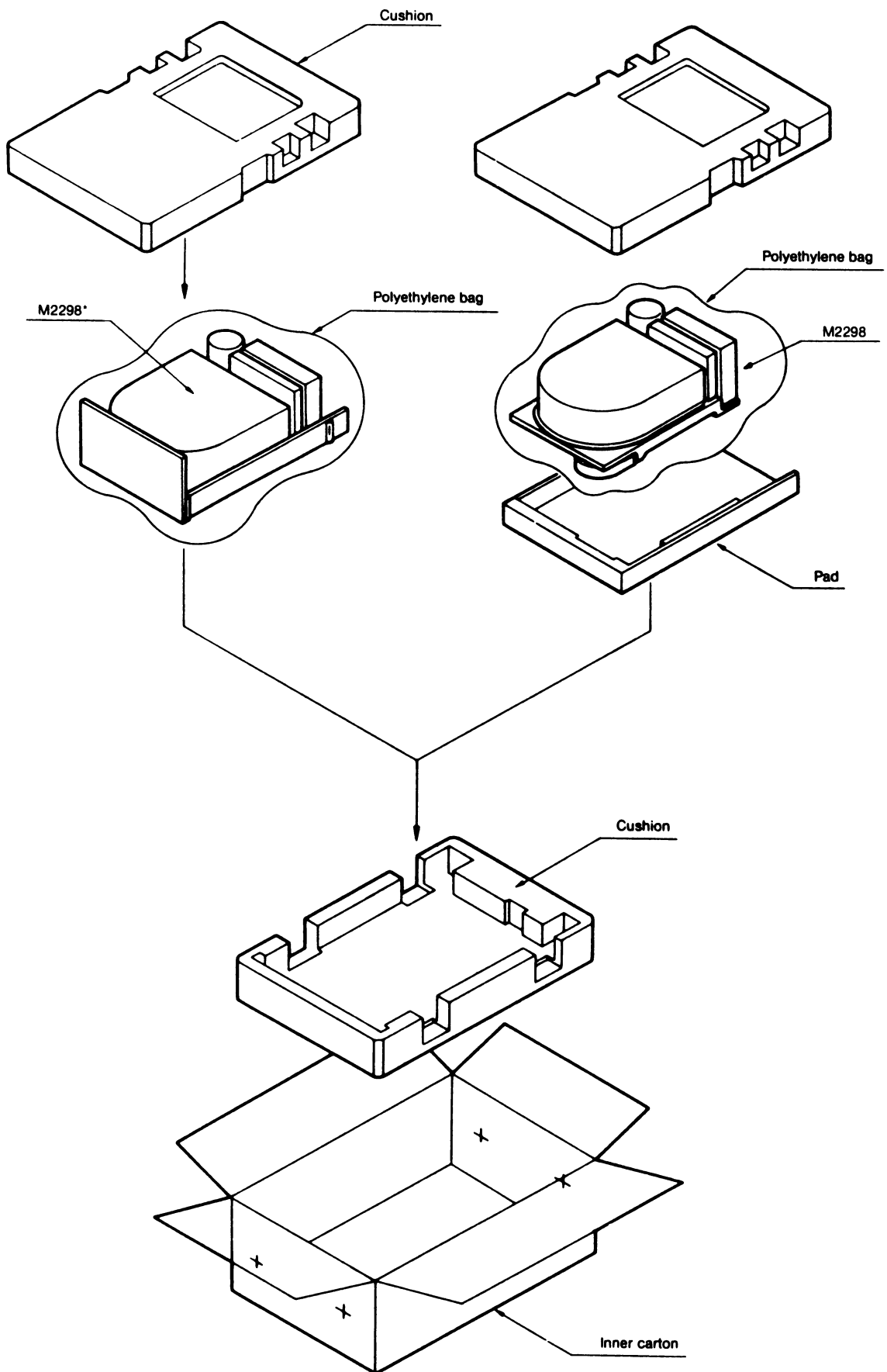


Figure 3.2.1 Construction of carton (Sheet 1 of 2)
M2298* Shown with Optional Front Panel and slides

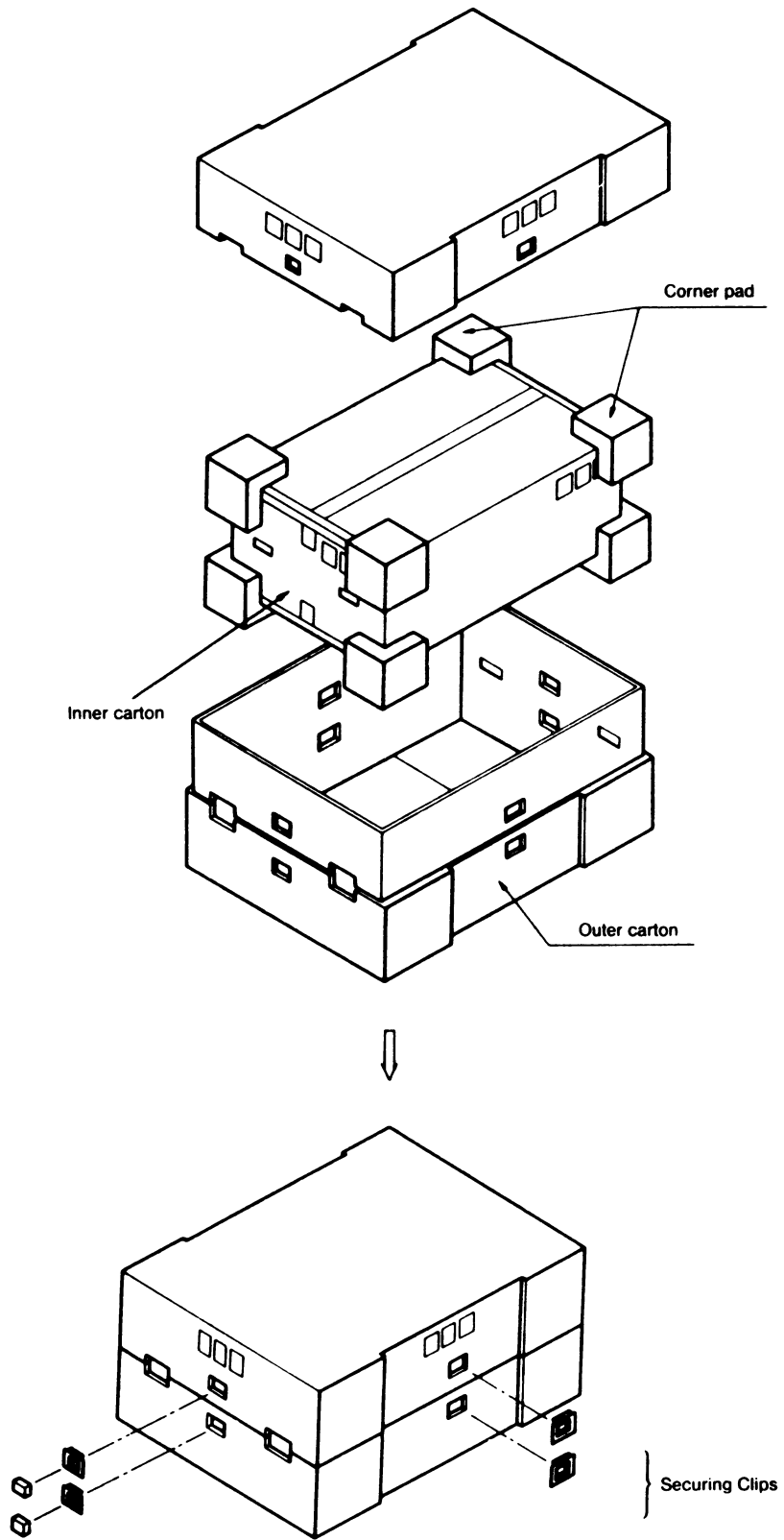


Figure 3.2.1 Construction of carton (Sheet 2 of 2)

3.3 VISUAL INSPECTION

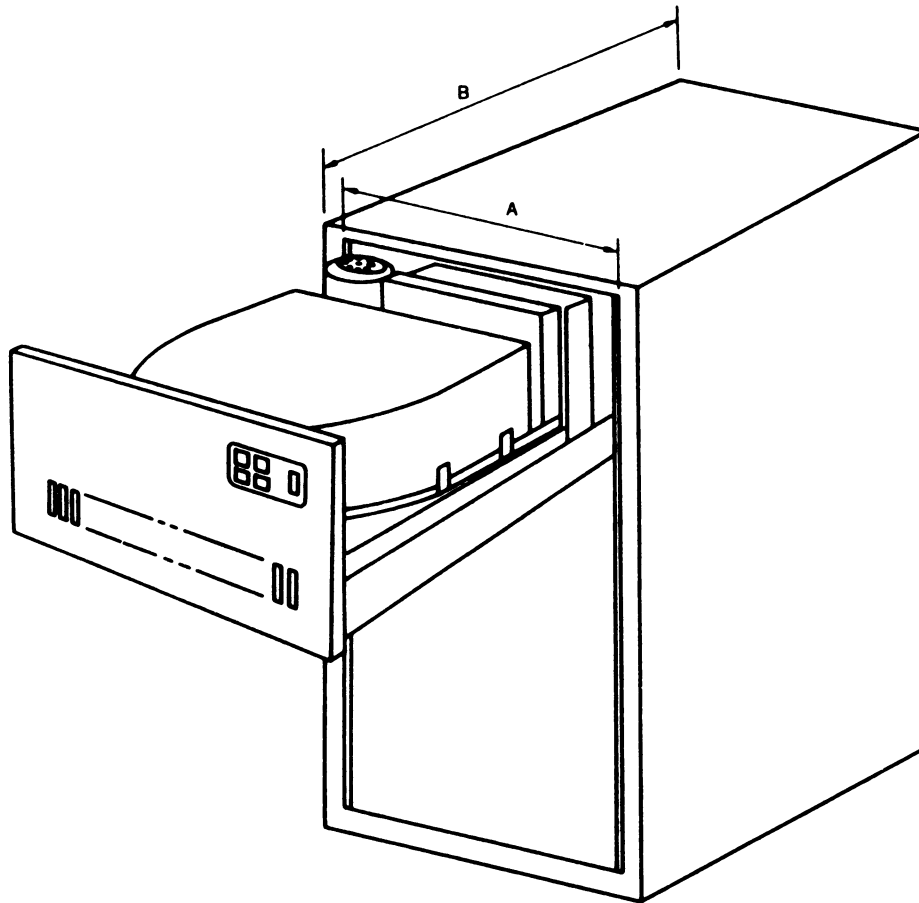
After unpacking the unit, visually inspect it as follows:

- (a) Check for scratches, rust and soiling.
- (b) Check for loose or missing parts and screws.
- (c) Check that the printed-circuit boards in the PCB Chassis are mounted in the correct positions.
- (d) Check that the specified parts, motor lock, spindle lock, and actuator lock are securely locked.

3.4 INSTALLATION

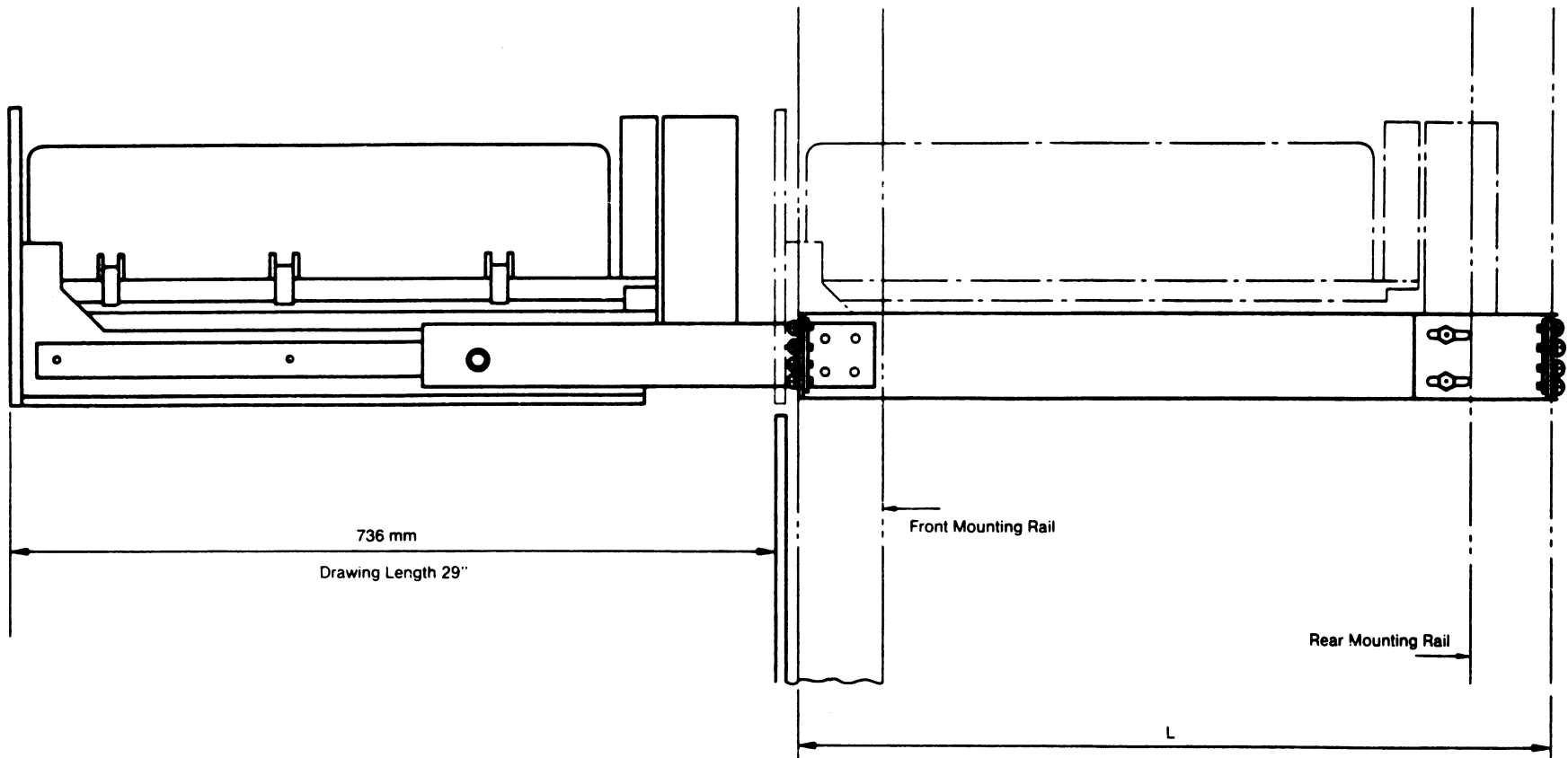
3.4.1 Mounting

The M2298 may be mounted in a 19 inch rack or built into a system cabinet. The respective mounting methods are illustrated in Figure 3.4.1 and Figure 3.4.2.



Dimension A	Standard Rack:	inside	450mm (17 72")
		outside	482.6mm (19")
Dimension B	USA Standard:		762mm (30")
	European Standard:		751mm

Figure 3.4.1 19" Rack mount Installation



L: Distance between Front and Rear Mounting rail.

Front Panel Unit

B03B-4540-E353A: 24" to 30" adjustable.

E354A: 24" to 30" adjustable.

Figure 3.4.2 19" Rack Mount Draw Out View

3.4.2 Vertical Mount Installation

The general installation procedure for a vertically-mounted unit is described below.

- (1) Turn the unit over and place it on suitable cushioning material (the cushioning material on top of the inner carton of the shipping carton is provided for this purpose (see Figure 3.2.1) so that the plastic cover of the disk enclosure is at the bottom. At this time, hold the unit by the aluminum casting so that excessive force is not applied to the motor and gate section or disk enclosure section. Be especially careful that shock and horizontal force are not applied to the unit when placing it onto the cushioning material with the plastic cover of the disk enclosure at the bottom. Refer to Figure 3.4.3.
- (2) At this time, install the mounting fixture to the unit.
(Tighten all the mounting screws on the unit from the top.)
- (3) Mount the unit in the cabinet. Refer to Figure 3.4.4.
- (4) After mounting, release the spindle lock (see paragraph 3.4.3), actuator lock (see paragraph 3.4.4) and motor lock (see paragraph 3.4.5). These locks must always be locked when moving the equipment. See paragraph 3.6. (This also applies to the 19 inch rack mount installation).
- (5) Adjust spindle belt tension per Section 6.5.3 (c) for vertical mounting.

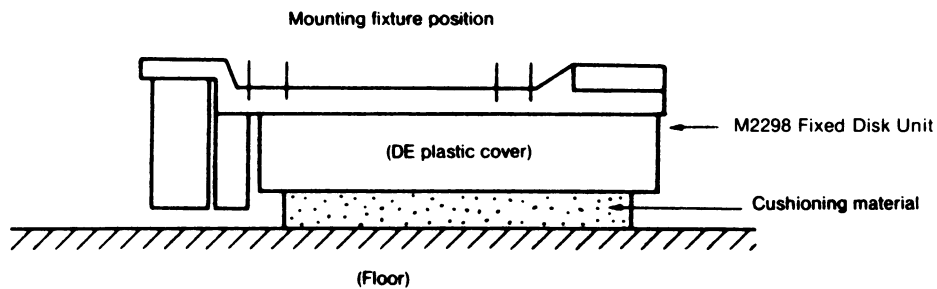
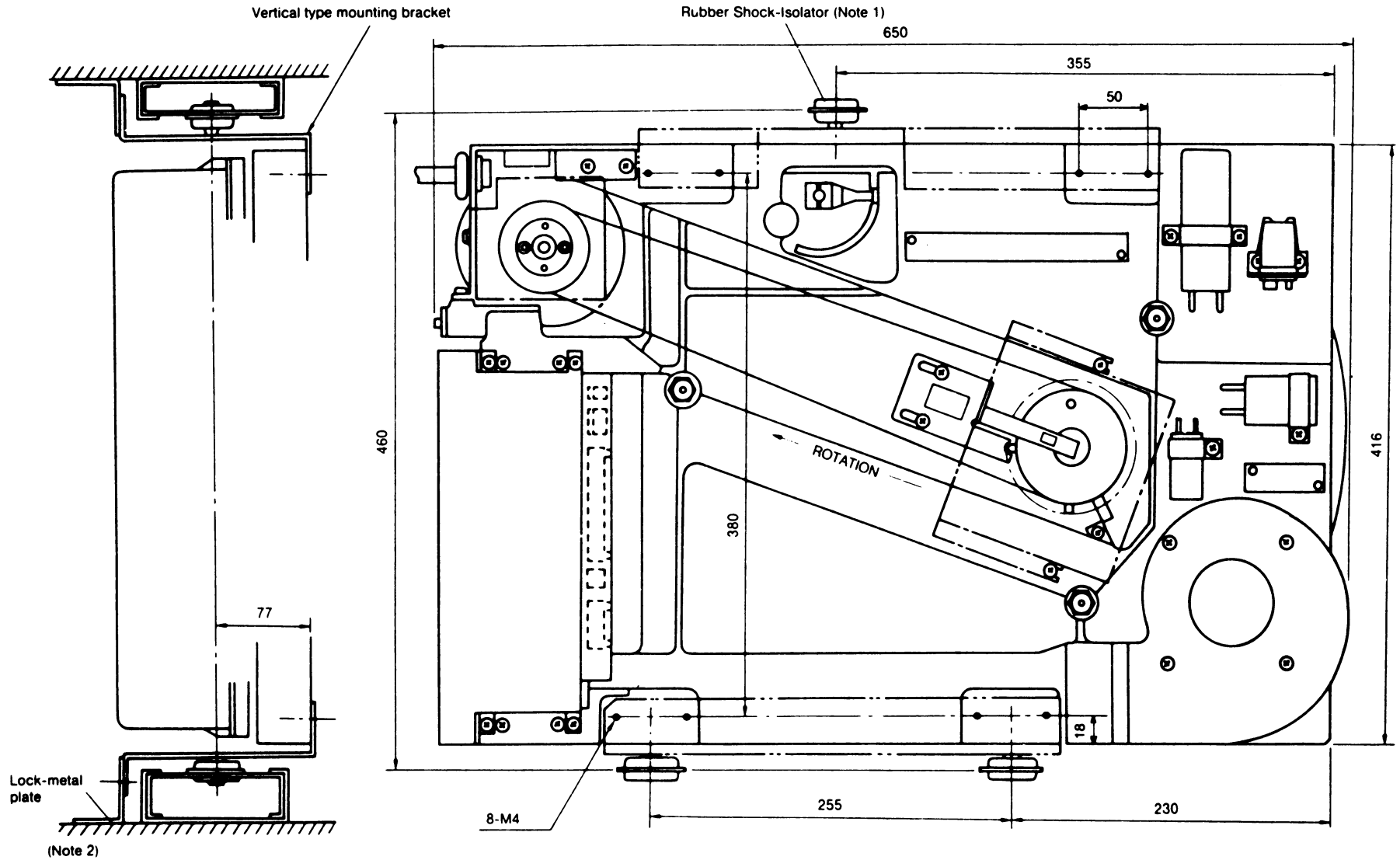


Figure 3.4.3 Mounting Fixture



Note 1: Three Rubber-Shock-Isolators are optional.

Note 2: The Unit must be locked only when it is to be shipped.

(Unit: mm)

Figure 3.4.4 An Example of Vertical Mount Installation

3.4.3 Unlocking Spindle

The spindle is locked with a spindle lock so that it cannot rotate during shipment. The spindle lock is located at the bottom of the spindle, and locks the spindle pulley. When installing the unit, the spindle lock must be released by loosening screws A (two screws) shown in Figure 3.4.5.

After unlocking, the spindle ground brush must be adjusted (see paragraph 6.5.5).

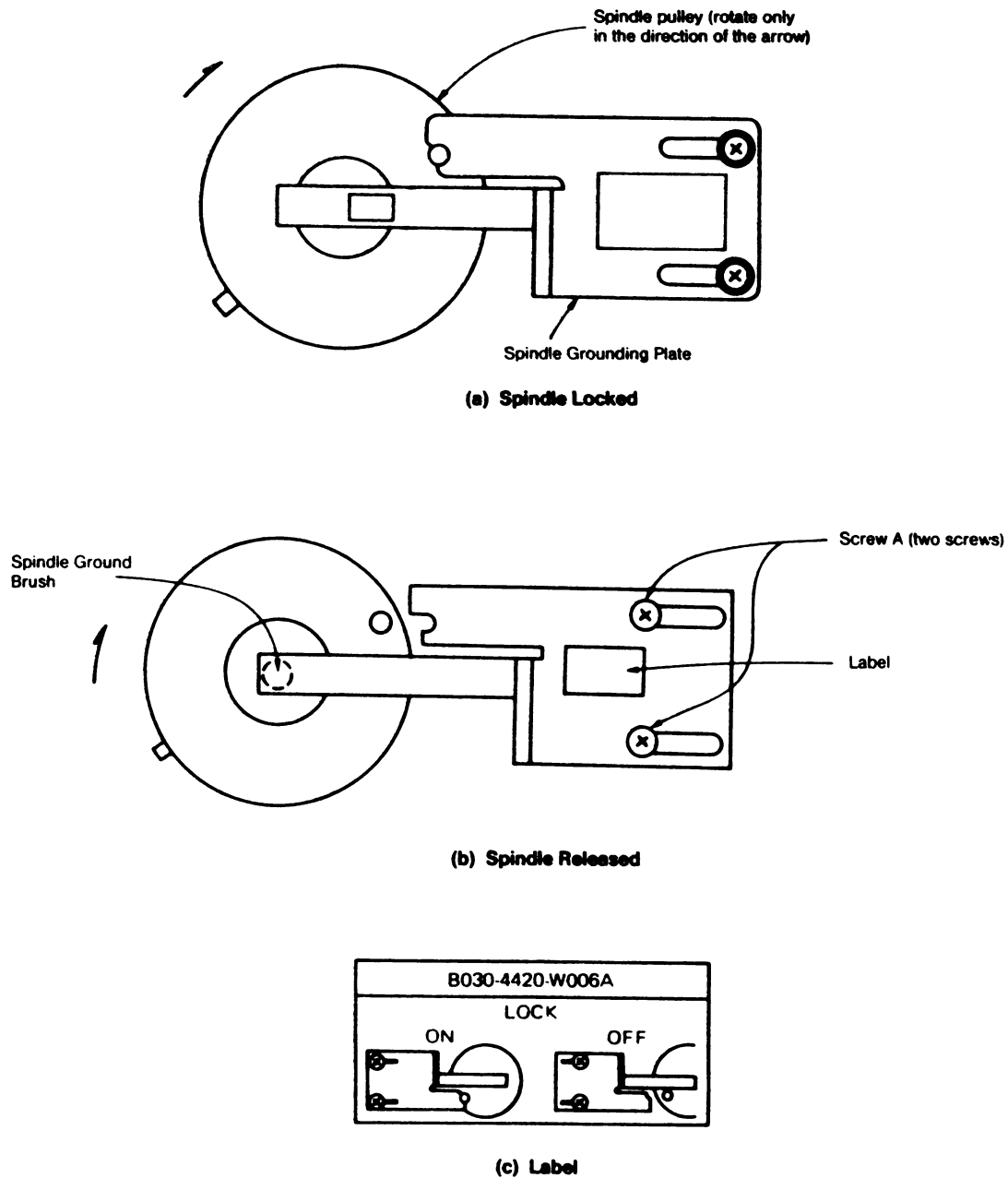
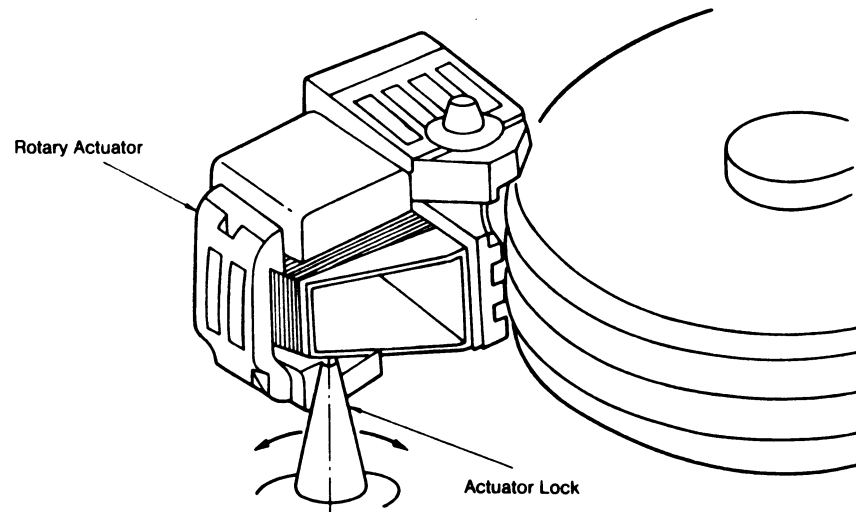


Figure 3.4.5 Releasing Spindle Lock

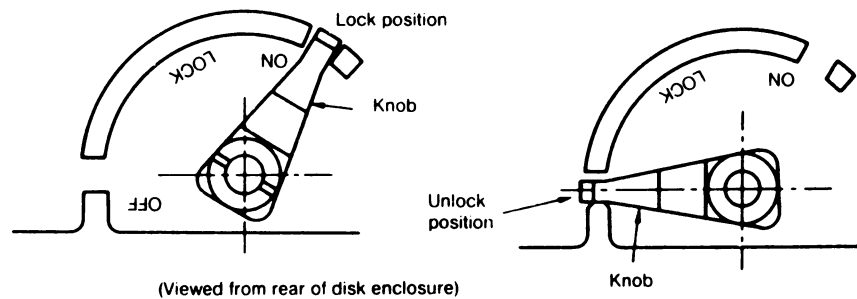
3.4.4 Unlocking the Actuator

If the actuator rotates when the disk is stopped, the heads and disks may be damaged. Therefore, the actuator is locked during shipment.

After installing the unit, the actuator must be unlocked by rotating the stopper. The stopper can be unlocked by turning the knob at the bottom rear of the disk enclosure through the hole in the sub-frame.



(a) Stopper positions



(b) Actuator locked

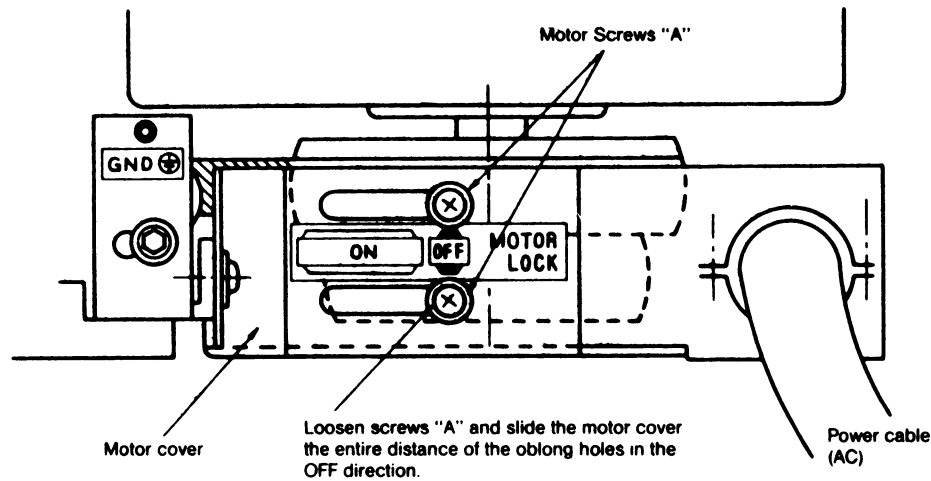
(c) Actuator unlocked

Figure 3.4.6 Actuator Lock

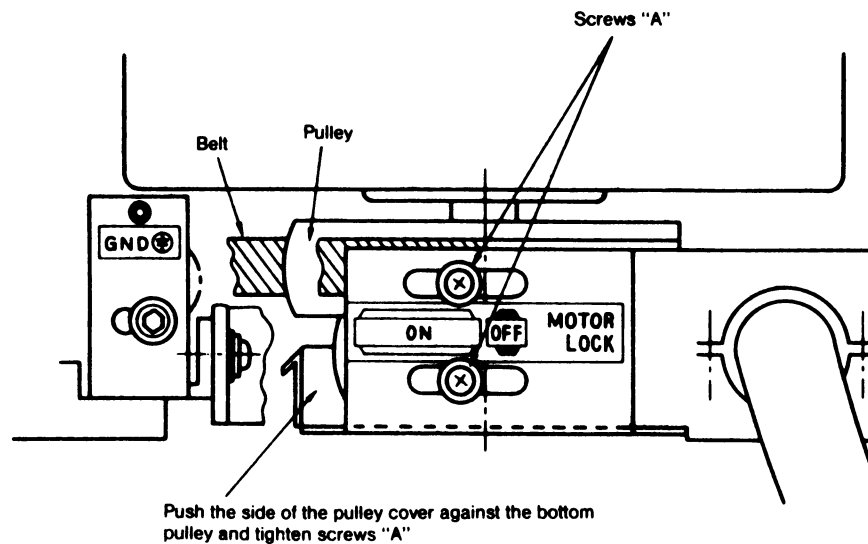
3.4.5 Unlocking the Motor

The motor must be locked during shipment to prevent unhooking the belt by vibration of the spindle. The motor is locked by pushing the side cover of the motor pulley (cover covering the motor pulley section) against the motor pulley. The motor is unlocked by loosening the two screws "A" holding the motor cover to the rear of the unit and sliding the pulley cover fully to the Left (unlock) position. Then secure screws "A". (Figure 3.4.7)

(a) Motor unlocked



(b) Motor locked



Note: Lock-on position is different according to power line frequency.

Figure 3.4.7 Motor lock and release

3.4.6 50Hz/60Hz Exchange

Check if the power line frequency is 50Hz or 60Hz, and confirm that the correct motor pulley is being used. The correct pulley diameter and belt position (50Hz/60Hz) are given on a label attached to the motor pulley cover (bottom side). The large diameter pulley is for 50Hz and the small diameter pulley is for 60Hz. (The label is illustrated in Figure 3.4.8.) When the power line frequency and the pulley mounted in the unit are different, the motor pulley must be changed and the belt tension adjusted as will be described in paragraph 6.5.3.

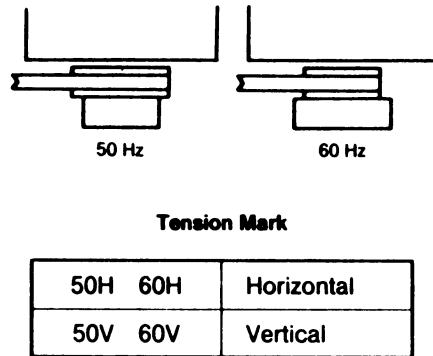


Figure 3.4.8 Frequency and pulley position (label)

3.4.7 Dual Port Installation

The Dual Port option consists of the following components:

Dual port option: B03B-4540-E901A

- Crosscall B (XCBM) PCB assembly:
B16B-7990-0020A
- 50-pin cable (between KGEM and XCBM):
B660-1065-T037A#L05R01 (50 mm)
- 10-pin cable (between CN32 on XCBM and CN21 on QBRM):
B660-1060-T089A#L16R01 (160 mm)
- 26-pin cable (between CN34 on XCBM and OM3 on GBRM):
B660-1065-T061A#L07R01 (70 mm)
- Cover:
B030-4540-X901A
- Mounting plate:
B030-4540-X903A
B030-4540-X904A
- Others: Screws and label

When shipping the Dual Port option, the option is assembled with a PCB assembly, a cover and mounting plates. Three cables and four screws (M3 binding screw) are supplied as accessories.

The mounting procedure of Dual Port option is as follows:

- (1) Mount the four screws (M3 binding screw) on the PCB chassis.
- (2) Slide the option until the screws fit to the elongation notches on the mounting plates.
- (3) Tighten these screws to fix the option.
Refer to Figure 3.4.9 for the above-mentioned procedures.
- (4) 50-pin cable
 - 1) Remove the top cover from the PCB chassis.
 - 2) Insert the 50-pin cable (B660-1065-T037A#L05R01: 50mm) in CN30 on KGEM.
 - 3) Reposition the top cover, and fix it with screws.
 - 4) Insert the opposite connector in CN31 on XCBM.
- (5) 26-pin cable
 - 1) Insert the 26-pin cable (B660-1065-T061A#L07R01: 70mm) in CN34 on XCBM.
 - 2) Insert the opposite connector in OM3 on mother board GBRM.
- (6) 10-pin cable
 - 1) Insert the 10-pin cable (B660-1060-T089A#L16R01: 160mm) in CN32 on XCBM.
 - 2) Insert the opposite connector in CN21 on the mother board.
When doing this, see that the cable passes behind the FPT and CKCLR switches on the mother board.
Refer to Figure 3.4.10 for the above-mentioned cabling procedures.

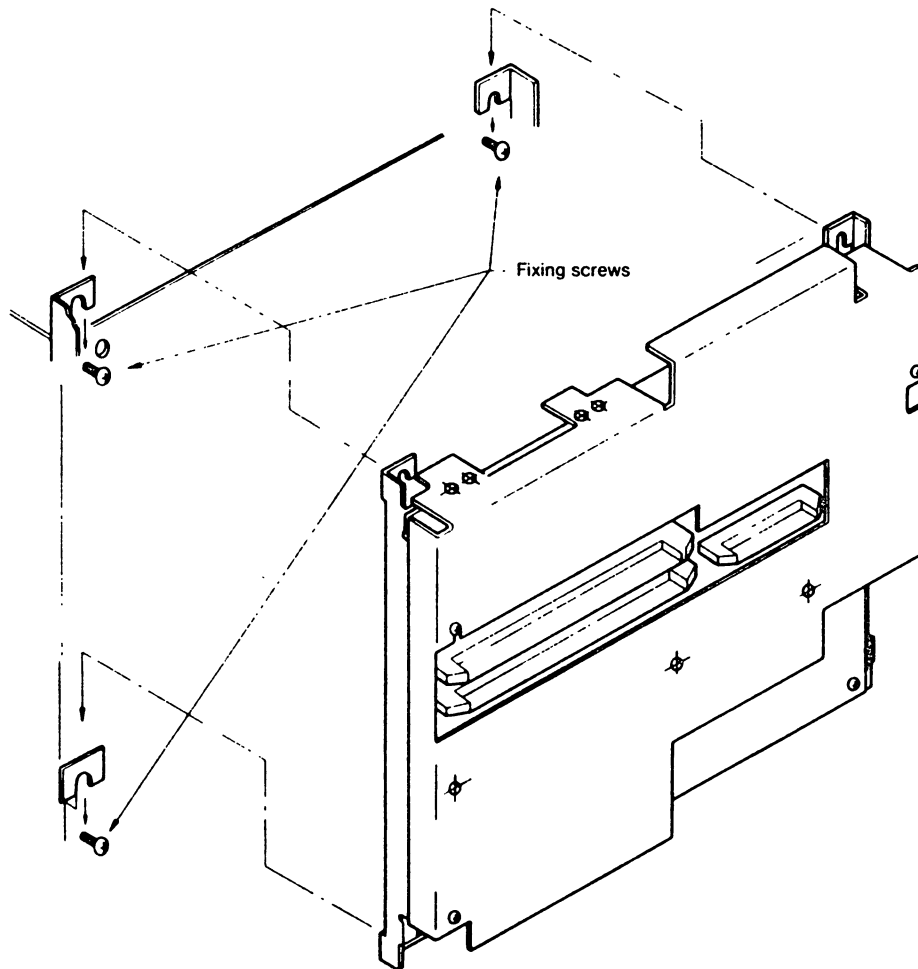


Figure 3.4.9 Fixing the Dual Port option

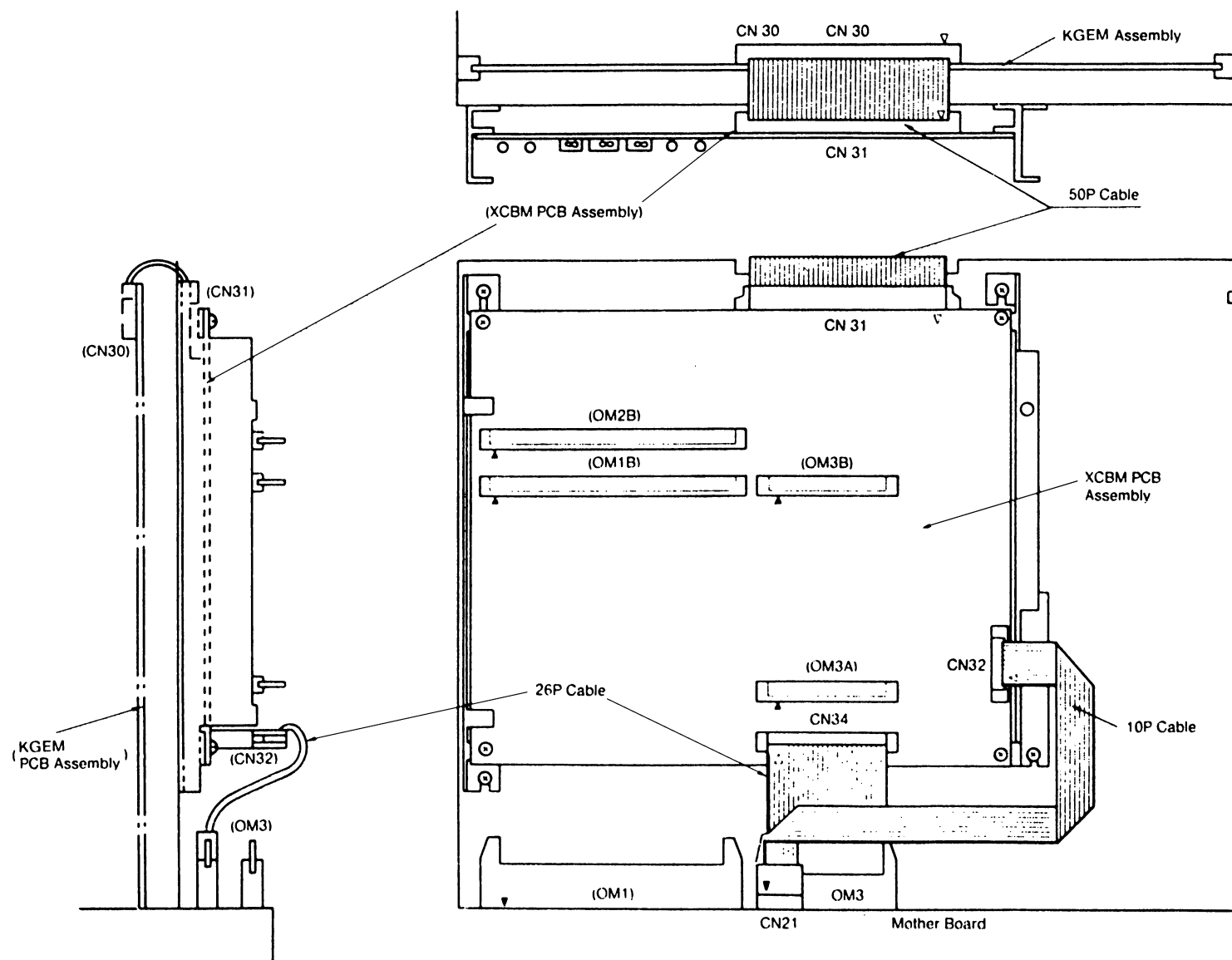


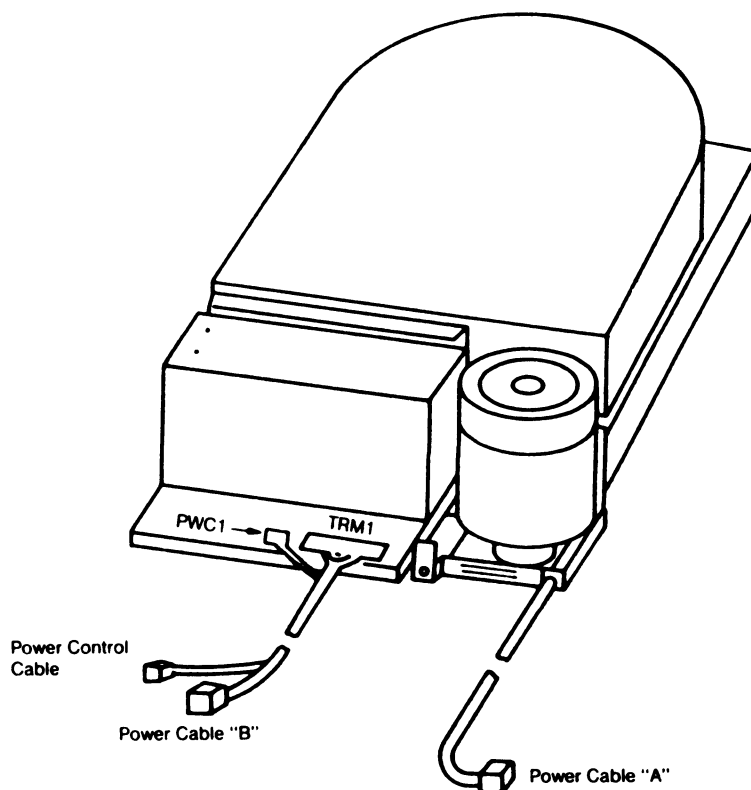
Figure 3.4.10 Dual Port Internal Cabling

3.5 CABLING

3.5.1 Power Cable

The power cable consists of an AC power supply "A" cable and a DC power supply "B" cable. The "A" cable supplies power to drive the spindle motor and brake, and blower motor, and the "B" cable supplies DC operating power to the logic and analog circuits.

The power cable connections are given in Figure 3.5.1 and Table 3.5.1.



(This figure is referred to when connectors are used.)

Figure 3.5.1 Power Cables

Table 3.5.1 Power Cables

Cable	Pin Assignment	Wire Mark	Voltage	AWG No.	Wire Color	Connector
"A"	1	AC-A1	AC Input A1	AWG 18	White/Orange	Plug (AMP) 1-480708-0
	3	AC-A2	AC Input A2	AWG 18	White	
	4	*AC-B1	AC Input B1	AWG 18	White/Orange	
	6	*AC-B2	AC Input B2	AWG 18	White	
	5	FG	FG	AWG 18	Green	Contact (AMP) 350550-3
	7	ALM	ALARM	AWG 20	Grey	
	9	ALM	ALARM	AWG 20	Yellow	
	10	+24V	DC +24V	AWG 16	Red	
	12	0V	0V	AWG 16	Black	
"B"	5	+5V	DC +5V	AWG 14	Red	Plug (AMP) 1-480710-0
	6	0V	0V	AWG 14	Black	
	1	+12V	DC +12V	AWG 18	Red	
	2	0V	0V	AWG 16	Black	Contact (AMP) 350550-7 (1, 2, 7, 8P)
	7	—12V	DC—12V	AWG 18	Blue	
	8	0V	0V	AWG 16	Black	

*Note: When AC input is 220V/240V, AC-B input should be nominal AC 100V.

Table 3.5.2 Power Control Connector (CN1)

Pin Assignment	Signal	Wire Color	AWG No.	Connector
1	*RDY1	Yellow	AWG 20	Plug (AMP) 1-480706-0
2	*RDY2	Yellow	AWG 20	
3	*RDY3	Yellow	AWG 20	
4	Pick In	Black	AWG 20	
5	Hold	Black	AWG 20	Contact (AMP) 350550-7
6	Pick Out	Black	AWG 20	
7	0V	Yellow	AWG 20	
8	0V	Yellow	AWG 20	

The power cable "A" and "B" are furnished with the unit.
"A" cable is for AC power and "B" cable is for DC power with the Power Control connector.

Table 3.5.3 Power Cable List

Description	Specification
"A" Power Cable with connector	B660-1055-T017A
"B" Power Cable with connector	B660-1055-T018A

The cable length shall be specified in 1, 2, 3 and 4m lengths.

Example: B660-1055-T017A#L3R003

$$3.00 \times 10^3 \text{mm} = 3.0\text{m}$$

3.5.2 Connecting with Optional Power Supply

3.5.2.1 AC Input Select

The optional power supply unit for USA version (B14L-5015-0179A) can be operated under AC 100V or AC 115V, and the power supply unit for European version (B14L-5105-0180A) can be operated under AC 220V or AC 240V. Therefore, before connecting with the power supply, they must be selected by the transformer taps inside the unit according to site AC input.

The selected AC voltage before shipping is labelled on the unit.

AC voltage select procedure is as follows:

- (1) Remove the cover by loosening screws as shown in Figure 3.5.2 (1). After removing of the cover, the terminal is visible as shown in Figure 3.5.2 (2)/(3).
- (2) AC voltages are indicated nearby the terminal.
The wire from N.F.B. must be connected to the terminal according to site AC input.
- (3) Fix the cover by fastening the screws.

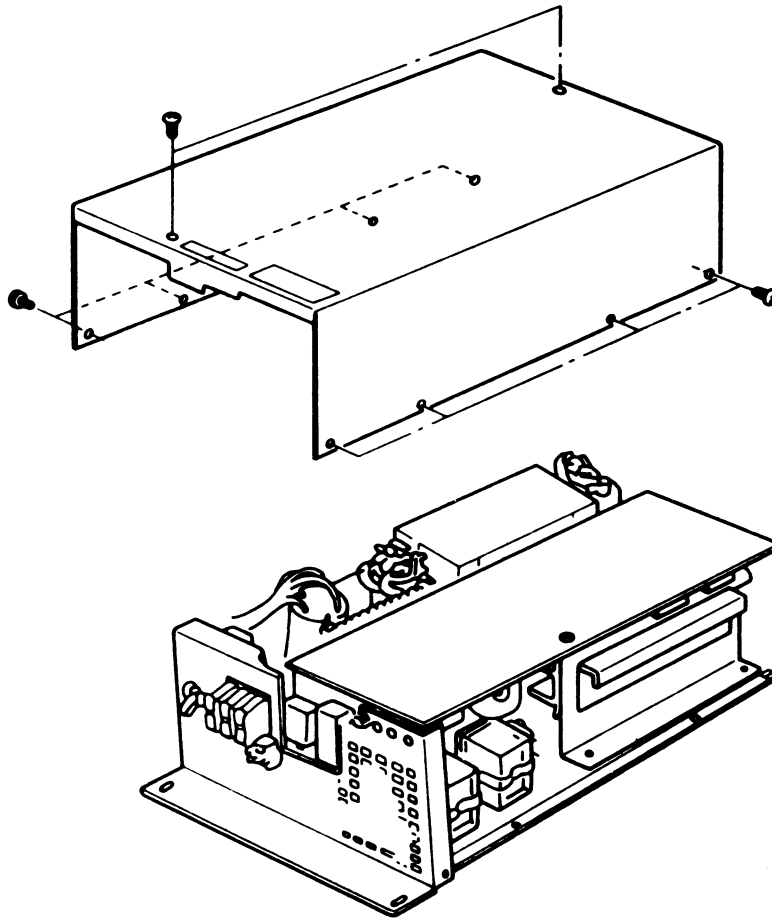


Figure 3.5.2 AC Input Select (Sheet 1 of 3)
(Removal of the cover)

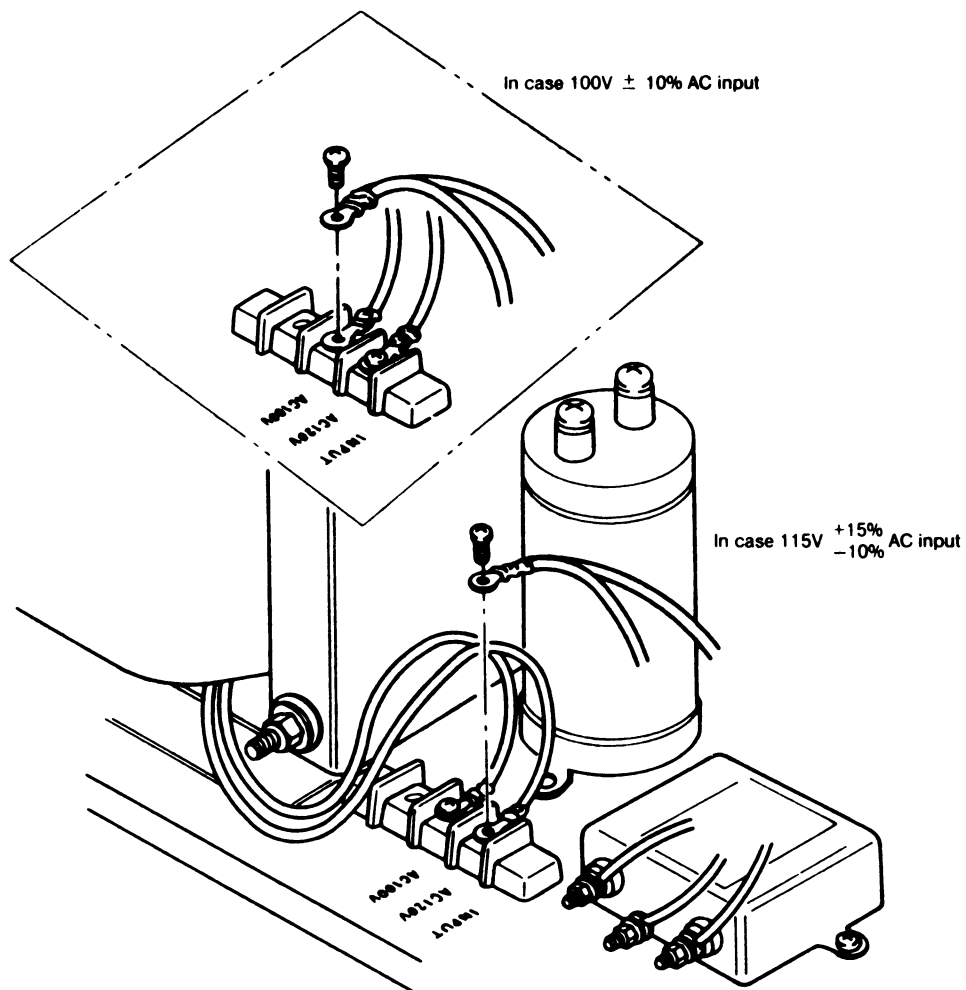


Figure 3.5.2 AC Input Select (Sheet 2 of 3)
USA Version

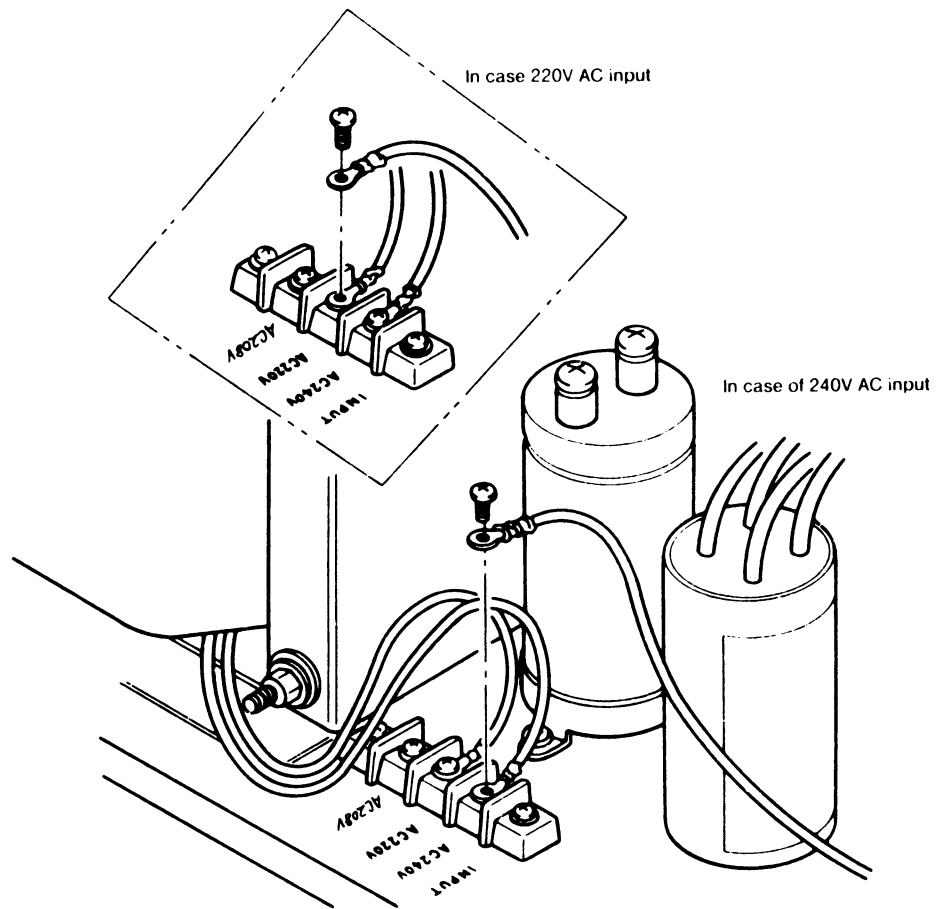


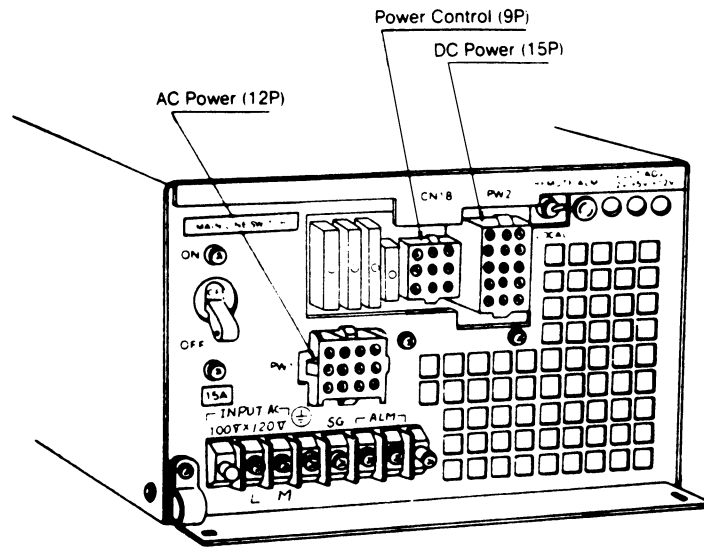
Figure 3.5.2 AC Input Select (Sheet 3 of 3)
European Version

3.5.2.2 Power Cable Connection

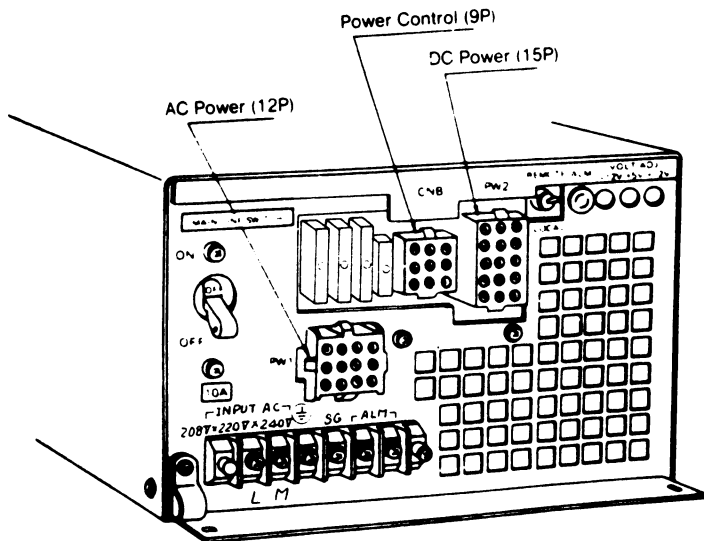
The FDU M2298 provides three power cables, AC cable, DC cable and Power Control cable. AC power connector (12P) is connected to PW1, DC power connector (15P) to PW2, and Power Control connector (9P) to CN18 respectively as shown in Figure 3.5.3.

3.5.2.3 DC Voltage Adjustment

After connecting the power cables between FDU M2298 and a power supply unit, adjust the each DC voltage on TRM2 terminal to +5V and $\pm 12V$ by specified potentiometers.



(1) USA Version Power Supply Unit



(2) European Version Power Supply Unit

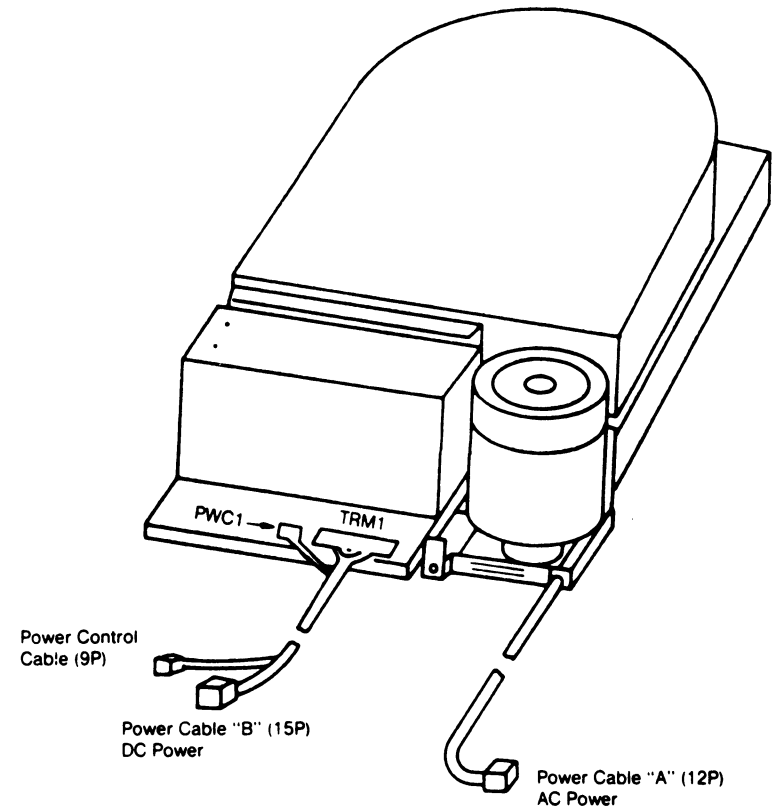


Figure 3.5.3 Power Cable Connection

3.5.3 Interface Cabling

Interface cables include cable "A" (60P) for control signals and cable "B" (26P) for data signals.

Cables are connected to the system in the star connection mode or the daisy-chain mode as shown in Figures 3.5.4, and 3.5.5.

For the star connection mode, the line termination for cable "A" is necessary for every unit.

For the daisy-chain mode only the last unit requires a Line Terminator.

The grounding wire of the Line Terminator must be connected to a signal ground TRM1-2.

In the case of dual-port operation, the interface cables from the channel-A and B controllers are also connected to the system in the star connection mode or in the daisy-chain mode as shown in Figures 3.5.6 and 3.5.7.

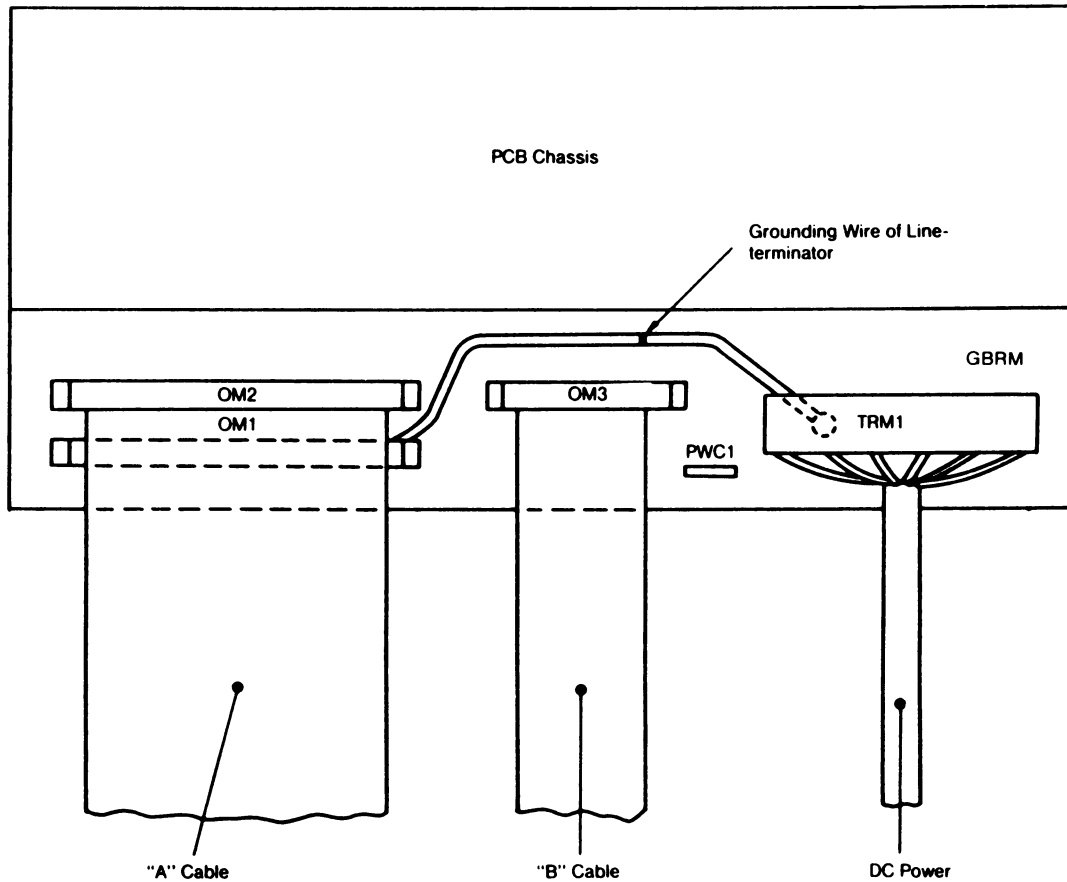


Figure 3.5.4 Interface Cabling (Single Port)

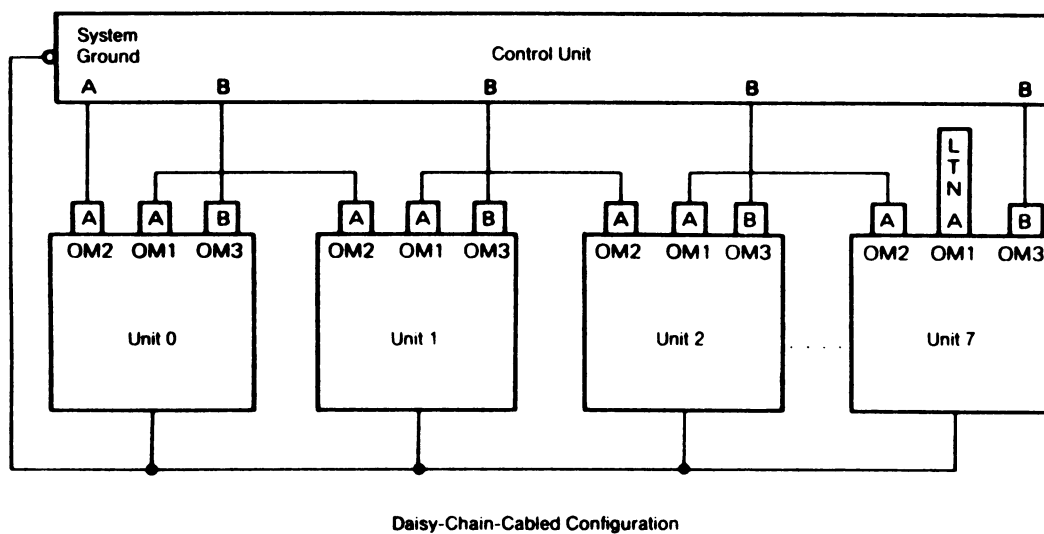
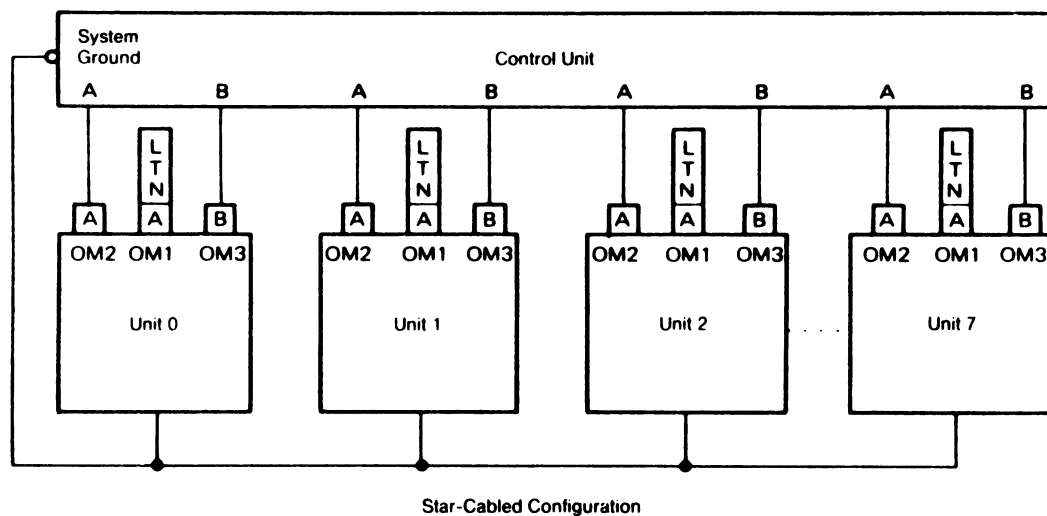


Figure 3.5.5 System Interface Cabling (Single Port)

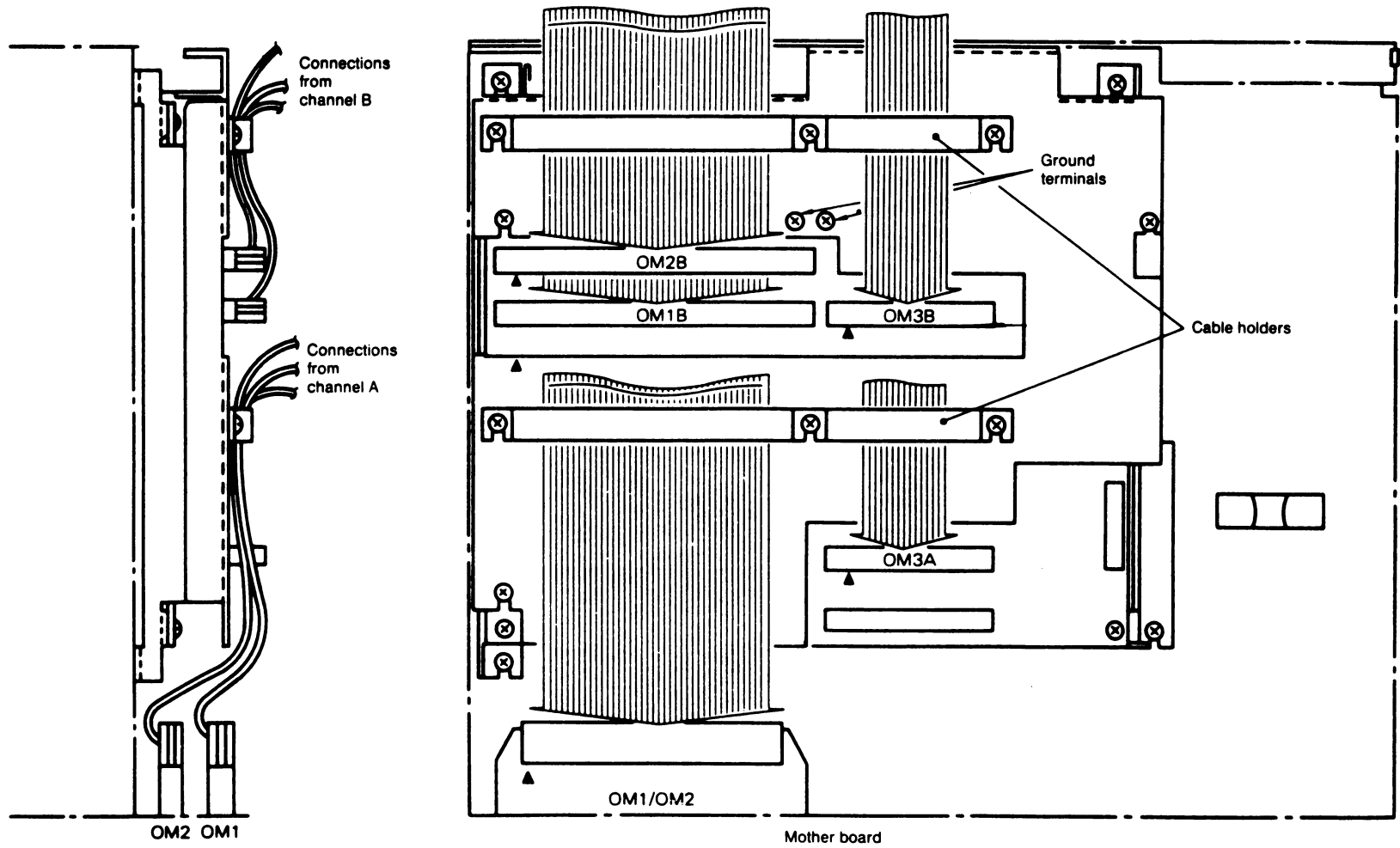
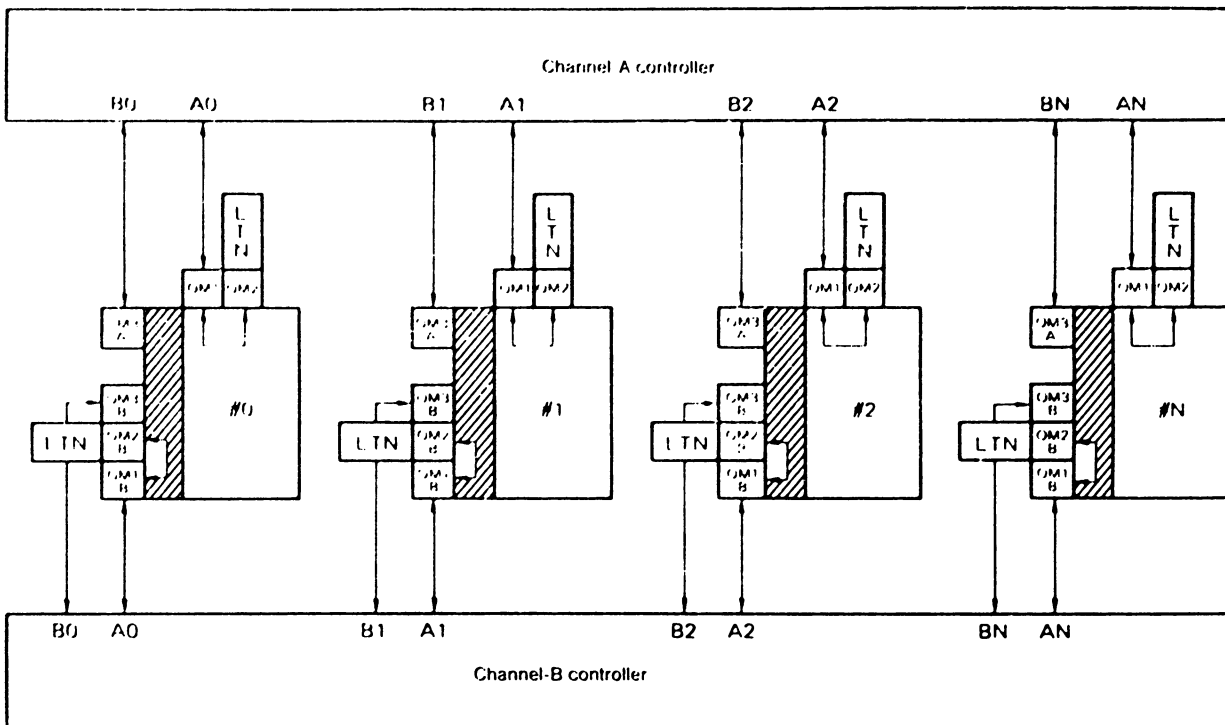
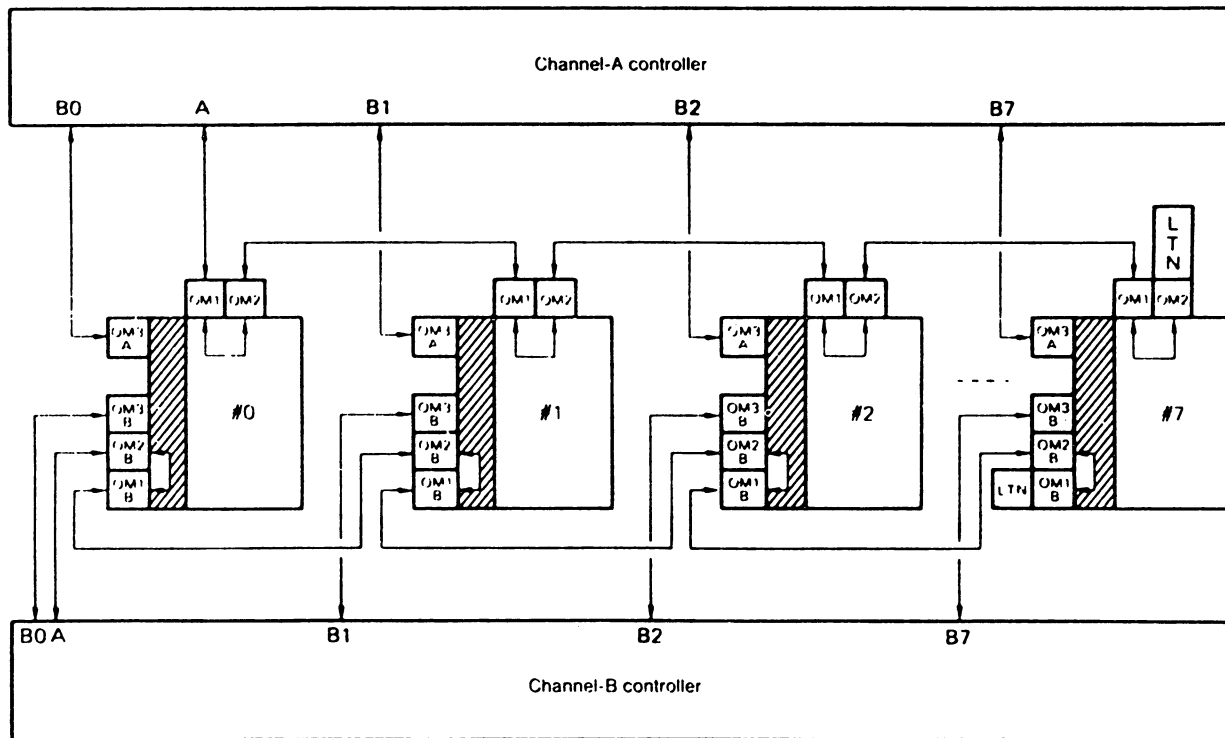


Figure 3.5.6 Interface Cabling (Dual Port)



(a) Star Connection

Note: Hatched areas denote dual port options



(b) Daisy Chain

Figure 3.5.7 System Interface Cabling (Dual Port)

3.5.4 System Grounding

- (1) The frame ground (FG) and signal ground (SG) within the FDU are separated. If the FG and SG connection is required on the system, connect the grounding cable as shown in Figure 3.5.8, or if the system ground is required between the system and FDU, connect the ground conductor to the GND terminal.

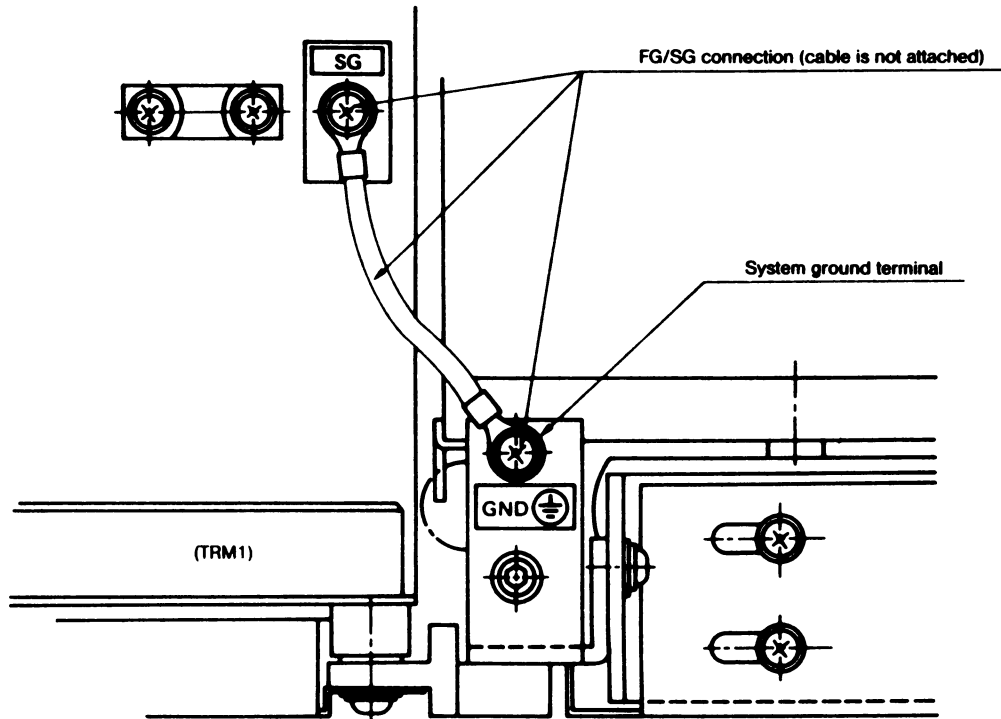


Figure 3.5.8 Ground Terminal on the Unit

- (2) The FG and SG terminals are provided with the optional power supply unit as shown in Figure 3.5.3. Connecting or disconnecting between FG and SG on the power supply unit can be performed according to system power distribution and system ground requirement.

- (3) When the interface cable is longer than 3m (10 feet), an auxiliary grounding cable should be connected among the control unit and disk units.

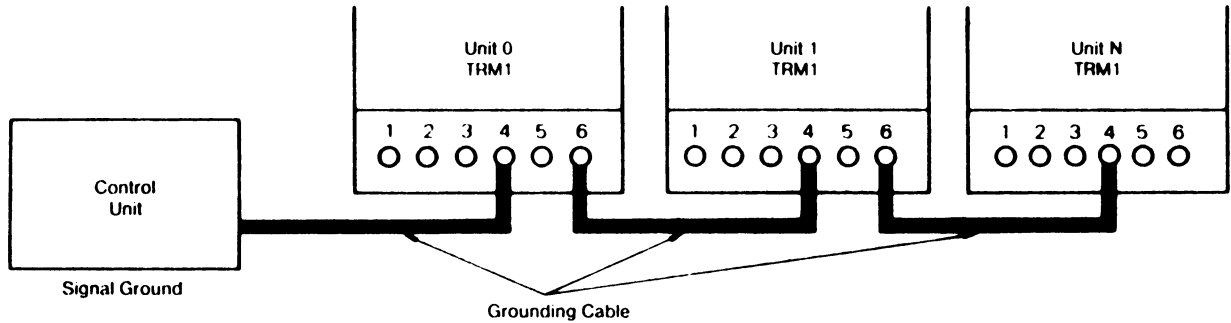


Figure 3.5.9 System Grounding

3.5.5 Mode Select Setting

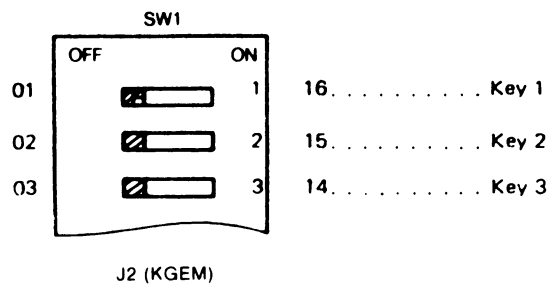
When the FDU M2298 is installed in the system, the customer must set the following modes according to system requirements: Disk Logical Unit Number, Tag 4/5 Enable and Sector Mode on KGEM PCB assembly and Sector Counting on VOIM PCB assembly.

3.5.5.1 Disk Addressing

Disk Logical Unit Number 0 to 7 is selectable on SW1 at location J2 on the KGEM PCB assembly. Set the desired disk address with three keys on SW1 using binary code as shown in Table 3.5.4.

Table 3.5.4 Disk Addressing

Disk Address	Key 1	Key 2	Key 3
	2^0	2^1	2^2
0	OFF	OFF	OFF
1	ON	OFF	OFF
2	OFF	ON	OFF
3	ON	ON	OFF
4	OFF	OFF	ON
5	ON	OFF	ON
6	OFF	ON	ON
7	ON	ON	ON



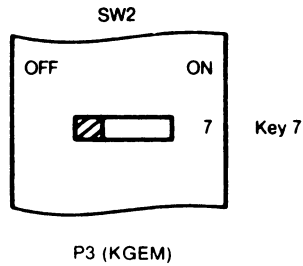
3.5.5.2 Sector Mode

The customer can select Hard Sector mode (1 to 128 sectors) using Key 7 on SW2 at location P3 on the KGEM PCB assembly according to Table 3.5.5.

In the case of Hard Sector, the customer must set the number of sectors per disk revolution as described in 3.5.5.4.

Table 3.5.5 Sector Mode

Sector Mode	Key 7
Hard Sector	OFF
Variable Soft Sector	ON

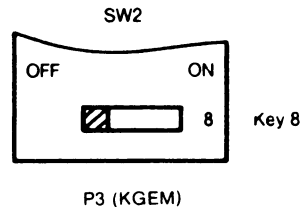


3.5.5.3 Tag 4/5 Enable

FDU M2298 provides optional Tag 4 and Tag 5 functions, however, the customer may disable or enable these functions using Key 8 on SW2 at location P3 on the KGEM PCB assembly. Disabling the Tag 4/5 functions inhibits the receivers of Tag 4 and Tag 5 on the interface.

Table 3.5.6 Tag 4/5 Enable

Tag 4/5	Key 8
Disable	OFF
Enable	ON



3.5.5.4 Sector Counting

Sector count configuration switches, SW1 and SW2, are located at R7 and P7 respectively on the VOIM PCB assembly. Each key of SW1 and SW2 represents the binary powers of 2 Bytes Clock as shown in Table 3.5.7.

Table 3.5.7 Sector Counting Keys

SW1 Key No.	Value	SW2 Key No.	Value
1	2	1	256
2	4	2	512
3	8	3	1024
4	16	4	2048
5	32	5	4096
6	64	6	8192
7	128	7	16384

SW1 and SW2 keys must be set according to the number of bytes per sector. Knowing that the number of bytes possible on a track equals 40,960, any sectoring requirement from 1 to 128 sectors per track can be configured using the following formula:

- (1) Calculation based on Sectors/Track
- (2) Calculation based on Bytes/Sector

Example: 584 Bytes/Sector

- 1) Calculate the value to be set.

$$= 16,384 - (\text{Byte/Sector})$$

$$= 16,384 - 584$$

$$= 15,800$$

- 2) Select the keys that must be in the OFF position referring to Table 5-7 after the following calculation.

$$15,800 = 8,192 + 4,096 + 2,048 + 1,024 + 256 + 128 + 32 + 16 + 8$$

Keys must be "OFF":

6	5	4	3	1		7	5	4	3
└──────────┘						└────────┘			
SW2						SW1			

- 3) Calculate the Sectors/Track

$$\text{Sectors/Track} = \frac{\text{Bytes/Track}}{\text{Bytes/Sector}}$$

$$= \frac{40,960}{584}$$

$$= 70,137$$

- 4) If the above calculation results in a remainder, truncate the remainder. The integer portion means actual sectors per track.

$$\text{Actual Sectors/Track} = 70$$

- 5) Calculate the number of the last sector (remainder).

$$\text{Last Sector Length} = 20,480 - (\text{Bytes/Sector}) \times (\text{Sectors/Track})$$

$$= 40,960 - 584 \times 70$$

$$= 80$$

Table 3.5.8 Commonly Used Sector Configurations

NO SECTORS	S1							S2							BYTE/SECT	LAST SECTOR SHORT
	1	2	3	4	5	6	7	1	2	3	4	5	6	7		
4	1	1	1	1	1	1	1	1	1	1	0	0	1	0	10,240	0
8	1	1	1	1	1	1	1	1	1	0	0	1	0	0	5,120	0
12	0	1	0	1	0	1	0	1	0	1	1	0	0	0	3,414	-8
16	1	1	1	1	1	1	1	1	0	0	1	0	0	0	2,560	0
24	1	0	1	0	1	0	1	0	1	1	0	0	0	0	1,708	-32
32	1	1	1	1	1	1	1	0	0	1	0	0	0	0	1,280	0
64	1	1	1	1	1	1	0	0	1	0	0	0	0	0	640	0
128	1	1	1	1	1	0	0	1	0	0	0	0	0	0	320	0

3.6 SHIPPING

Perform the following operations when the unit is to be shipped after mounting within a system:

- (a) Lock the spindle (refer to 3.4.3)

Caution: Rotate spindle in the direction indicated only

- (b) Lock the actuator (refer to 3.4.4)

- (c) Lock the motor (refer to 3.4.5)

- (d) Secure the slide locks; in vertical mounting mode, attach the vertical type mounting bracket to the cabinet so that excessive force is not applied to the rubber shock isolators. Process so that shock exceeding 5G is not applied to the unit during shipment.

When the unit is shipped by itself, the same operations (a to c) are required before packing into the proper carton.

3.7 STORAGE AND REPACKING

The FDU M2298 shipping carton is a reusable cardboard carton having a special double construction. When reshipping the unit, repack it in the original carton or a carton having equivalent functions.

When the environment is severe and the unit is to be stored for an extended period of time, it should be stored in the packed state.

Units can be stacked three cartons high.

When storing unpacked units, avoid dusty locations and locations where the environmental changes are extreme.

BLANK

Section 4

Theory of Operation

BLANK

4. THEORY OF OPERATION

4.1 GENERAL DESCRIPTION

The description of operation of the Fixed Disk Unit is divided into three parts. The first part describes the main assemblies of the unit. The second part describes the magnetic heads and magnetic disks. The third, and last part describes the interface, servo circuit, R/W control, and other electronic controls.

4.2 ASSEMBLIES

4.2.1 Disk Enclosure (DE)

The Disk Enclosure is a completely sealed unit containing the disks, spindle, actuator, and heads. Each of these are visible from the outside through a plastic cover. The DE is sealed at the factory and must not be opened in the field.

The DE is treated as one maintenance part.

The Read/Write PCB is mounted on the DE, but is an independent part.

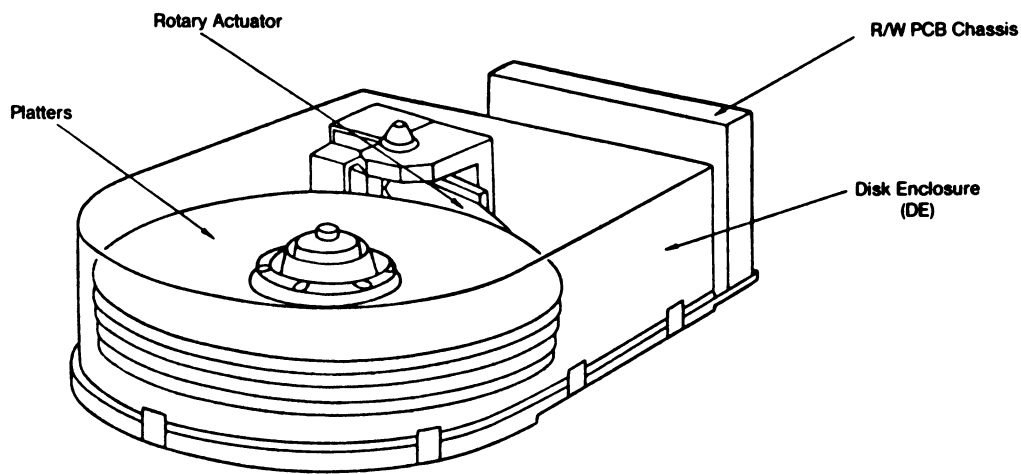


Figure 4.2.1 Disk Enclosure

4.2.2 Spindle Assembly

The disk spindle is mounted in the DE housing in the bottom of the disk enclosure. The housing is sealed to prevent air from entering through the bearings. A hub is attached to the top of the spindle, and disks (recording media) are clamped to the hub. A pulley is attached to the bottom of the spindle and is driven by the spindle drive motor with a flat belt. The spindle is grounded through a Spindle Brush mounted on the Grounding Plate.

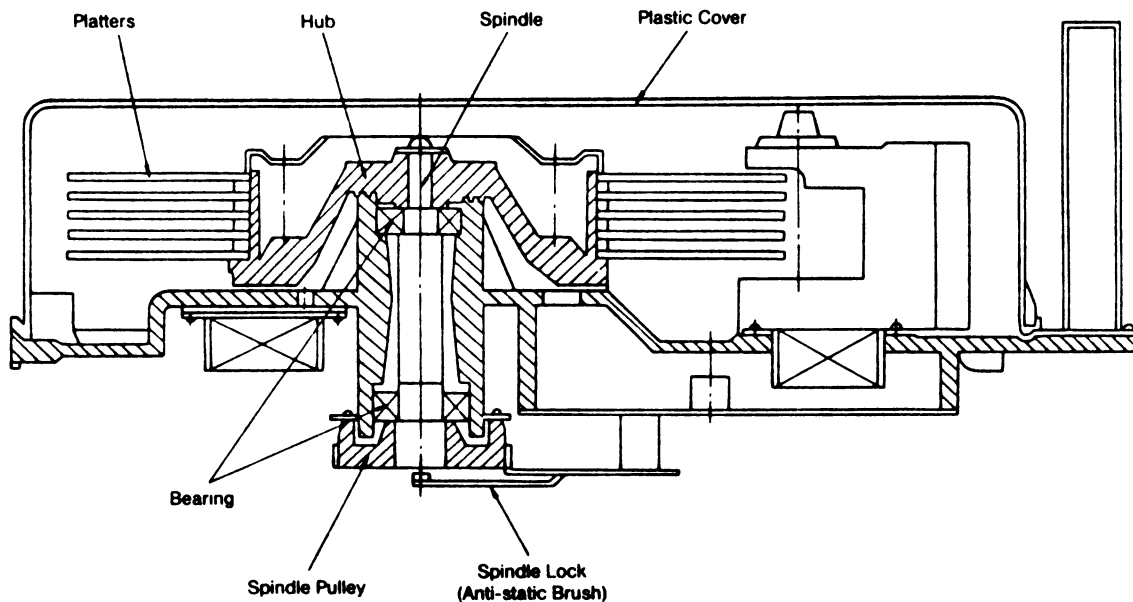


Figure 4.2.2 Spindle Assembly

4.2.3 Spindle Drive Motor and Brake

As this fixed-disk unit uses contact start/stop heads, the head-disk contact time must be minimized during rotation. Therefore, the disk drive system uses a thermally protected high torque motor for quick acceleration to nominal rotational speed and a brake for quick stopping.

Should overheating occur, the AC power to the motor is automatically disconnected and the rotational speed is gradually decreased. In this case the alarm signal is not sent to the power unit. When the temperature drops to an acceptable level, the motor will recover to nominal speed.

A flat belt connects the spindle drive motor to the spindle.

The motor is mounted so as to pivot, and sufficient tension is supplied to the belt by pulling the motor with a spring.

A brake is mounted at the top of the motor. This brake is actuated when the DC +24V is turned off. When the current at the brake coil is turned off, the brake pad is pushed to the brake plate by a spring and stops the motor.

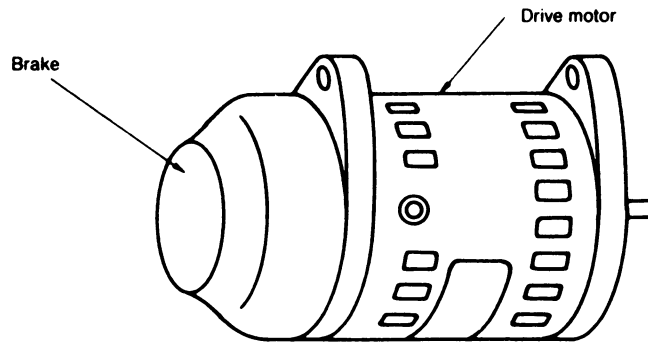


Figure 4.2.3 Disk Spindle Motor and Brake

4.2.4 Actuator Arm Assembly

A rotary type actuator with low power consumption and low heat dissipation is used to move the data heads and servo head to the specified cylinder along a circular arc.

A moving coil is attached to the other end of the actuator arm and moves freely between fixed permanent magnets without contact. When current is applied to the coil, interaction occurs between the coil and magnets and the actuator moves around the pivot.

The actuator performs the following types of motion, which are controlled by servo feedback current from the servo head:

- (1) **Positioning**
Heads are moved to the specified cylinder address.
- (2) **Track Following**
Heads follow the specified track to prevent mispositioning from disturbances such as shock, vibration, or temperature change.

The servo head is located on the lower surface of the bottom disk. Servo data is written on the outer recording area of this disk.

This data is used as a control signal for the actuator; that is, it is used as a track crossing signal for positioning or as a track following signal.

The heads are in contact with the disk surfaces during start and stop (C.S.S.) at a fixed position called the landing zone. A magnet is used to pull or fix the actuator at this position. If no current is applied to the moving coil, the heads are fixed at the landing zone.

Once the disks attain the required rotational speed, an initial seek instruction is issued. Current then flows in the coil and the heads are released from the landing zone and moved to the recording zones.

4.2.5 Actuator Lock, Spindle Lock

When the disks are stopped, the heads are in contact with the disks. The spindle and actuator are fixed with both the spindle lock and actuator lock for disk and head protection during maintenance, replacement, and transportation of the DE. (See Figures 3.4.5 and 3.4.6.)

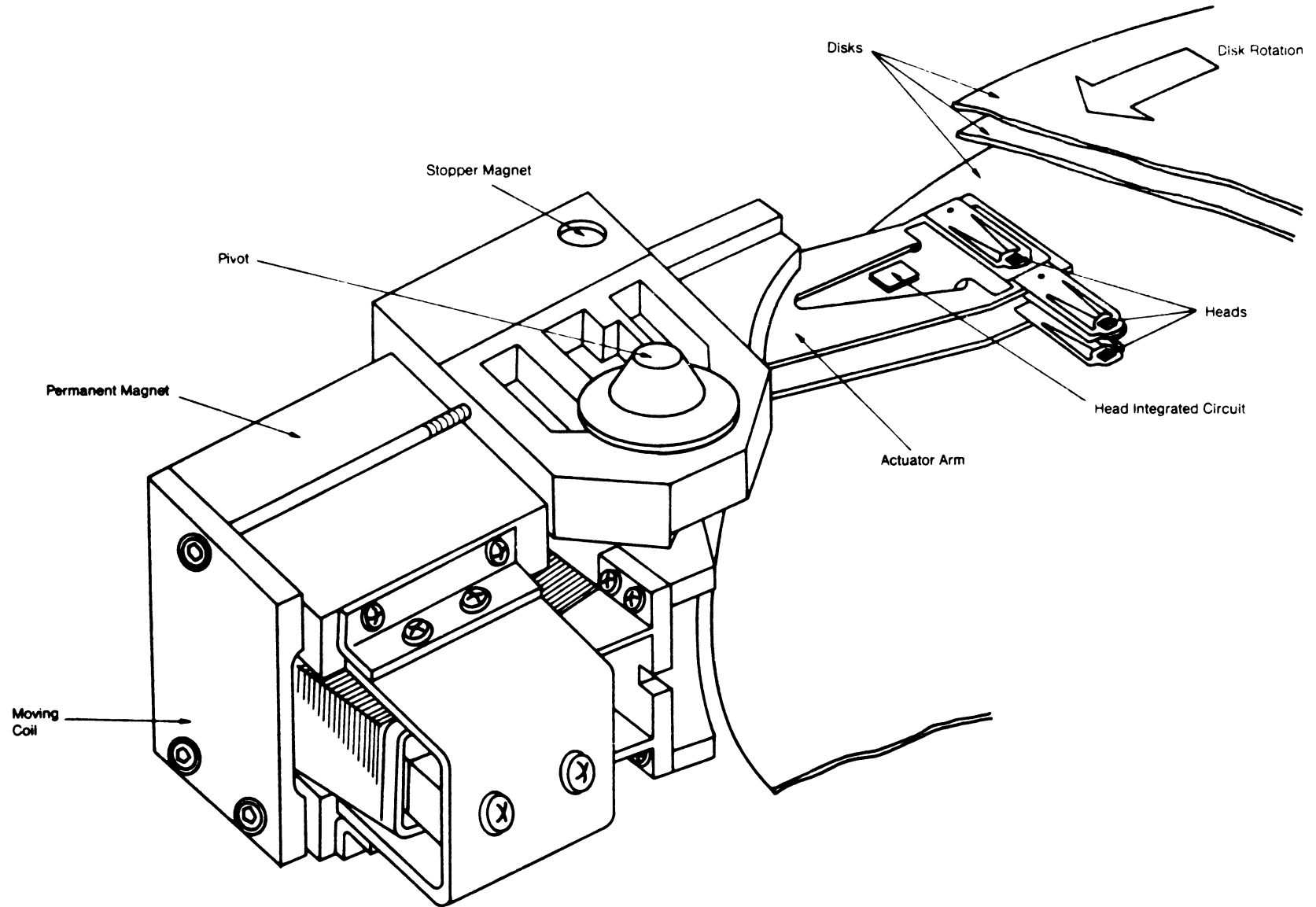


Figure 4.2.4 Actuator Arm Assembly

4.2.6 Air Circulation in DE

As the C.S.S. head used in this disk unit has a very low flying height (approximately 0.45um) head crashes could be caused by microscopic foreign particles. To keep the inside of the DE clean, this enclosure is completely sealed and clean air is supplied through two filters. One filter is used for external air exchange, while another filter is used as a re-circulation filter to keep the air inside the DE clean.

The breather filter is used for the following purposes:

- (a) Prevention of negative pressure in the vicinity of the spindle when the disk begins to rotate.
- (b) Prevention of dust intake when the air in the DE contracts due to a temperature difference between the DE and its environment.

The re-circulation filter, attached to the closed loop duct in the DE, is used to keep the air free of foreign particles. When a pressure difference is caused in the DE by the rotation of the spindle, the air in the DE circulates through the closed loop. Because it continually passes through this filter, the air is always kept clean.

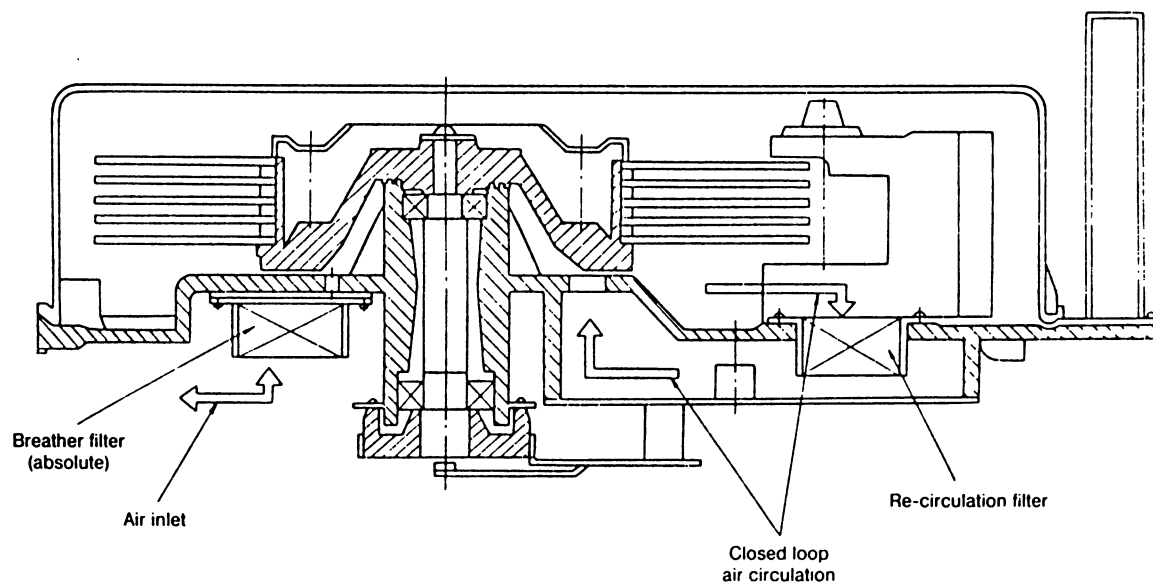


Figure 4.2.5 Air Circulation inside DE

4.2.7 Sub-frame

The sub-frame is supported by four vibration isolating rubber supports (three rubber supports for the vertical type). The disk enclosure is mounted on this sub-frame with three bolts and nuts. The DE can be easily replaced by removing these three nuts.

The DE is insulated from the sub-frame to prevent any influence from noise and vibration.

The sub-frame contains a duct to supply air from the cooling blower to the R/W PCB and the control PCB's.

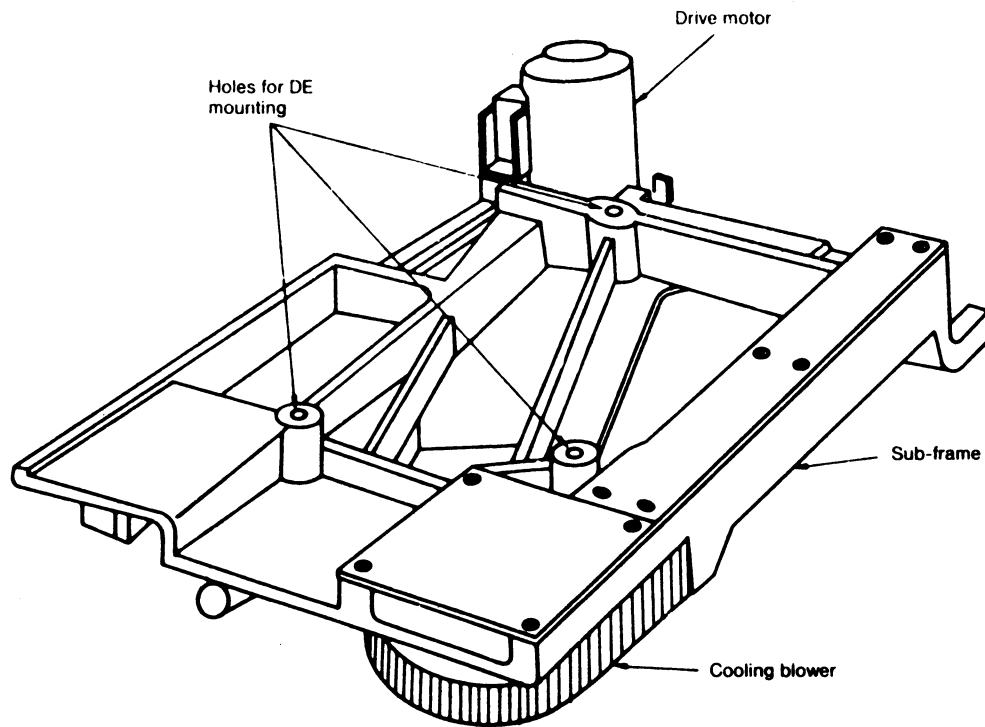


Figure 4.2.6 Sub-frame

4.2.8 Cooling

A cooling blower provides air to cool the printed circuit boards and motor. Cool air is always supplied from the front to the inside by this blower.

The air is sent through the duct in the sub-frame and divided into two channels. One cools the read/write printed-circuit board, and the other cools the printed-circuit boards in the chassis, and then the motor.

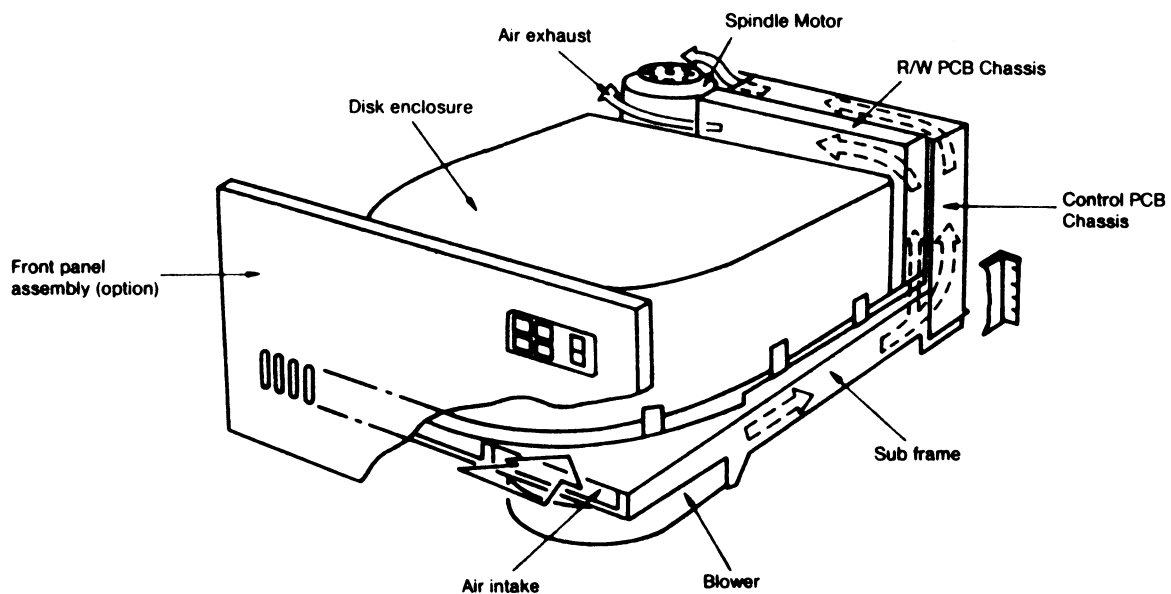


Figure 4.2.7 Cooling

4.3 MAGNETIC HEADS AND RECORDING MEDIA

4.3.1 Magnetic Heads

To accomplish high density recording, CONTACT START/STOP (C.S.S.) flying heads are employed. The heads fly on the surface air flow generated by the rotating disk. The C.S.S. system differs from the conventional ramp load system in that the heads are always over the recording media and rest on the disk surface when the disk is not rotating.

Therefore, the head and disk make contact, and the wear caused by this contact must be minimized. For this reason, the C.S.S. type head is lightly loaded and the surface pressure is reduced by using a tapered flat slider such as that shown in Figure 4.3.2. The slider has 3 rails. The air intake end of the slider is tapered to obtain flying force by means of the air flow over the disk surface. Reads and writes are performed by a ferrite core at the rear of the head, the minimum flying height position.

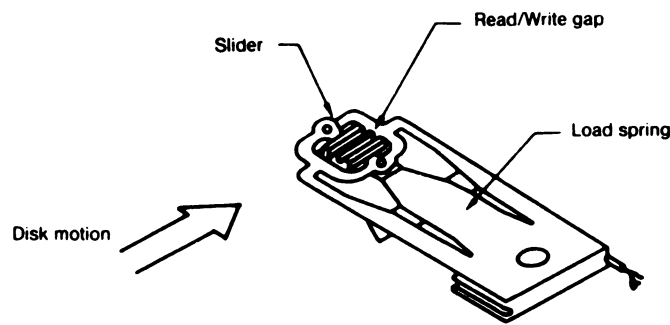


Figure 4.3.1 Read/Write Head

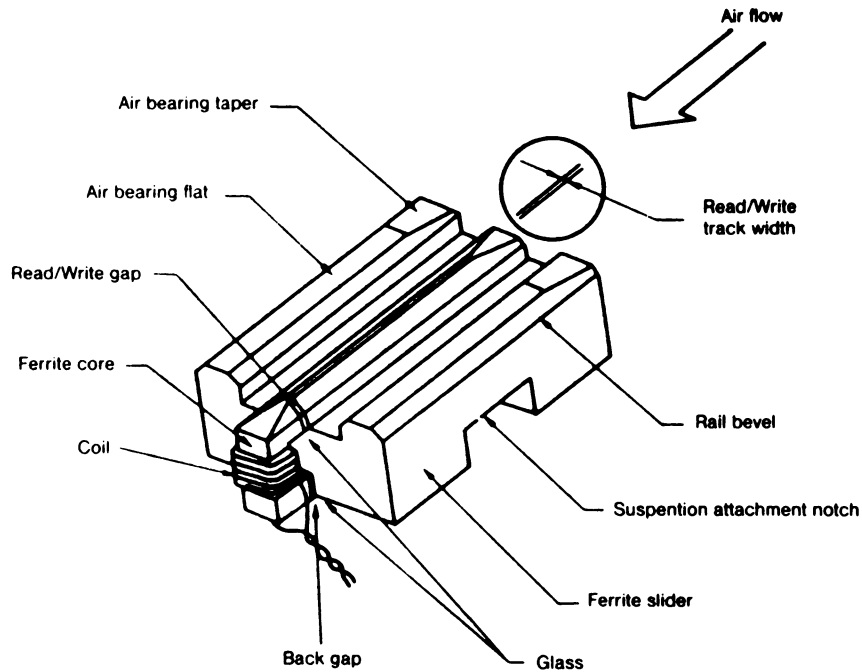


Figure 4.3.2 Tapered Flat Slider

4.3.2 Recording Media (Magnetic Disk)

A magnetic disk is an aluminum disk approximately 356mm (14 inches) in diameter and approximately 2mm (75mil) thick coated with a magnetic material and is used to record data. Since this unit employs CONTACT START/STOP type heads, to prevent wear, the surface is coated with a special material. Five disks are installed for a maximum storage capacity of 671MB. The outer portion, bottom surface of the lowest disk is for the servo area on which the positioning data and clock signals are recorded.

4.3.3 Servo Track Format

4.3.3.1 Servo track configuration

The servo area, the bottom surface of the bottom disk, is used to store unique data patterns (Servo data). This data is prerecorded on the disk before the unit is shipped from the factory and is accessed by the servo head (read only).

These unique data patterns are used to generate the Track Positioning, Index, Guard Band and Clock signals. They are analog signals as shown in Figure 4.3.3.

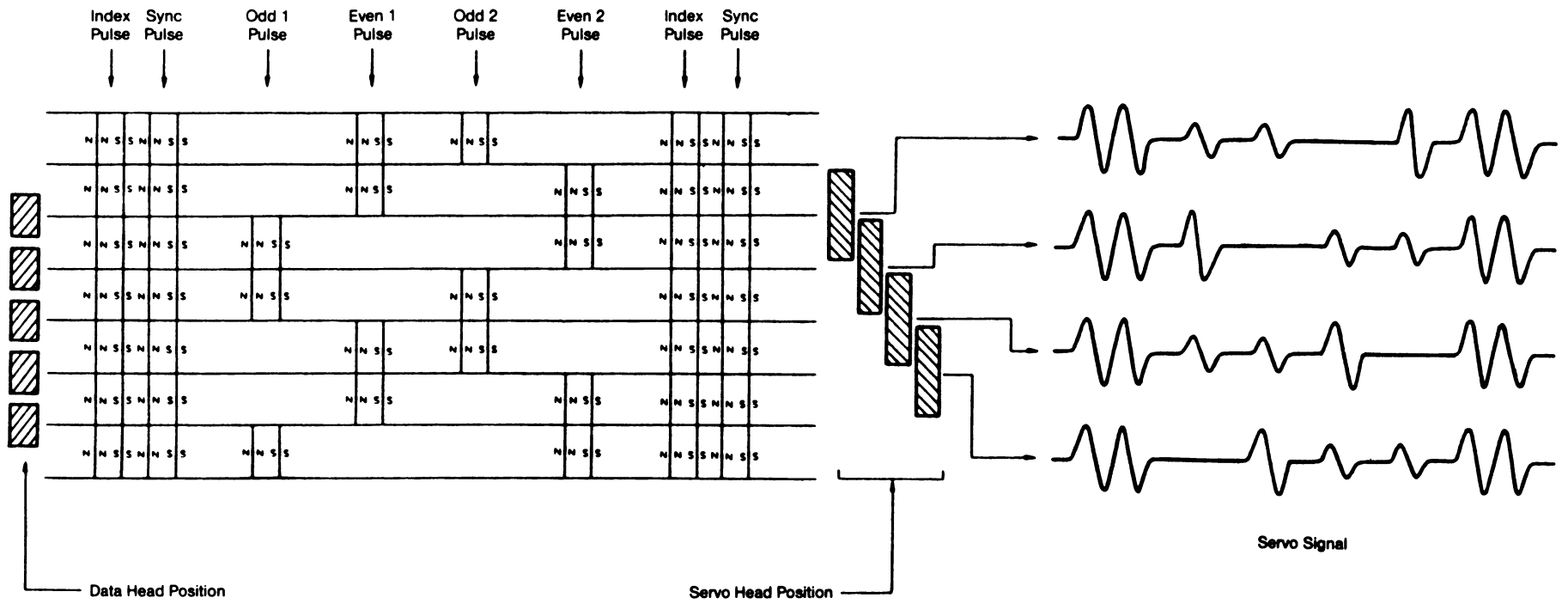


Figure 4.3.3 Dual-Phase Composite Servo Signal

The servo area consists of a combination of ODD1, ODD2, EVEN1 and EVEN2 tracks. The physical placement of servo tracks is shown in Figure 4.3.4. The servo tracks are divided into the following four parts:

- (1) Inner Guard Band 2 (IGB2)
Inner Guard Band 2 is used for speed control during RTZ or Initial seek sequence.
- (2) Inner Guard Band 1 (IGB1)
Inner Guard Band 1 is located between IGB2 and Cylinder 0, and is used for speed control during RTZ or Initial Seek sequence.
- (3) Servo Band
Servo band is used for tracking to determine the center of each cylinder.
- (4) Outer Guard Band (OGB)
The Outer Guard Band is used to recognize that the head has passed through the servo zone in an outward direction.

4.3.3.2 Servo Pattern

The servo signal is a “dual phase composite signal.” It is used to provide angular positioning information (location with reference to the Index Mark of the disk) and radial positioning information (location with reference to the cylinders/Guard Bands).

Index and Guard Band patterns are developed through the use of unique “sync patterns”. The sync patterns are a combination of normal and missing index bits and are written at the factory. Refer to Figure 4.3.5 and section 4.3.3.3.

Angular positioning information is derived from the sync pattern shown in Figure 4.3.5 (A). This sync pattern is decoded into the Index Signal which will appear once per revolution.

Radial positioning information is provided by writing ODD1-EVEN2, ODD1-ODD2, EVEN1-ODD2, and EVEN1-EVEN2 patterns, in that order, on the servo surface.

During head movement across the cylinders, the servo circuit detects the amplitude changes between ODD1 and EVEN1 peaks (phase 1), and between ODD2 and EVEN2 peaks (phase 2), and then converts them into two position signals (phase 1: Normal, phase 2: Quadrature) through the position sensing.

After head movement, the servo head, which has double the core width of the data head, settles on the border of two types of servo patterns controlled by the two least-significant bits of the target cylinder address. The servo circuit then makes the ODD1 (or ODD2) peak equal to the EVEN1 (or EVEN2) peak by positioning the servo head on the center of the servo track. Refer to Figure 4.3.3.

The sync patterns for IGB 2, IGB 1 and OGB are shown in Figure 4.3.5 (B-D) and described in section 4.3.3.3.

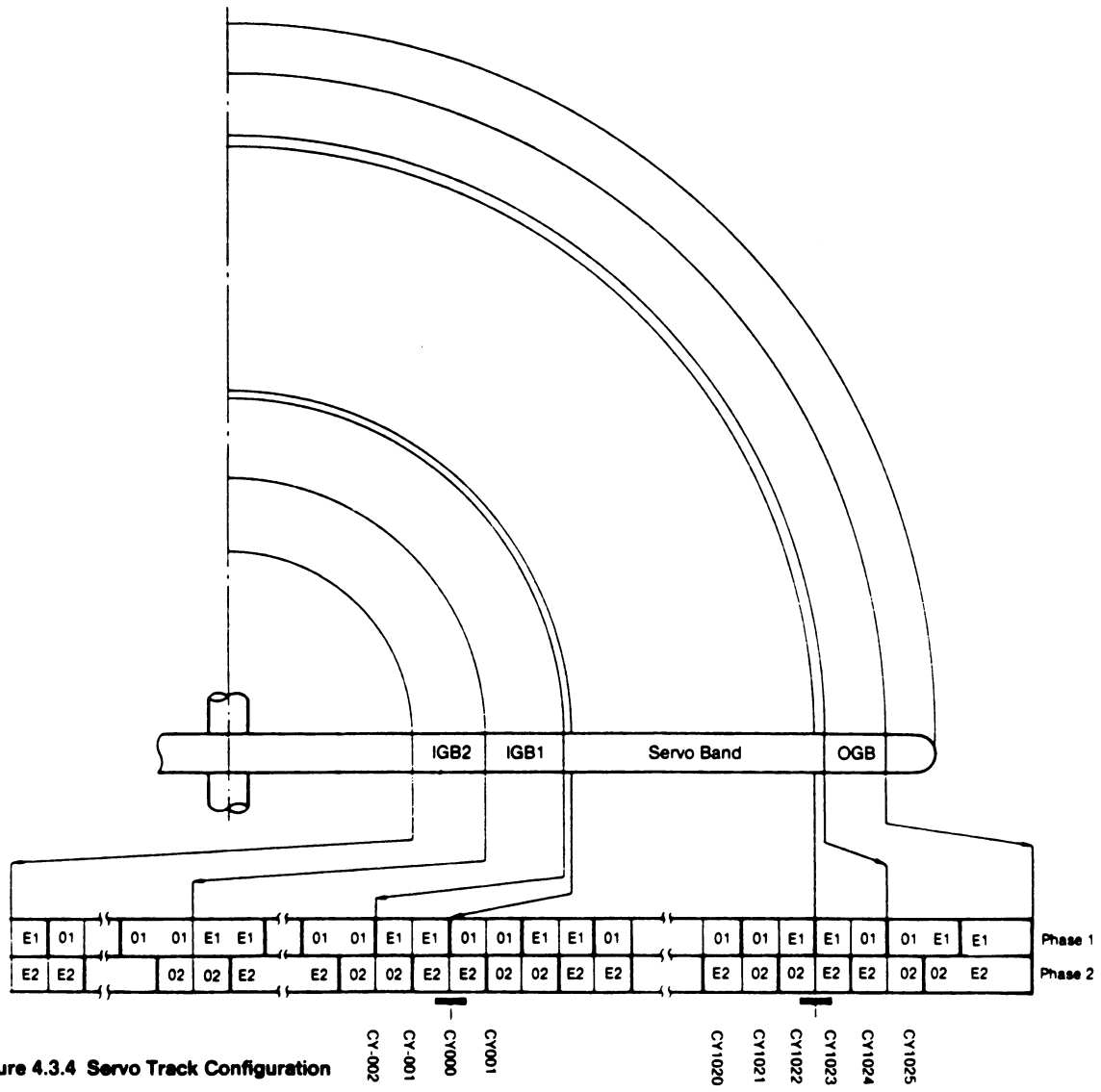
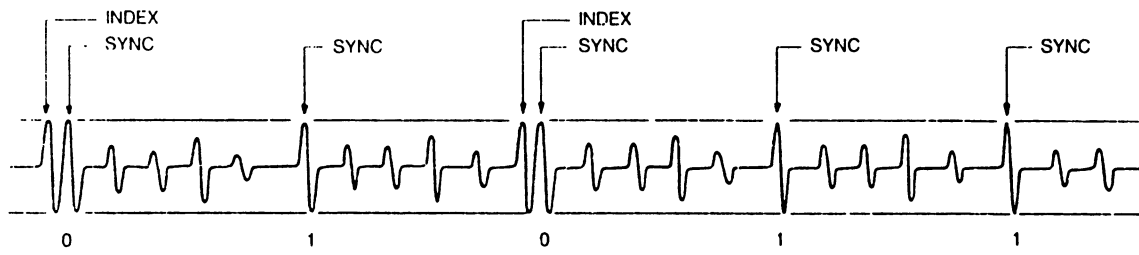
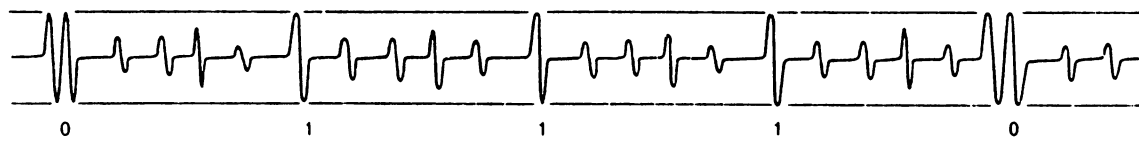


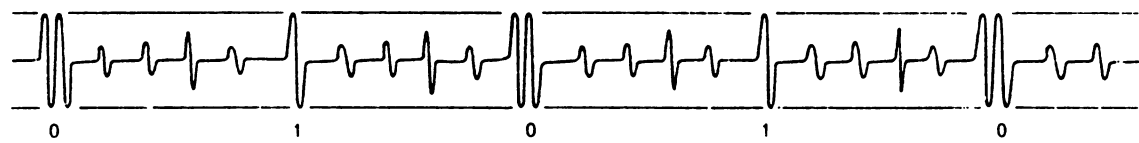
Figure 4.3.4 Servo Track Configuration



Valid index pattern
(A)



Inner Guard Band 2 pattern
(B)



Inner Guard Band 1 pattern
(C)



Outer Guard Band pattern
(D)

Figure 4.3.5 Index Pulse Pattern

4.3.3.3 Index, IGB2, IGB1 and OGB

Index, IGB2, IGB1 and OGB are detected by decoding the combination of Missing-bits and Normal-bits. Each of the patterns are shown in Table 4.3.1.

Table 4.3.1 Index/IGB2/IGB1/OGB Patterns

Signal	Pattern	Pattern Interval	Number/Revolution
Index	01011	40,960 B	1
IGB2	01110	512 B	79
IGB1	01010	512 B	79
OGB	10011	512 B	79

Note: 0: Normal Bit
1: Missing Bit

4.3.4 Data Surface Format

The data surface consists of all the disk surfaces except the servo surface and is composed of three basic parts.

- (1) Landing Zone (LZ)
The Landing Zone is the area the heads contact during Stop and Start. The Landing Zone corresponds to IGB2 on the servo surface.
- (2) Behind Home (BH)
Behind Home is the transition area on both sides of the data tracks and corresponds to IGB1 or OGB on the servo surface.
- (3) Data Track
The data track area consists of 1024 cylinders for data recording, with cylinder 0 being the innermost track and cylinder 1023 being the outermost track.

4.3.5 Head and Surface Configuration

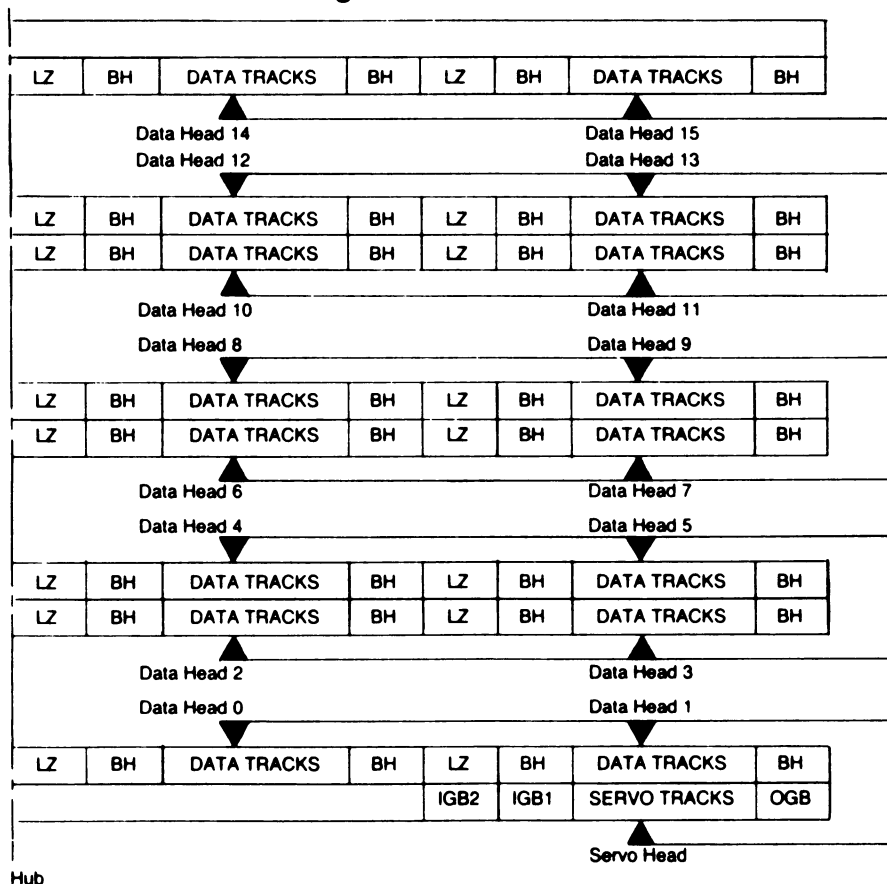


Figure 4.3.6 Head and Surface Configuration

4.4 FORMAT

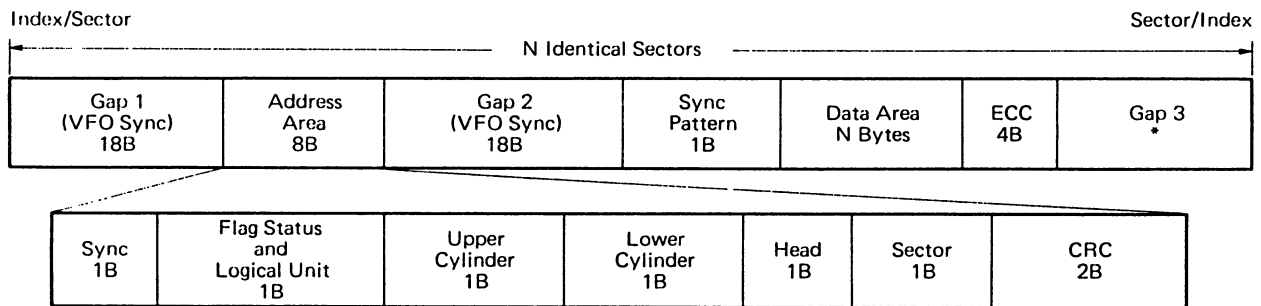
4.4.1 Description

A "sector" is an area assigned an address on the disk. Each sector consists of an Address Area (AA) to confirm that the correct sector has been read and a Data Area (DA) on which the actual data is recorded.

Index and sector pulses are used by the controller to find the beginning of the track and sector. Sector format is determined by the controller. Fixed Sector format can be used with this unit.

This recommended Fixed Sector format will be described in this section.

4.4.2 Fixed Sector Format



Example: 128 Sectors/Track

$$\begin{aligned} \text{Data Area} &= \frac{\text{Total Bytes/Track}}{\text{Sector/Track}} - (\text{Gap loss} + \text{Check Bytes}) \\ &= \frac{40,960}{128} - (49 + \text{GAP3}) = 256 \text{ Bytes} \end{aligned}$$

In Case of 256 bytes data length, GAP3 is 15 Bytes.

$$\text{Track Efficiency} = \frac{256 \times 128}{40,960} \times 100 = 80\%$$

Notes: 1) This format is an example only and may be structured to suit individual requirements.

2) The Sync Byte Sent on the 8-Cable will be recommended with a "19" (Hex) pattern.

3) Fixed sectors per track may be any number from 1 through 128 and can be selected by setting the configurator switches on the PCB (VOIM). Refer to 5.4.4.

4.4.3 Description of Format Parameters

4.4.3.1 Fixed Sector Format

- (1) Gap 1
This gap allows for displacement of the head and circuit tolerances under worst case conditions. This gap must be a minimum of 18 bytes long.
- (2) VFO Sync
All "0"'s are written and used to synchronize the data from the disk and the read/write clock from the disk VFO circuits.
- (3) Sync Pattern
This pattern represents the start of the address area. The sync pattern is the same as that before the data area, but the address area sync and data area sync byte may be different.
- (4) Flag Status and Logical Unit
This indicates the status of the disk on the sector. Normal record, primary record, or secondary record condition may be indicated. This specification is a function of the control unit.
- (5) Upper Cylinder, Lower Cylinder
This indicates the cylinder address of the track.
- (6) Head Address
This indicates the head address of the track.
- (7) Sector Address
This indicates the Sector address of the track.
- (8) CRC (Cyclic Redundancy Check)
This is a check byte used to check whether the data was read correctly.
- (9) Write Splice
When the address and data areas are written separately, this is the location of the read/write head transitions.
- (10) VFO Sync
All "0"'s are written and used to synchronize the data from the disk and the read/write clock from the disk VFO circuits.
- (11) Sync Pattern
Indicates the beginning of the data area. The recommended pattern is "14(Hex)". Refer to (3).
- (12) Data area
The data is actually recorded at this area.
- (13) ECC
ECC byte to insure the data area information has been read correctly.
- (14) Gap 3
This eliminates the possibility of destroying the end of a record written with a late displacement head.
This is the delay allowance for the control unit. It should be written all "0"'s.

4.5 INTERFACE

4.5.1 Introduction

4.5.1.1 Purpose

This section describes the logical and physical specifications for signal transfer within the interface between a Fixed Disk Unit (FDU) and the control unit.

4.5.1.2 Application

The following are SMD interface specifications and apply to the M2298.

4.5.1.3 Connection

The external connection (for transmitting and/or receiving interface signals for the unit) consists of two connectors, "A" and "B", which are connected, respectively, to cables "A" and "B". "A" cables may be connected in a daisy-chain configuration. Therefore, a line terminator must be inserted into the "A" connector of the last device. "B" cables are connected in a star configuration. Therefore, the control unit requires "B" cables and connectors to match the number of units to be connected.

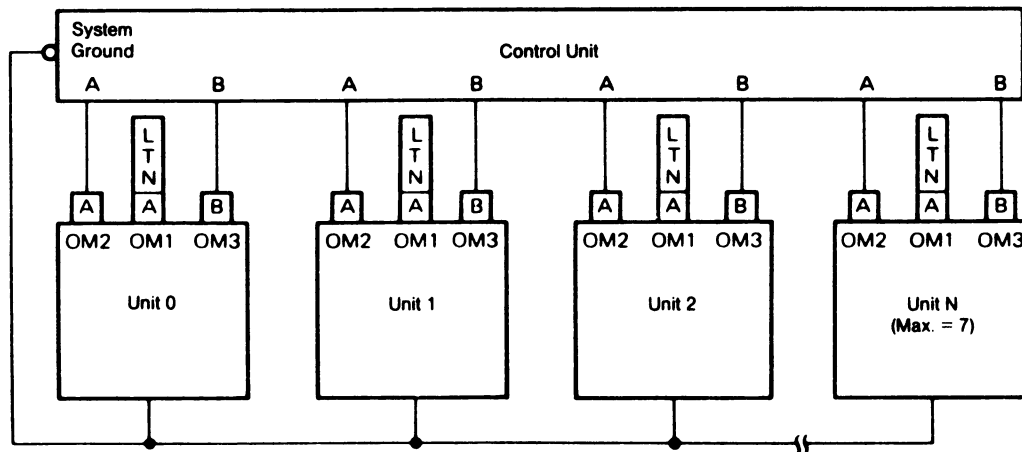
4.5.1.4 Time Specification

Timings are specified at the connector position of the unit. Accordingly, it is necessary for signal timings to consider both the delay time of the interface cable and the circuits of the disk control unit.

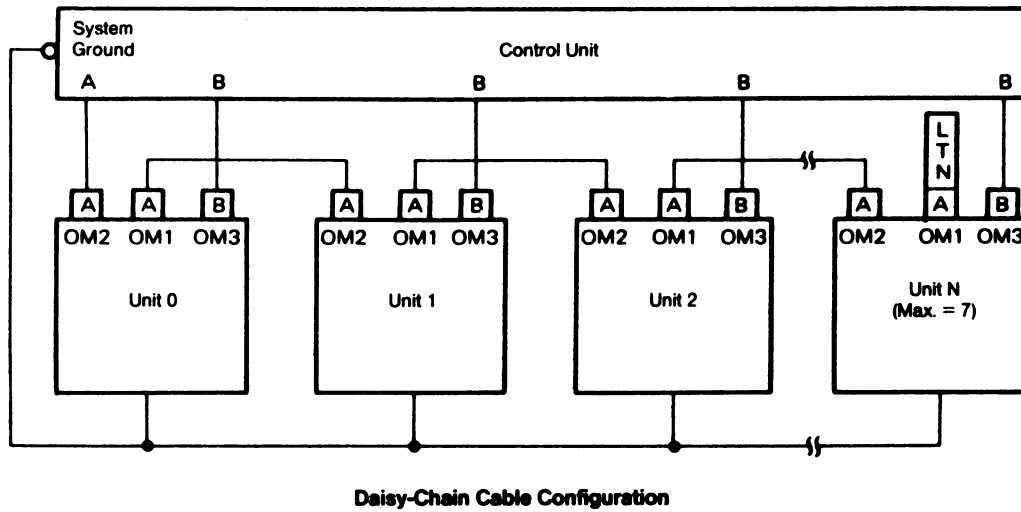
4.5.1.5 Interface Transmitter/Receiver

Transmitters and receivers of SN75110 and SN75107 or equivalent are used to provide a terminated, balanced-line transmission system. Refer to Section 4.5.7.

4.5.2 Interface Cabling



Star Cable Configuration



- Notes: (1) Line terminators (LTN) are required on the control unit and each unit in a star cable configuration.
 (2) Line terminators are required on the control unit and last drive in a daisy-chain cable configuration.

Figure 4.5.1 Interface Cabling

4.5.3 Type and Name of Signal Lines

4.5.3.1 "A" – Cable Lines for Balanced Transmission

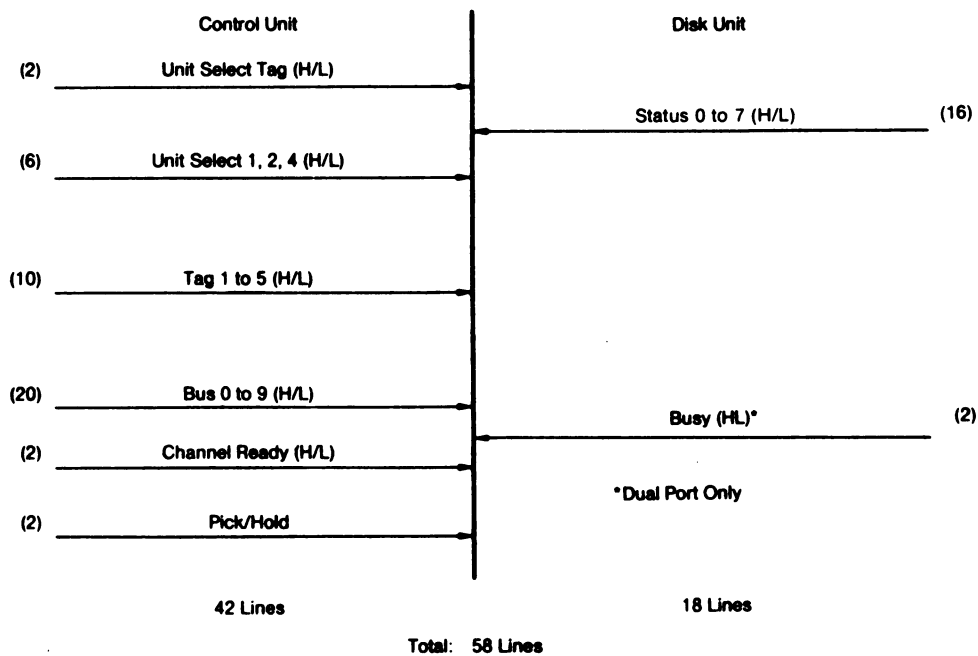


Figure 4.5.2 "A" Cable Signals

4.5.3.2 "B" – Cable Lines for Balanced-line Transmission

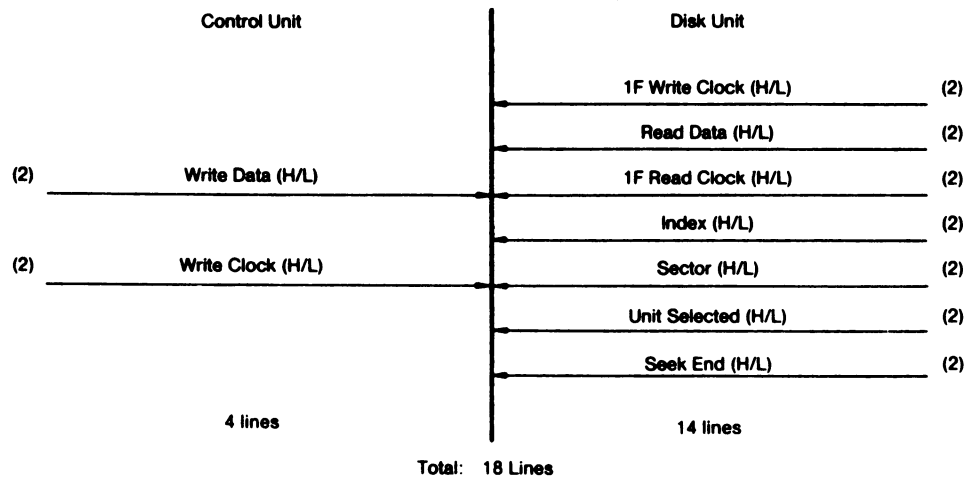


Figure 4.5.3 "B" Cable Signals

4.5.4 Description of Signal Lines

4.5.4.1 "A" – Cable Input Signal

- (1) Unit Select Tag
This signal gates Unit Select 1, 2 and 4 to select the desired disk. Refer to timing of Unit Select 1, 2 and 4 (Figure 4.5.6).
- (2) Unit Select 1, 2 and 4
These three signals are binary-coded to select the desired disk and are validated by the leading edge of Unit Select Tag. The logical disk number (0 through 7) is selectable by means of a switch located on the PCB card.
- (3) Tag 1 to 3 and Bus 0 to 9

Table 4.5.1 Tag/Bus Lines

Bus	Tag 1	Tag 2	Tag 3	Unit Select Tag ²
	Cylinder Address	Head Address	Control Select	
0	1	1	Write Gate	—
1	2	2	Read Gate	—
2	4	4	Servo Offset Plus	—
3	8	8	Servo Offset Minus	—
4	16	—	Fault Clear	—
5	32	—	—	—
6	64	—	RTZ	—
7	128	—	—	—
8	256	—	—	—
9	512	—	Release ¹	Priority Select ¹

Note 1: Dual Port Only.

2: Validates (or gates) the Unit Select 1, 2, and 4 lines in addition to the dual port priority select line.

- (4) **Cylinder Address (Tag 1)**
The cylinder address is set by Tag 1 and bus lines (Bus 0 to 9) on the unit. However, throughout Tag 1, the bus lines must be stable. Refer to Figures 4.5.8 to 4.5.10.
- (5) **Head Address (Tag 2)**
The head address is set by Tag 2 and Bus 0 to 3 on the unit; however, throughout Tag 2, Bus 0 to 3 must be stable. Refer to Figure 4.5.10.
- (6) **Control Select**
Bus lines 0 to 9, specified by Tag 3, have a different meaning in each bit. All signals are defined as control signals.
- (6)-1 **Write Gate (Bus 0)**
This signal enables the write operation on the specified track. This signal is validated under the following conditions:

Unit Ready	True
On Cylinder	True
Seek Error	False
Device Check	False
Channel Ready	True
File Protect	False
Offset	False

If Write Gate is turned on in cases other than the above-mentioned conditions, Device Check occurs and writing is inhibited. Refer to the definition of a Device Check.

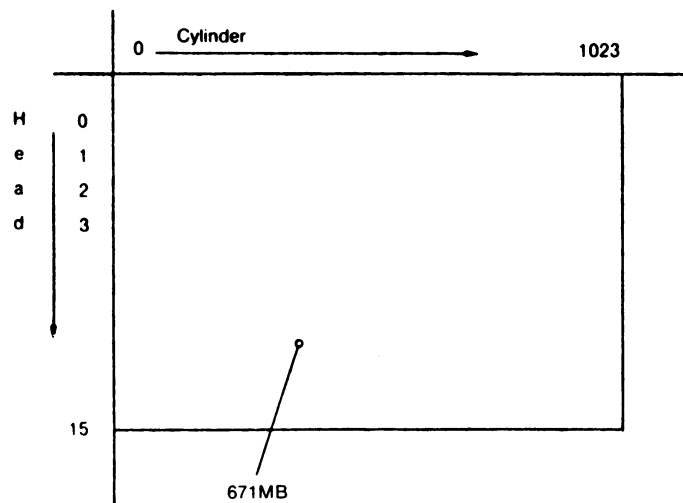


Figure 4.5.4 Storage Addressing M2298

- (6)-2 Read Gate (Bus 1)
This signal is used to recover data from the specified track. Refer to the timing of Read Gate and Read Data in Figure 4.5.23 and Figure 4.5.24.
- (6)-3 Servo Offset Plus (Bus 2)
When Servo Offset Plus signal is true, the head is offset 3.0um from nominal On Cylinder position, away from the spindle. Refer to Figure 4.5.11. When false, a 4ms delay is required before writing.
- (6)-4 Servo Offset Minus (Bus 3)
When Servo Offset Minus signal is true, the head is offset 3.0um from nominal On Cylinder position, towards the spindle. Refer to Figure 4.5.11. When false, a 4ms delay is required before writing.
- (6)-5 Device Check Clear (Bus 4)
This signal clears the device check status; however, if sources of a device check still exist (refer to Device Check), this status is not cleared.
- (6)-6 RTZ (Return to Zero) (Bus 6)
No matter where the data heads are located on the media, they are returned to cylinder zero and head zero by the RTZ signal. This signal clears the Seek Error flip-flop. Refer to Figure 4.5.13.
- (6)-7 Release (Bus 9)
The Release command releases Channel Reserve and Unconditionally Reserve in the drive, making alternate channel access possible after selection by the other channel ceases.

If the customer desires the Release Timer feature using the Release Time switch on the optional Dual Port PCB assembly, release will occur 500ms (nominal) after the deselection of the drive. Refer to Figure 4.5.6 and Figure 4.5.7.
- (7) Channel Ready
This signal is used to prevent damage to the file caused by interface disturbances when the control unit power is lost. Therefore, this signal must be stable when the control unit is available, and must be disabled before logic levels decay at the interface lines when a power failure of the control unit occurs. Refer to Figure 4.5.14.
- (8) Tag 4 and Tag 5 (Selectable)
When Tag 4 goes true, the unit issues Sector Address Status signals on the Status 0 to 7 lines.

When Tag 5 goes true, the unit issues Device Check Status signals on the Status 0 to 5 lines.

When both Tag 4 and Tag 5 are true, the Device Type Code will be issued in BCD on the Status 0 to 5 lines. See Table 4.5.2 and Figure 4.5.15.
- (9) Pick and Hold
Power Sequencing requires that the mode switch on the power supply unit be set to Remote.

When the control unit sets the Pick and Hold lines to ground, the first FDU starts up the power sequence. Once this FDU has reached nominal speed, the Pick signal is transferred to the next FDU, and repeated until all FDU's are powered up. When the mode switch on the power supply is set to Local, each FDU must be powered up manually.

(10) Priority Select (Dual Port Only)

When the control unit issues Unit Select Tag and Bus Bit 9 with a specified disk address, the disk drive will be unconditionally selected and absolutely reserved by the channel issuing the command, providing both channels are enabled and a priority select condition does not exist on the opposite channel. Once the drive is unconditionally reserved by a Priority Select command, the respective channel has exclusive access to the drive. The opposite channel can access it only after Release command has been issued by the selected channel. Refer to Figure 4.5.7. When a dual port drive is unconditionally reserved, all interface signal are inhibited on the other channel, including unit selected and Busy signals.

4.5.4.2 A — Cable Output Signal

(1) Status 0 to 5

The status 0 to 5 lines display status information determined by combinations of Tag 4 and Tag 5 signals. Information available on status lines 0 to 5 during various status of Tag 4 and 5 is specified in Table 4.5.2.

Table 4.5.2 Status Lines Determined by Tag 4/5

Tag 4	False	True	False	True
Tag 5	False	False	True	True
Status	Unit Status	Sector Address	Check Status	Device Type
0	Unit Ready	Sector Address 1	Control Check 1	Device Type 1
1	On Cylinder	2	2	2
2	Seek Error	4	Read/Write Check 1	4
3	Device Check	8	2	8
4	File Protected	16	3	16
5	—	32	4	32
6	Index	64	—	64
7	Sector	128	—	128

(A) Unit Status

(1) Unit Ready

When this signal is true, and the unit is selected, this signal indicates the unit is up to speed, and no fault condition exists within the unit.

(2) On Cylinder

This line indicates that the heads are located on the specified track (cylinder).

(3) Seek Error

This signal indicates that a seek error has occurred. In this case, the On Cylinder signal does not always go true. The Seek Error is cleared only by performing an RTZ (Tag 3 and Bus 6). Seek Error status is defined as follows:

- Seek was unable to complete a move within 704ms.
- RTZ was unable to complete a move within 704ms.
- The heads have moved to a position outside the recording area.
- An illegal cylinder address was issued to the FDU.
- Heads have overshot the new cylinder address.

(4) Device Check

This signal indicates that a fault condition exists in the unit. The following fault conditions may be detected by the unit.

a) Control Check 1

Instructions received during Not Ready status.

- b) **Control Check 2**
Instructions received during fault condition status. Write Gate received during an off-set operation, reading or Seek Error condition.
- c) **Read/Write Check 1**
Write Gate received during Off-track status or VCM overcurrent.
- d) **Read/Write Check 2**
Write fault or write current detected during a not-write operation.
- e) **Read/Write Check 3**
Write Gate received during write protected status.
- f) **Read/Write Check 4**
Write or Read Gate received when multiple heads are selected.

If an above-mentioned condition has occurred, writing is immediately inhibited and a Device Check signal is issued to the control unit. The device check status is cleared by the following operations:

- Fault Clear on Tag 3 and Bus 4
- Fault Clear on the operator panel (if operator panel is employed)
- Fault Clear Switch on the PCB chassis

Device Check Status turns on the check lamp on the operator panel as well as Maintenance Aid LED's on PCB chassis.

(5) File Protected

File Protected signal indicates that the FDU is in write-protected status. The File Protect function is enabled by the following switches:

- File Protect Switch on the operator panel (option)
- File Protect Switch on the PCB chassis

Attempting to write while protected will cause a Device Check (Read/Write Check 3) to be issued to the control unit.

(B) Sector Address 1 to 128 (Status Lines 0 to 7)

Eight-bits of binary-coded Sector Address are transferred from the Sector Counter, reset by the trailing edge of index, clocked by the trailing edge of Sector, and indicate the current sector address in the unit. Sector Address (Status Lines 0 to 7) will be issued to the control unit by activating Tag 4.

Refer to Figure 4.5.16 for timing of Sector Address (status lines 0 to 7).

(C) Device Check (Status 0 to 7)

Refer to item (A) - (4).

(D) Device Type (Status lines 0 to 7)

Enabling selectable Tag 4 and Tag 5 lines, causes key-selected Device Type Status to be issued to the control unit as Status 0 to 7 signals. Binary-coded Device Type signals are specified as shown in Table 4.5.3.

Table 4.5.3 Device Type Code

Device Type	Code (Hexadecimal)	Status							
		7	6	5	4	3	2	1	0
		2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰
M2298	20	0	0	1	0	0	0	0	0

Notes: 0: False
1: True

- (2) **Index**
This signal occurs once per revolution and is used for reference in read/write operation.
Refer to Figure 4.5.16 for the timing of Index and Sector.
- (3) **Sector**
The Sector Mark is derived from the servo track. The number of sectors per revolution is switch selectable and is determined by counting 2 Byte Clock. The switches are located on the VFO card within the PCB chassis. Each key of SW1 and SW2 represents binary powers of 2 Byte Clock.
- (4) **Busy (Dual Port Only)**
If the drive is already selected and/or reserved, a Busy signal will be issued to the "A" cable and the Unit Selected signal will be issued to the "B" cable of the channel attempting the select function. The Busy signal will remain until the Unit Select Tag is negated or the drive is no longer busy. Unit Selected signal should be used to enable Busy in the control unit. Refer to Figure 4.5.6.

4.5.4.3 B – Cable Input Signal

- (1) **Write Data**
This line carries NRZ data which is to be written on the disk surface and must be synchronized with Write Clock. Refer to Figure 4.5.17.
- (2) **Write Clock**
Write Clock is a return signal of the 1F Write Clock issued from the unit, and must be synchronized with the NRZ Write Data. Refer to Figure 4.5.17.

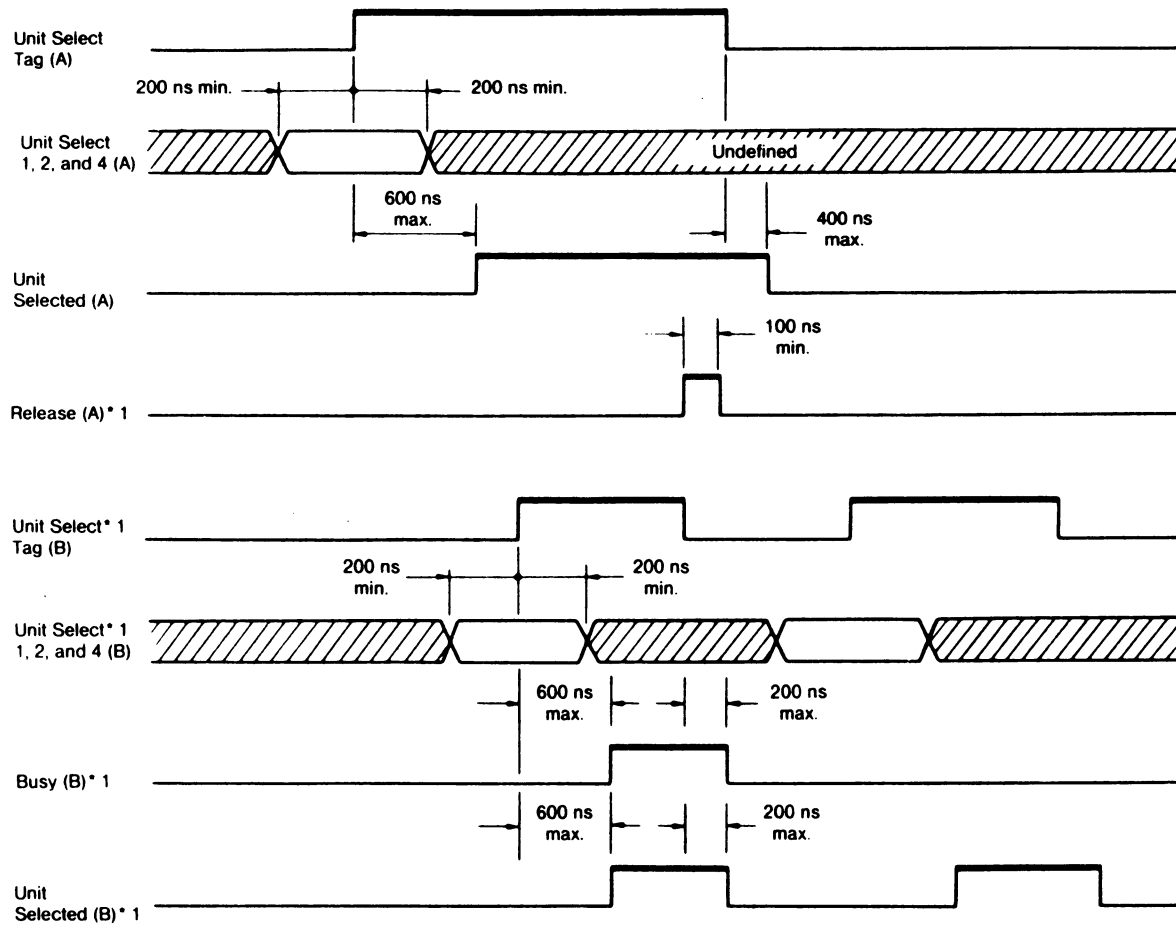
4.5.4.4 B – Cable Output Signal

- (1) **1F Write Clock**
This signal is used by the control unit to synchronize Write Data and Write Clock. 1F Write Clock is available during Unit Ready except during read operations. Refer to Figure 4.5.17.
- (2) **Read Data**
This line transmits the recovered data in the form of NRZ data synchronized with 1F Read Clock. Refer to Figure 4.5.18.
- (3) **1F Read Clock**
This line transmits 1F Read Clock which defines the beginning of a bit cell. The Read Data is synchronized with the 1F Read Clock. Refer to Figure 4.5.18.
- (4) **Unit Selected**
When the three unit select lines compare with the logical address of the unit, and when the leading edge of Unit Select Tag is received, the Unit Selected Signal goes true and is issued to the control unit. This signal also activates all status lines at the A–Cable.
- (5) **Seek End**
Seek End signal is a combination of On Cylinder and Seek Error, indicating that a Seek, RTZ, or Offset operation has terminated.
In the Dual Port function, the Seek End signal sent to the unselected channel will normally be a constantly true signal level. However, if the drive is selected by one channel, and the other channel receives a select, the Seek End signal sent to the waiting channel will go false for 30 μ s, when the Select and Reserve latches are reset on the selected channel.
- (6) **Index, Sector**
The Index and Sector pulses are issued on the interface for reference during read/write operations.

4.5.5 Control Timing

4.5.5.1 Unit Selection

Refer to Figure 4.5.6.

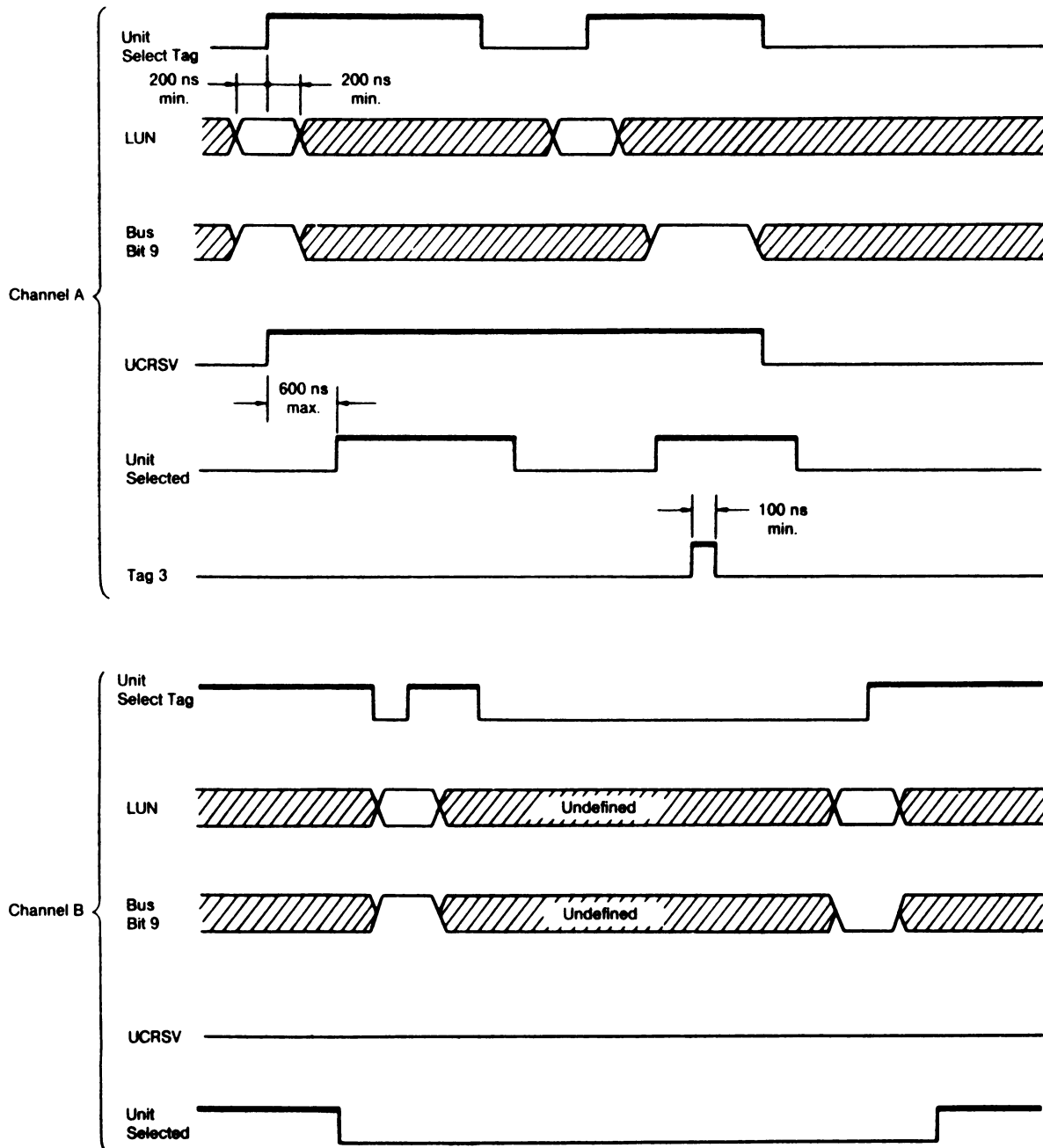


Note: * 1 – Dual Port only.

Figure 4.5.5 Unit Select Timing

4.5.5.2 Priority Select Timing (sample)

Refer to Figure 4.5.7.



- Notes: (1) LUN: Logical Unit Number (Unit Select 1, 2 and 4).
 (2) UCRSV: Unconditionally Reserved (Priority Selected).
 (3) Sample Sequence is as follows;
 CHB Selected → CHA Priority Select → CHB Priority Select → CHA Release → CHB Select

Figure 4.5.6 Priority Select Timing

4.5.5.3 Direct Seek Timing (Tag 1)

Refer to Figure 4.5.8.

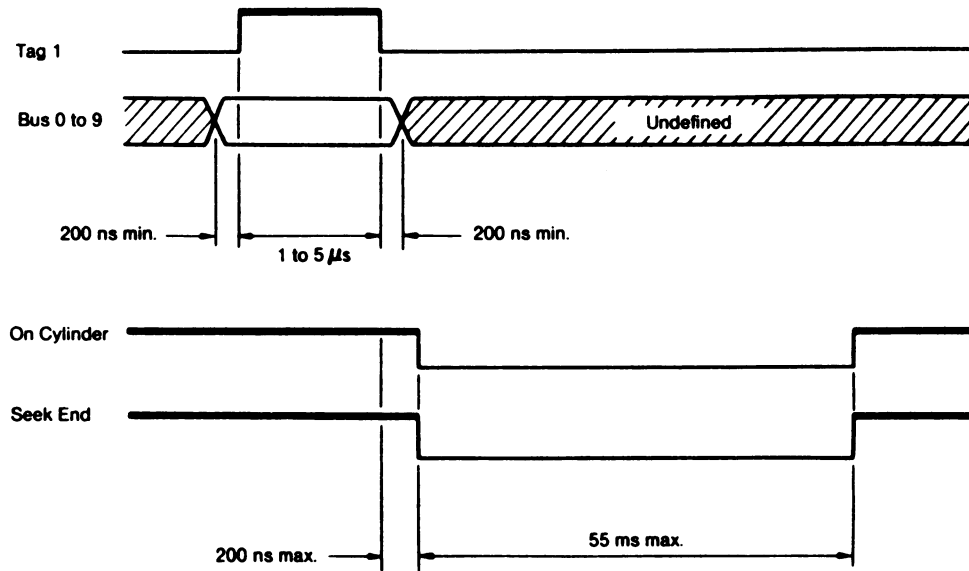


Figure 4.5.7 Direct Seek Timing

4.5.5.4 Zero Track Seek Timing

Refer to Figure 4.5.9.

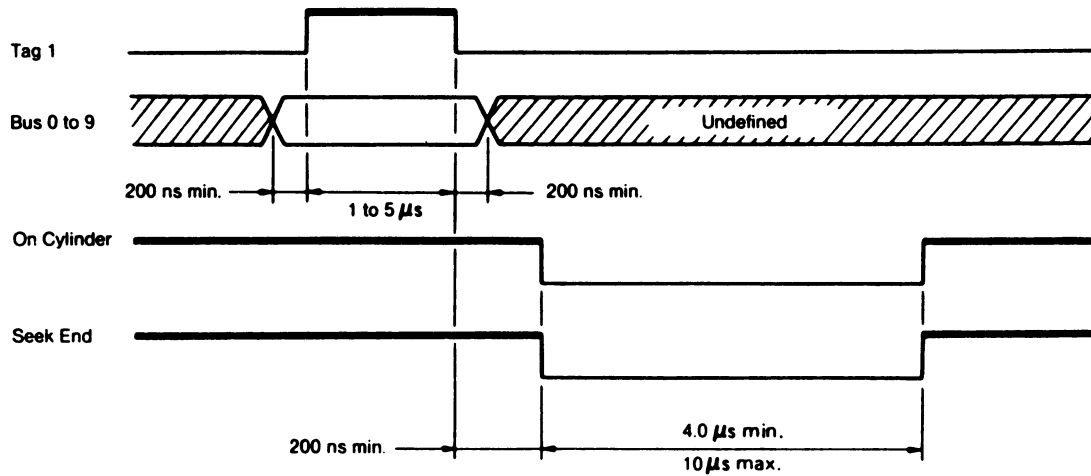


Figure 4.5.8 Zero Track Seek Timing

4.5.5.5 Tag 1 to Tag 2 Timing

Refer to Figure 4.5.10.

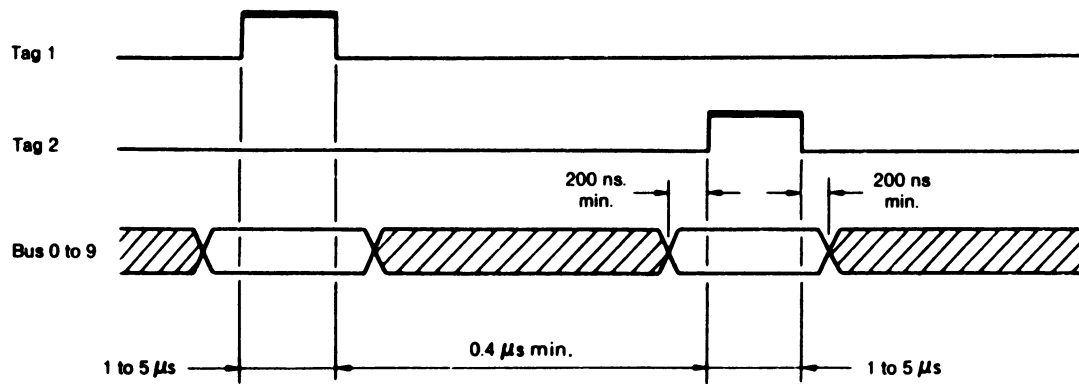


Figure 4.5.9 Tag 1 to Tag 2 Timing

4.5.5.6 Offset Plus/Minus Timing

Refer to Figure 4.5.11.

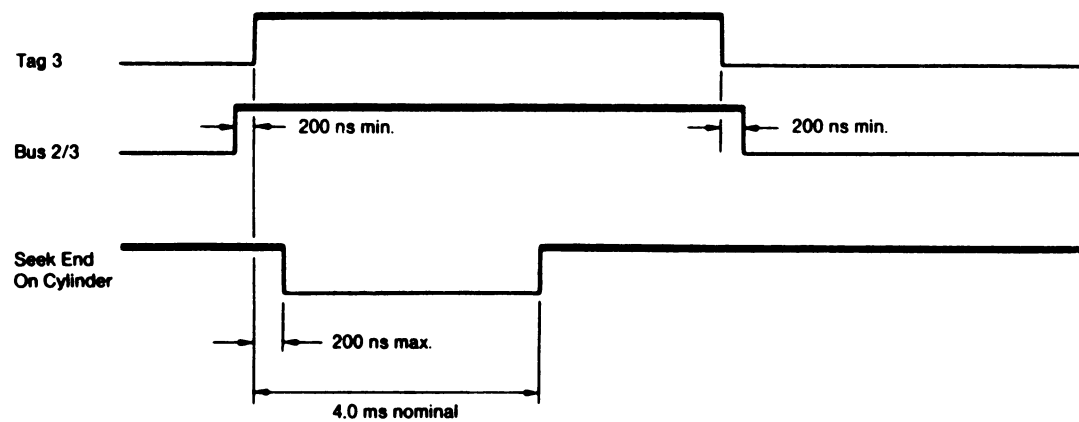


Figure 4.5.10 Offset Plus/Minus Timing

4.5.5.7 Device Check (Fault) Clear Timing

Refer to Figure 4.5.12.

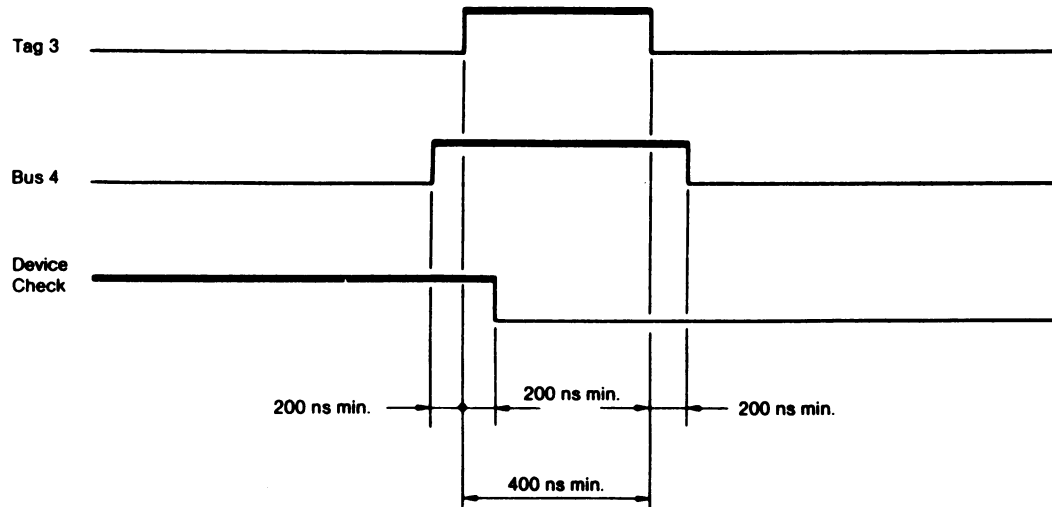
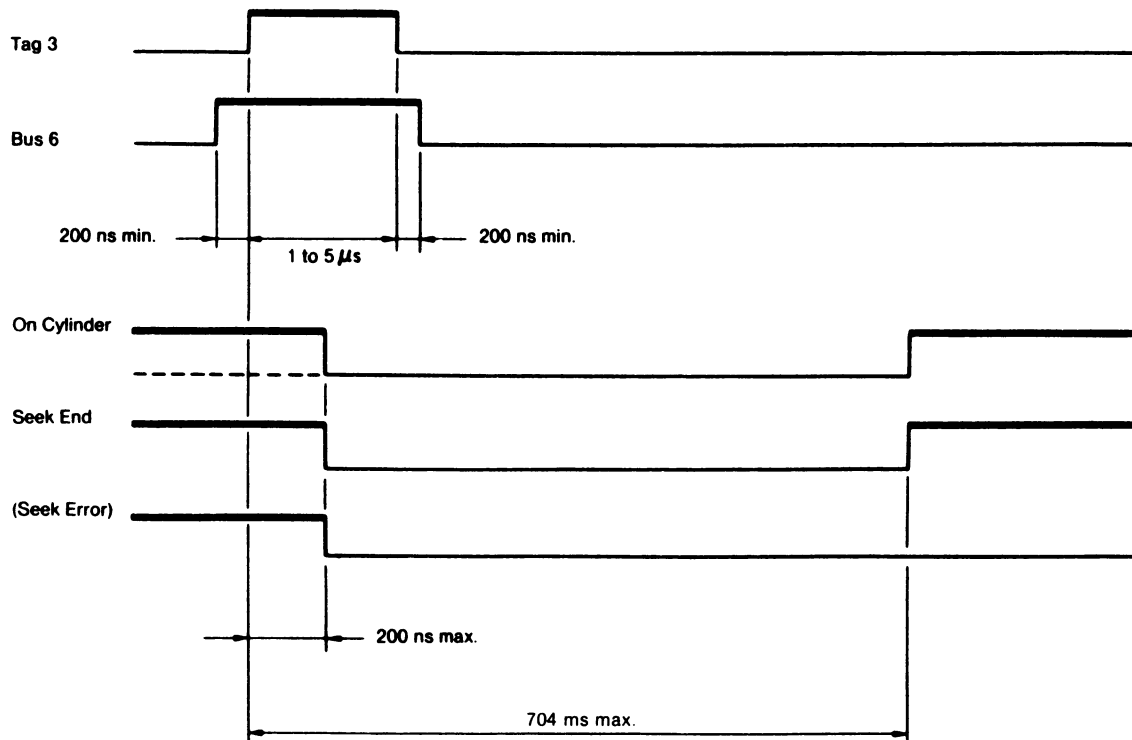


Figure 4.5.11 Fault Clear Timing

4.5.5.8 RTZ Timing

Refer to Figure 4.5.13.



Note: On Cylinder is not always set if a Seek Error occurs.

Figure 4.5.12 RTZ Timing

4.5.5.9 Channel Ready Timing

Refer to Figure 4.5.14.

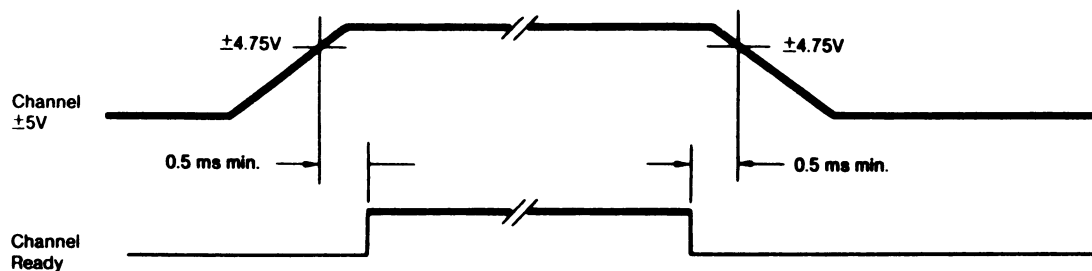


Figure 4.5.13 Channel Ready Timing

4.5.5.10 Tag 4/5 and Status 0 to 7 (optional) Timing

Refer to Figure 4.5.15.

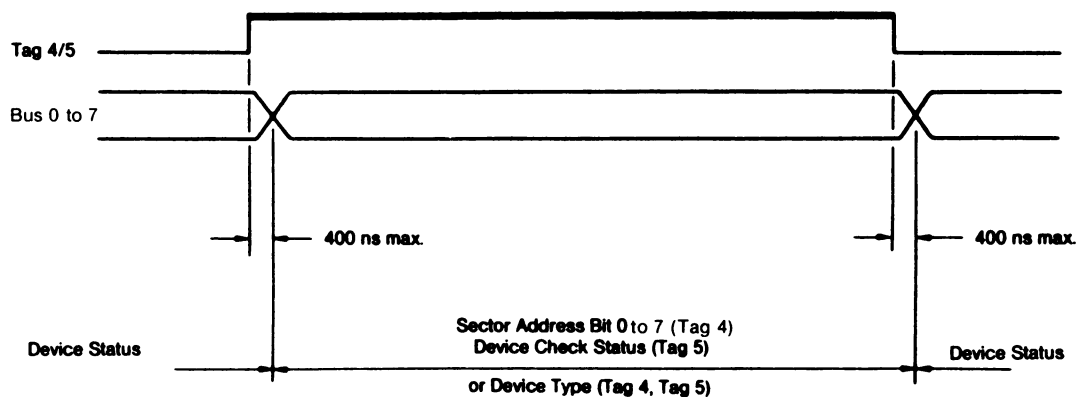


Figure 4.5.14 Tag 4/5 Timing

4.5.5.11 Index/Sector Timing

Refer to Figure 4.5.16.

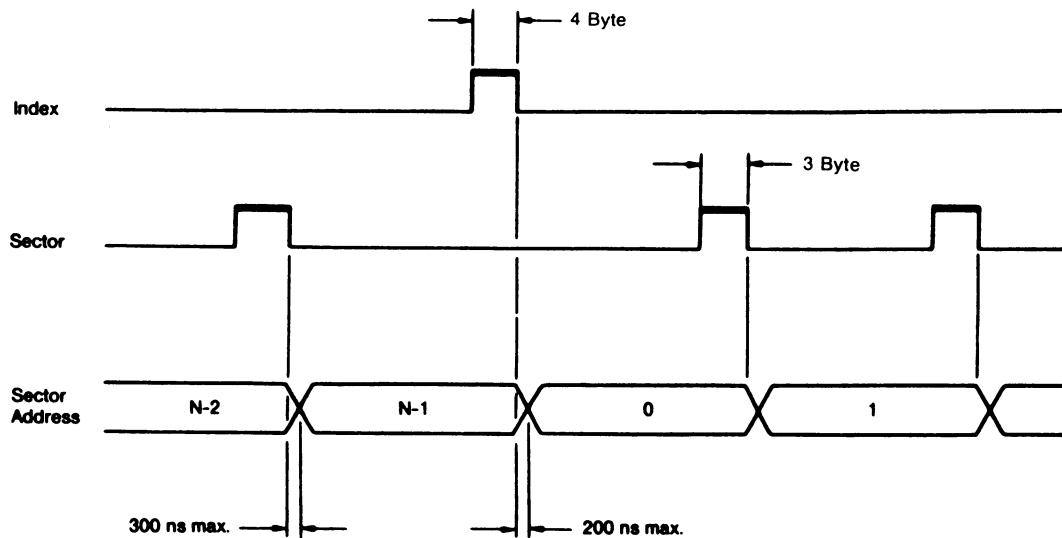
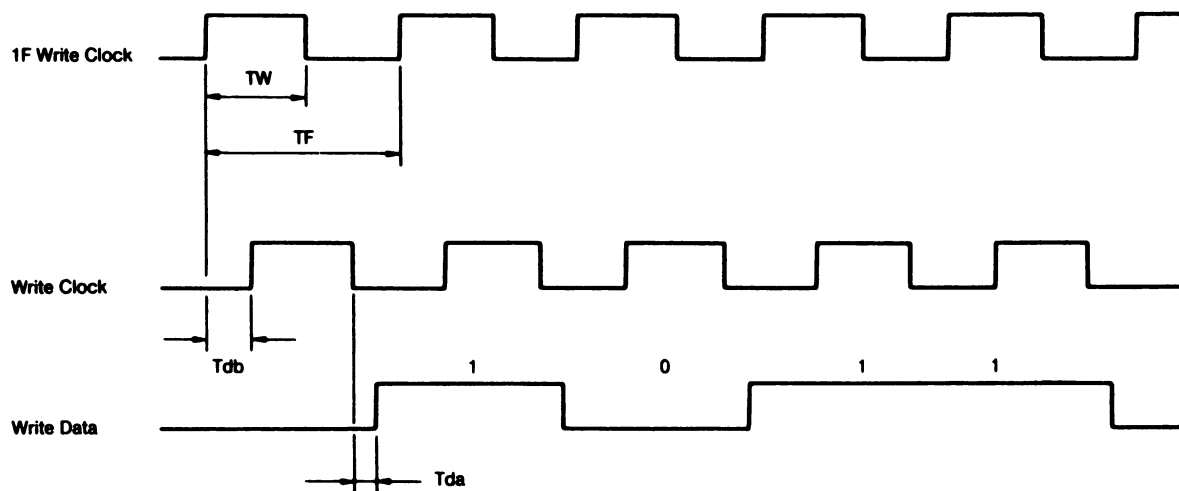


Figure 4.5.15 Index and Sector Timing

4.5.5.12 1F Write Clock, Write Data/Write Clock Timing

Refer to Figure 4.5.17.



$$T_w = T_F/2$$

$$T_F = 67.2 \text{ ns} \pm 3.4 \text{ ns}$$

T_{db} = Continuous delay within 2 bits

$$T_{da} = 0 \pm 15 \text{ ns}$$

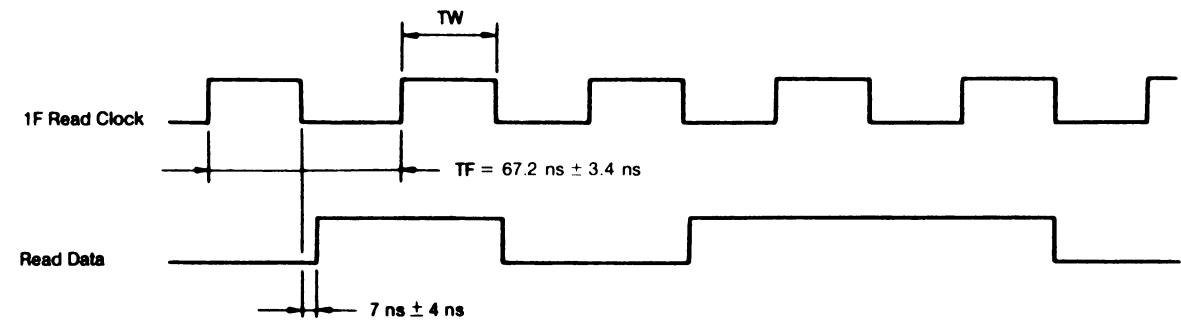
Notes: (1) Write Data and Write Clock timing shall be specified at the output connector of the control unit.

(2) The permissible value of $T_F = 67.2 \text{ ns} \pm 3.4 \text{ ns}$ is about $\pm 5\%$, which includes the rotational speed tolerance, $\pm 4\%$ and the servo jitter, $\pm 1\%$.

(3) NRZ Write Data issued from the control unit is write-compensated and then 2/7-modulated for writing on the disk surface.

Figure 4.5.16 Write Data and Write Clock Timing

4.5.5.13 Read Clock/Read Data Timing
Refer to Figure 4.5.18.



- Notes: (1) 1F Read Clock and Read Data timing shall be specified at the output connector of the disk unit.
(2) Read Data signal should be clocked at the positive-going edge of 1F Read Clock on the control unit.

Figure 4.5.17 1F Read Clock and Read Data Timing

4.5.6 Read/Write Timing

4.5.6.1 Format Write
Refer to Figure 4.5.19.

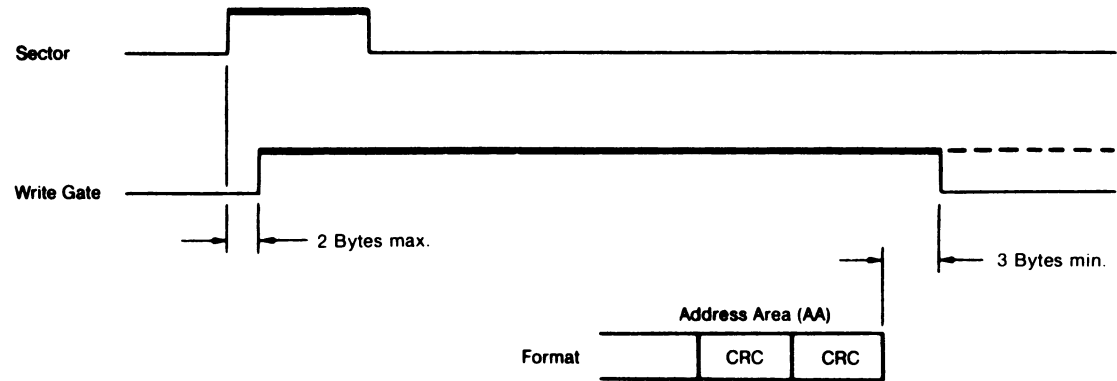


Figure 4.5.18 Format Write Timing

4.5.6.2 Data Write

Refer to Figure 4.5.19.

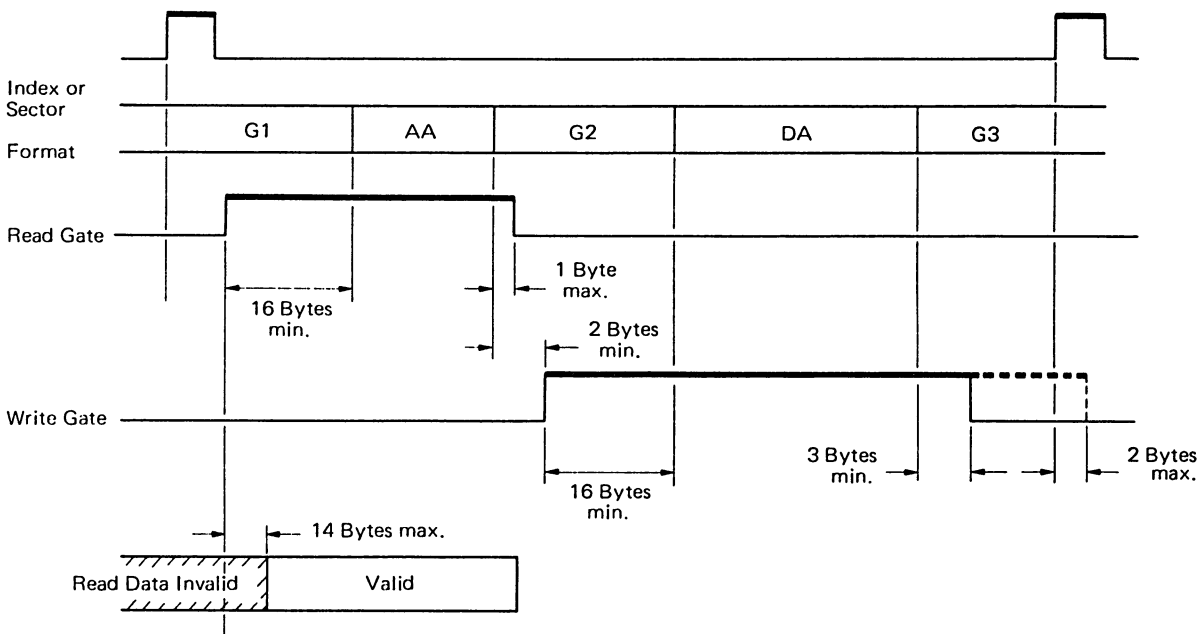
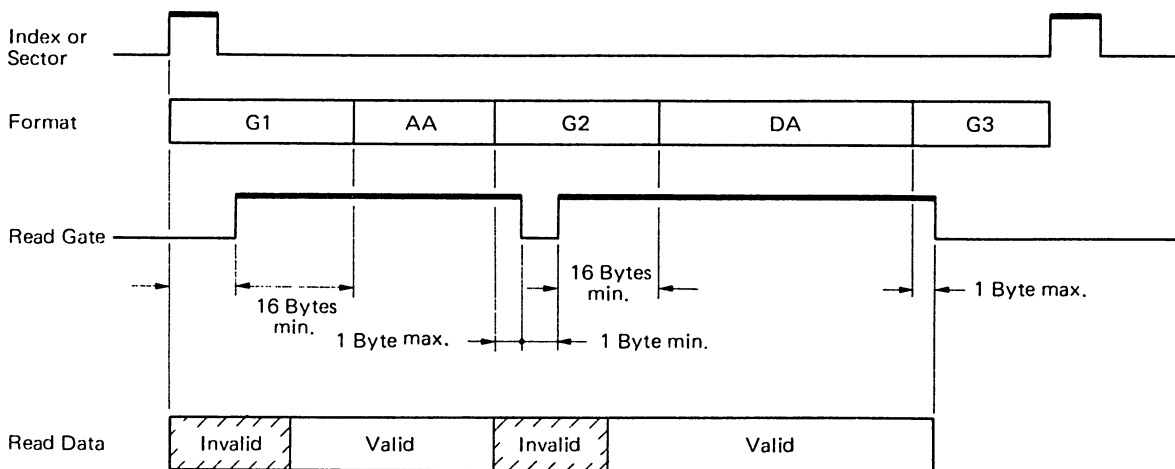


Figure 4.5.19 Write Data Timing

4.5.6.3 Data Read

Refer to Figure 4.5.20.



- Notes: (1) The invalid data in the above figure is inhibited in the unit; therefore, it may be disregarded in the control unit.
 (2) The timing for switching to 1F Read Clock should be performed after the invalid data. In this case, a phase adjustment is required for 1 or 2 bits.

Figure 4.5.20 Read Data Timing

4.5.6.4 Write-To-Read Recovery Time

Refer to Figure 4.5.24. When head selection has been stabilized, the recovery time before Read Gate can be enabled after Write Gate goes false is 10 μ s minimum.

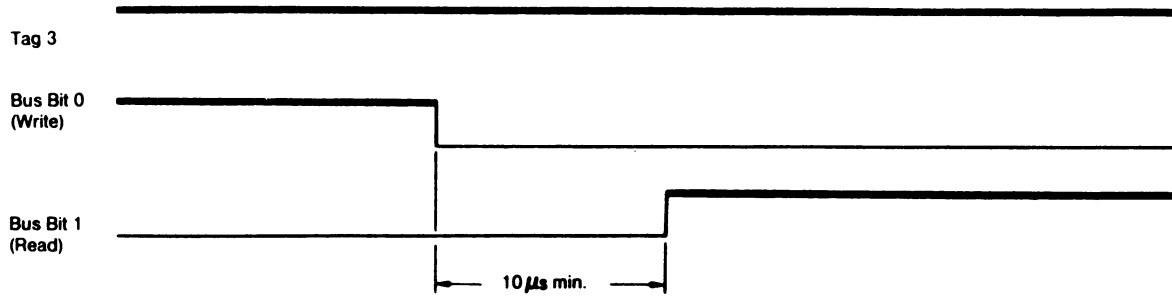


Figure 4.5.21 Write-To-Read Recovery Time

4.5.6.5 Head Select Transient

Refer to Figure 4.5.25. There is a 5 μ s delay within the disk drive due to circuit characteristics between the deselection of one head and the selection of another head.

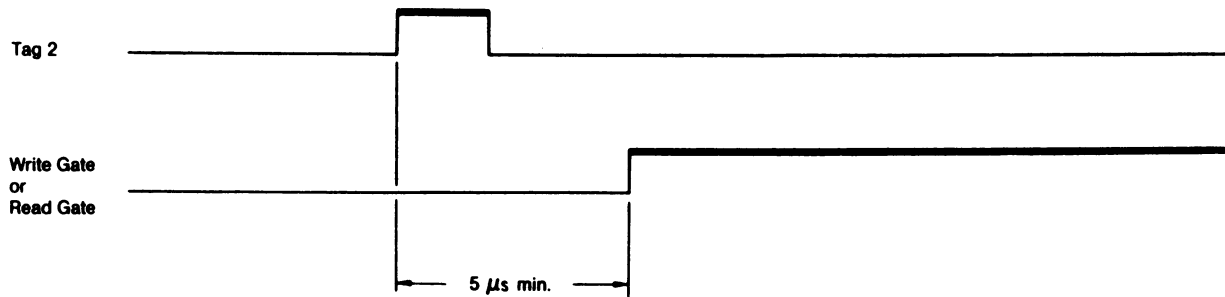


Figure 4.5.22 Head Select Transient

4.5.6.6 1F Write Clock in Reading

In the read operation, the 1F Write Clock signal fluctuates slightly within the Lock-To-Data or Lock-To-PLO signal (internal signal of Variable Frequency Oscillator circuit), as shown in Figure 4.5.26.

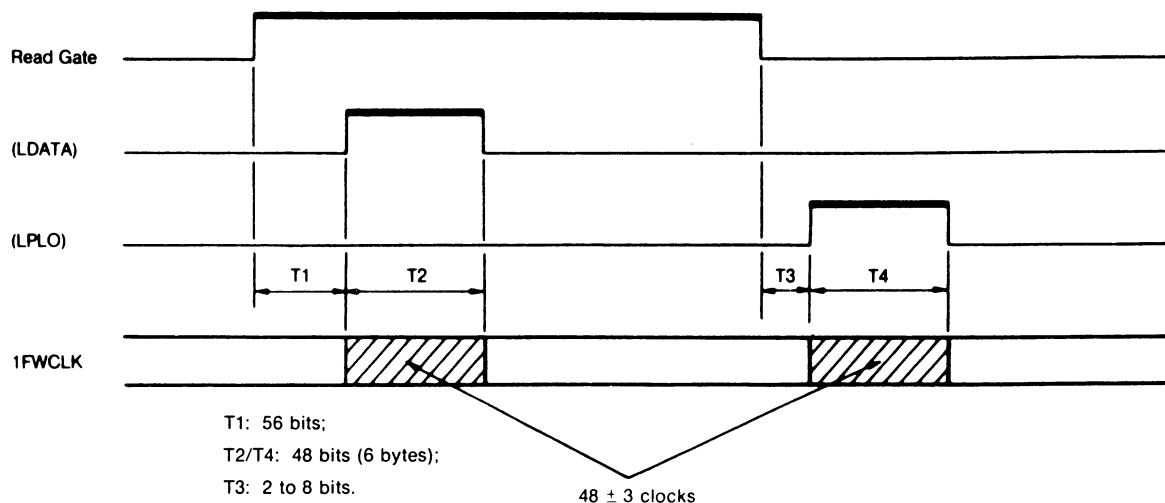


Figure 4.5.23 1F Write Clock in Reading

4.5.6.7 Head Address change at the last gap

This timing is specified for the customer who performs a head address change on the same cylinder in the last gap (Gap 3) of the sector.

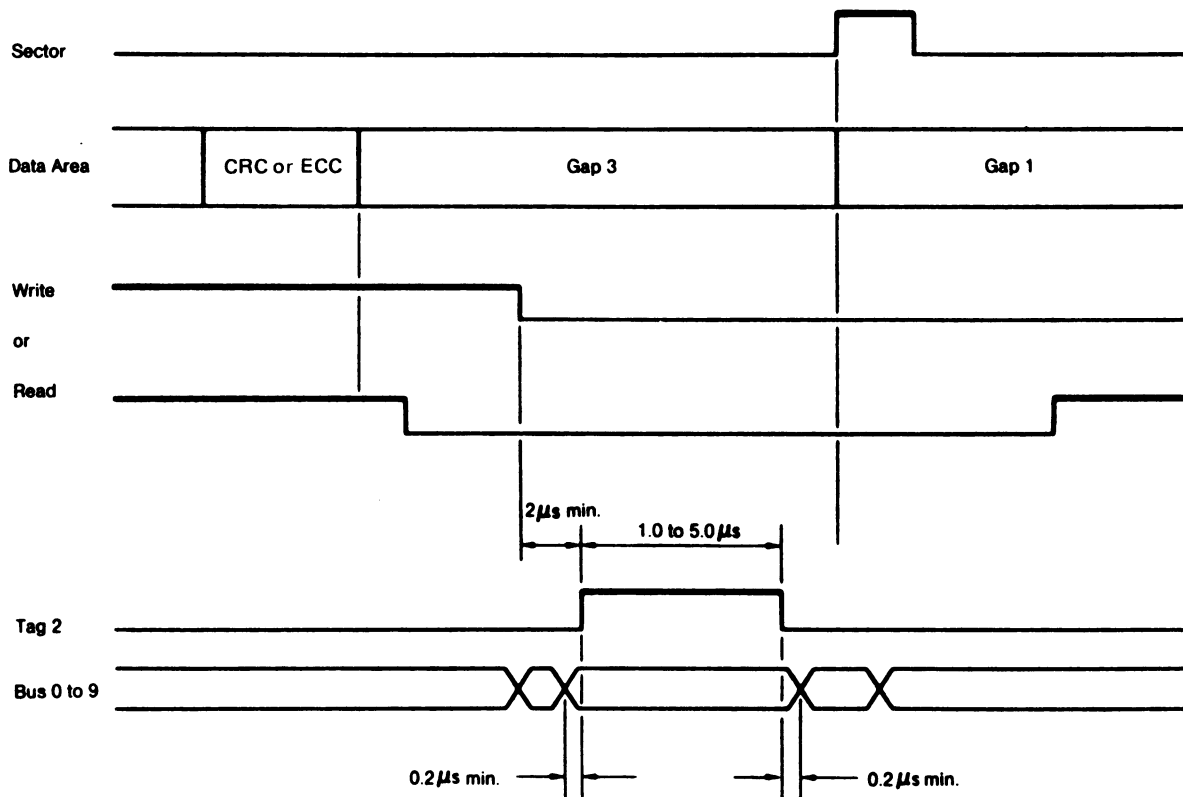


Figure 4.5.24 Head Address Change at the Last Gap

4.5.7 Interface Transmission

4.5.7.1 Driver and Receiver

Transmitters and receivers of SN75110 and SN75107 or equivalent are used to provide a terminated, balanced-line transmission. The Driver is SN75110 or equivalent, and the Receiver is SN75107/SN75108 or equivalent.

(1) Driver

Refer to Figure 4.5.28 and Table 4.5.4.

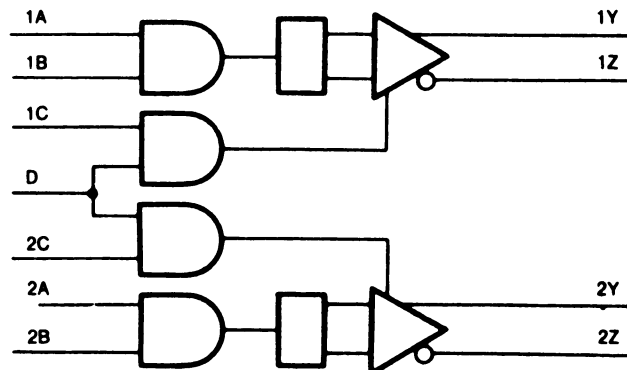


Figure 4.5.25 Drive Logic Diagram (SN75110)

Table 4.5.4 SN75110 Function Table

Logic Inputs		Inhibit Input		Outputs	
A	B	C	D	Y	Z
X	X	L	X	OFF	OFF
X	X	X	L	OFF	OFF
L	X	H	H	ON	OFF
X	L	H	H	ON	OFF
H	H	H	H	OFF	ON

Note: H-High Level, L-Low Level, X-Irrelevant.

- (2) Receiver
Refer to Figure 4.5.29 and Table 4.5.5.

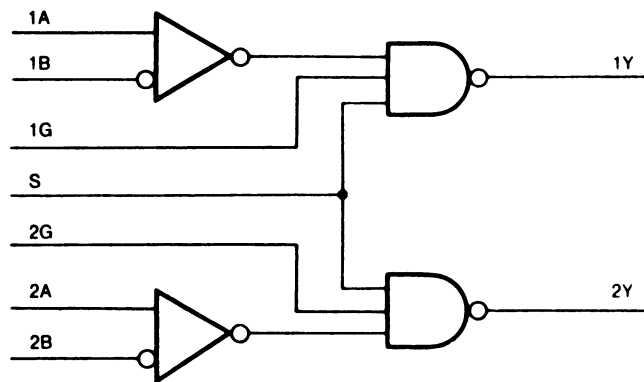


Figure 4.5.26 Receiver Logic Diagram (SN75107/75108)

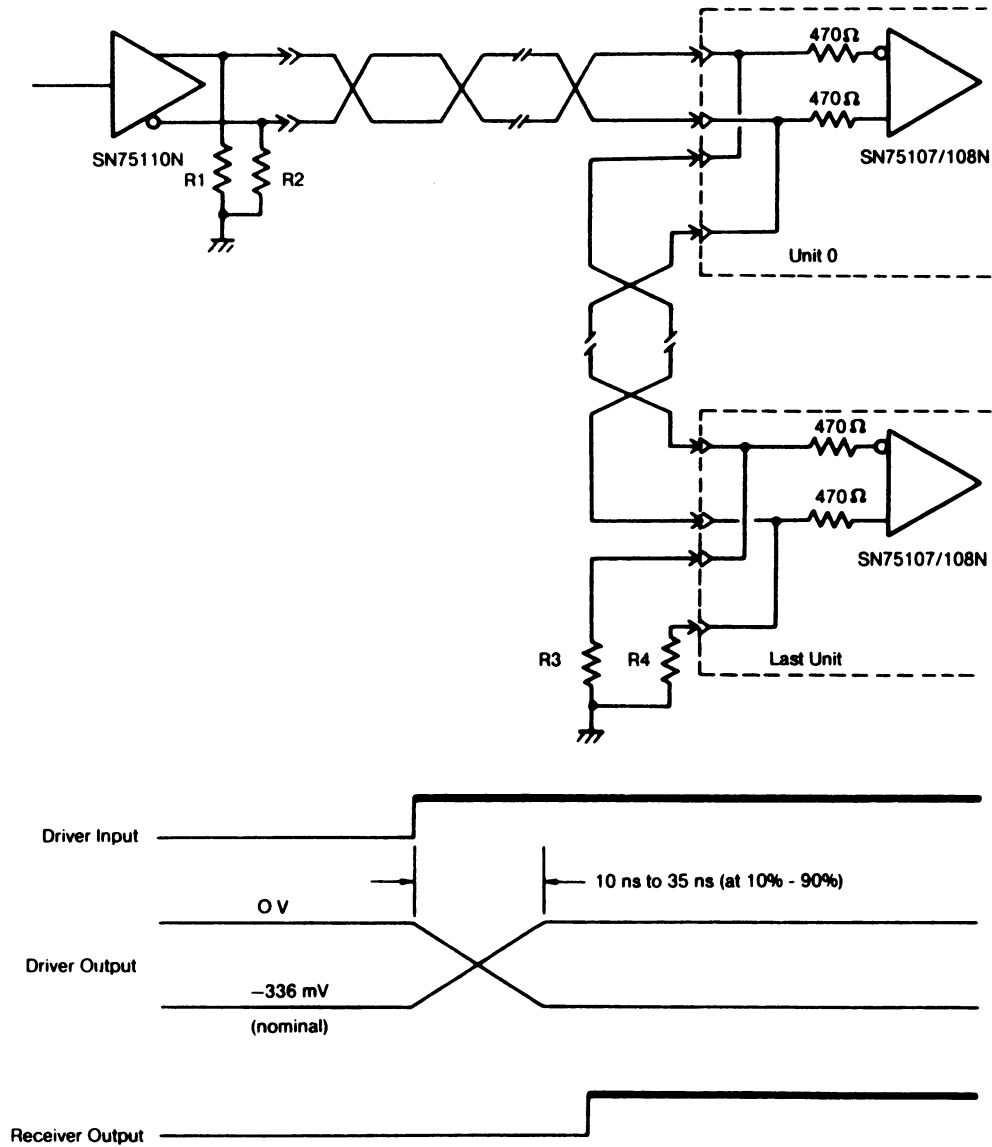
Table 4.5.5 SN75107/75108 Function Table

Differential Inputs	Strobes		Output Y
	G	S	
$A-B \geq 25 \text{ mV}$	X	X	H
$-25 \text{ mV} < A-B < 25 \text{ mV}$	X	L	H
	L	X	H
	H	H	Indeterminate
$A-B \leq -25 \text{ mV}$	X	L	H
	L	X	H
	H	H	L

Note: H-High Level; L-Low Level; X-Irrelevant.

4.5.7.2 "A" Cable (Control Cable) Transmission

Refer to Figure 4.5.30.

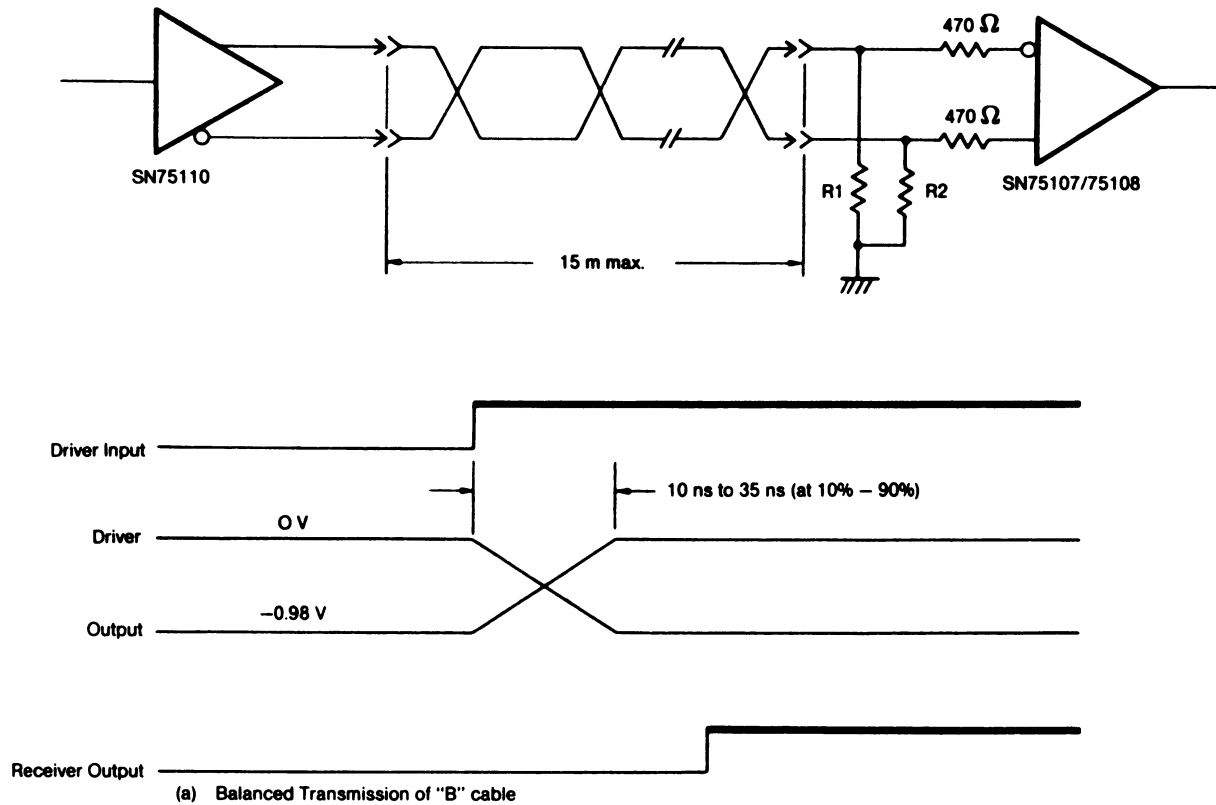


- Notes: (1) Line terminators are located on the unit and the controller. R1 to R4: $56\ \Omega \pm 5\%$, 1/10W.
- (2) A line terminator is located on the terminator assembly of the last unit in the daisy chain configuration.
- (3) The maximum cable length is 30 meters.

Figure 4.5.27 Balanced Transmission of "A" Cable

4.5.7.3 "B" Cable (Data Cable) Transmission

Refer to Figure 4.5.31.



- Notes:
- (1) Cable shall be flat with characteristic impedance of 100 ± 10 ohms.
 - (2) Line terminators are located on the receivers at the drive or control unit. R1 and R2 are $82 \text{ ohms} \pm 5\%$, 1/10W.
 - (3) The protect resistors (470 ohms) should be located on the receiver side. $470 \Omega \pm 5\%$, 1/10W.
 - (4) A bias network should be used to prevent disturbance conditions by power failure at the control unit end of Unit Selected and Seek End signals as in (b).

Figure 4.5.28 Balanced Transmission "B" Cable

4.5.7.4 Channel Ready Driver

The Channel Ready signal must be issued so that data is protected during a power failure of the control unit. Relay logic and passive terminations sometimes aid this requirement. If SN75110A drivers are used to drive the Channel Ready signal from the control unit, dual drivers should be connected in parallel, and no 56 ohm termination to ground should be used at the control unit.

4.5.8 Connector and Cable

4.5.8.1 Connector

- (1) A – Cable connector 60 pos.

	<u>Ansley</u>	<u>Fujitsu</u>
Unit Side:	609-6052MR	FCN-702P060-AU/M (Wire wrapping)
	—	FCN-704P060-AU/M (Straight)
	—	FCN-705P060-AU/M (Right Angle)
Cable Side:	609-6001M	FCN-707J060-AU/B

- (2) B – Cable Connector 26 pos.

	<u>Ansley</u>	<u>Fujitsu</u>
Unit Side:	609-2652MR	FCN-702P026-AU/M (Wire wrapping)
	—	FCN-704P026-AU/M (Straight)
	—	FCN-705P026-AU/M (Right Angle)
Cable Side:	609-2601M	FCN-707J026-AU/B

4.5.8.2 Cable

- (1) A – Cable
SS-455-248-60 SPECTRA STRIP
 $ZO = 100 \Omega \pm 10 \Omega$, 28 AWG, 7 strands
- (2) B – Cable
174-26 Ansley, 3476-26 3M
 $ZP = 100 \Omega \pm 15 \Omega$, 28 AWG, 7 strands

4.5.9 Connector Pin Assignment

4.5.9.1 A – Cable Connector 60 Pin

Table 4.5.6 A – Cable Pin Assignment

1	Tag 1 L	31	Tag 1 H
2	Tag 2 L	32	Tag 2 H
3	Tag 3 L	33	Tag 3 H
4	Bus 0 L	34	Bus 0 H
5	Bus 1 L	35	Bus 1 H
6	Bus 2 L	36	Bus 2 H
7	Bus 3 L	37	Bus 3 H
8	Bus 4 L	38	Bus 4 H
9	Bus 5 L	39	Bus 5 H
10	Bus 6 L	40	Bus 6 H
11	Bus 7 L	41	Bus 7 H
12	Bus 8 L	42	Bus 8 H
13	Bus 9 L	43	Bus 9 H
14	Channel 1 Ready L	44	Channel Ready H
15	Status 3 L	45	Status 3 H
16	Status 2 L	46	Status 2 H
17	Status 1 L	47	Status 1 H
18	Status 6L	48	Status 6H
19	Status 0 L	49	Status 0 H
20	Status 5 L	50	Status 5 H
21	Busy L	51	Busy H
22	Unit Select Tag L	52	Unit Select Tag H
23	Unit Select 1 L	53	Unit Select 1 H
24	Unit Select 2 L	54	Unit Select 2 H
25	Status 7L	55	Status 7H
26	Unit Select 4 L	56	Unit Select 4 H
27	Tag 5 L (Selectable)	57	Tag 5 H (Selectable)
28	Status 4 L	58	Status 4 H
29	(Pick)	59	(Hold)
30	Tag 4 L (Selectable)	60	Tag 4 H (Selectable)

4.5.9.2 B – Cable Connector 26 Pin

Table 4.5.7 B – Cable Pin Assignment

1	GND	14	1F Write Clock H
2	1F Write Clock L	15	GND
3	Read Data L	16	Read Data H
4	GND	17	1F Read Clock H
5	1F Read Clock L	18	GND
6	Write Clock L	19	Write Clock H
7	GND	20	Write Data H
8	Write Data L	21	GND
9	Unit Selected H	22	Unit Selected L
10	Seek End L	23	Seek End H
11	GND	24	Index H
12	Index L	25	GND
13	Sector L	26	Sector H

4.6 ELECTRIC CIRCUIT FUNCTION

4.6.1 Start/Stop Function

When power, AC input, DC + 5V, DC \pm 12V and DC + 24V, is applied to the FDU from the external power supply unit, the cooling blower is activated. In the case of Remote mode, the AC input to the spindle drive motor and DC + 24V is controlled by Pick and Hold signals from the control unit. DC + 24V is supplied to the brake coil of the spindle drive motor assembly and releases the spindle drive motor shaft lock.

When current flows through the brake coil and is detected by the Brake Current Detection circuit, its output activates the relay circuit. Then AC input is supplied to the spindle drive motor through the relay contacts.

The spindle drive motor provides rotating motion to the spindle of the Disk Enclosure through a flat belt. When the disk rotates, a tab on the spindle assembly is detected by the speed transducer, which generates pulses that are used to determine the rotational speed. The output pulse, Speed Signal (SPSG) is applied to Speed Detection circuit. When the rotational speed comes up to 80% of operating speed, Speed OK (SPOK) signal is issued and triggers the start time circuit, and also is sent to the external power supply unit through the power control connector PWC1.

Through this step of power-up sequencing, the actuator is held in the Landing Zone (IGB2) by a stopper magnet. When the Speed OK signal goes true, current flows through the coil of the Voice Coil Motor (VCM) on the actuator and the heads are kept in the Landing Zone electrically.

Five seconds after SPOK goes true, Guard Band Enable is activated. Ten seconds after SPOK, Start Pulse (STARTP) goes true. The Guard Band Enable signal allows detection of Guard Band signals, and Start Pulse activates the Initial Seek operation.

The stop sequence is initiated when input power is shut-off. The FDU does not require DC power sequencing, therefore, the stop sequence is initiated in various ways.

If DC + 24V drops below + 10V, the VCM Driver circuit is turned off and the actuator returns to the Landing Zone driven by the Retract Capacitor discharge. If there is a further reduction of DC + 24V, the spindle motor brake is activated and the drive motor stops. If DC + 5V or DC \pm 12V goes false, the same sequence occurs.

Also, if DC + 5V or DC \pm 12V goes false, Power Ready (PWRDY) goes false.

If PWRDY signal is disabled, the actuator returns to the Landing Zone and Unit Ready (URDY) signal goes false.

With the loss of AC input, the rotational speed will decrease slowly and then Speed OK signal will go false to retract the heads to the Landing Zone.

The Start/Stop block diagram is shown in Figure 4.6.1, timing chart in Figure 4.6.2, start sequence flow chart in Figure 4.6.3, and stop sequence flow chart in Figure 4.6.4

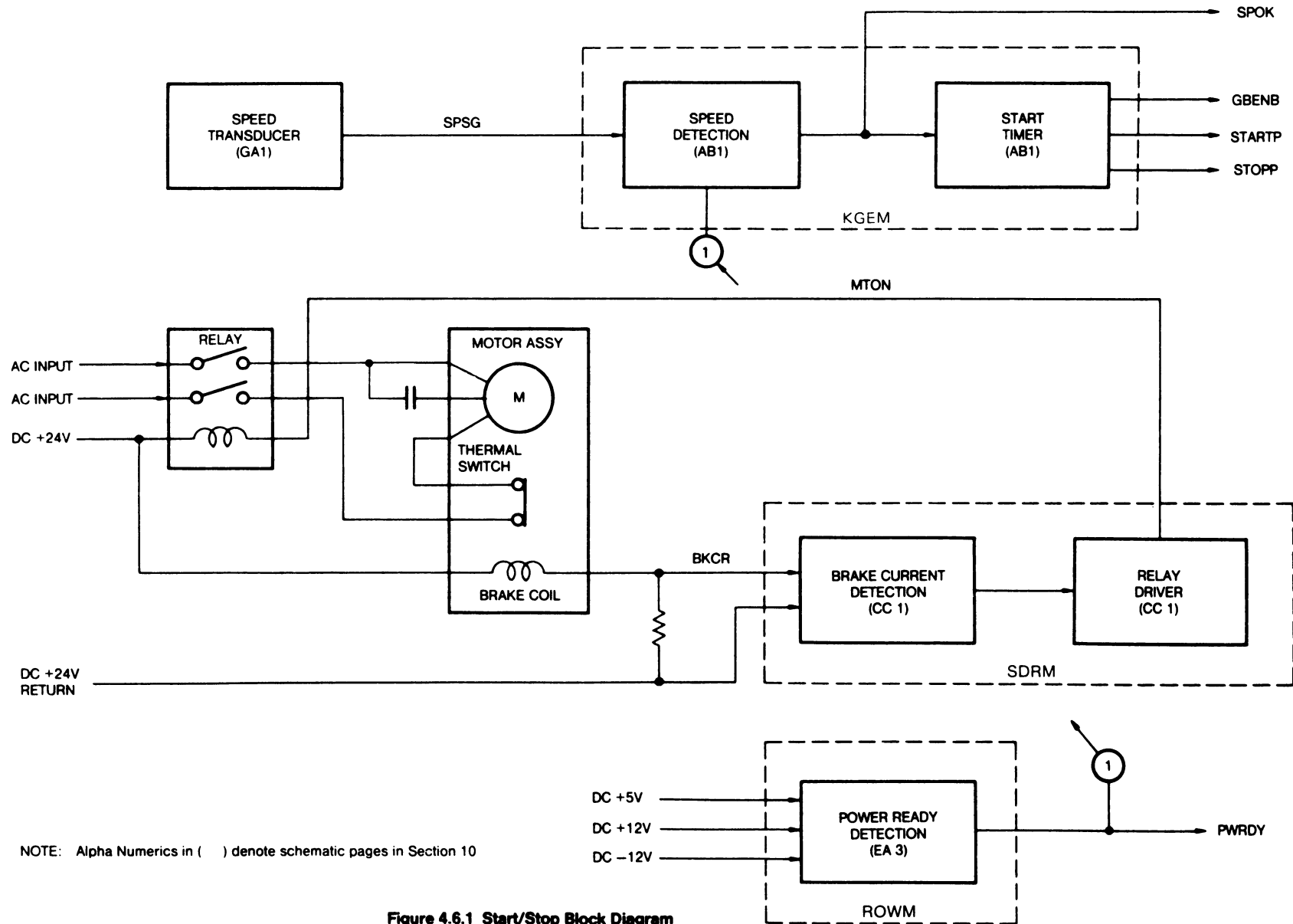


Figure 4.6.1 Start/Stop Block Diagram

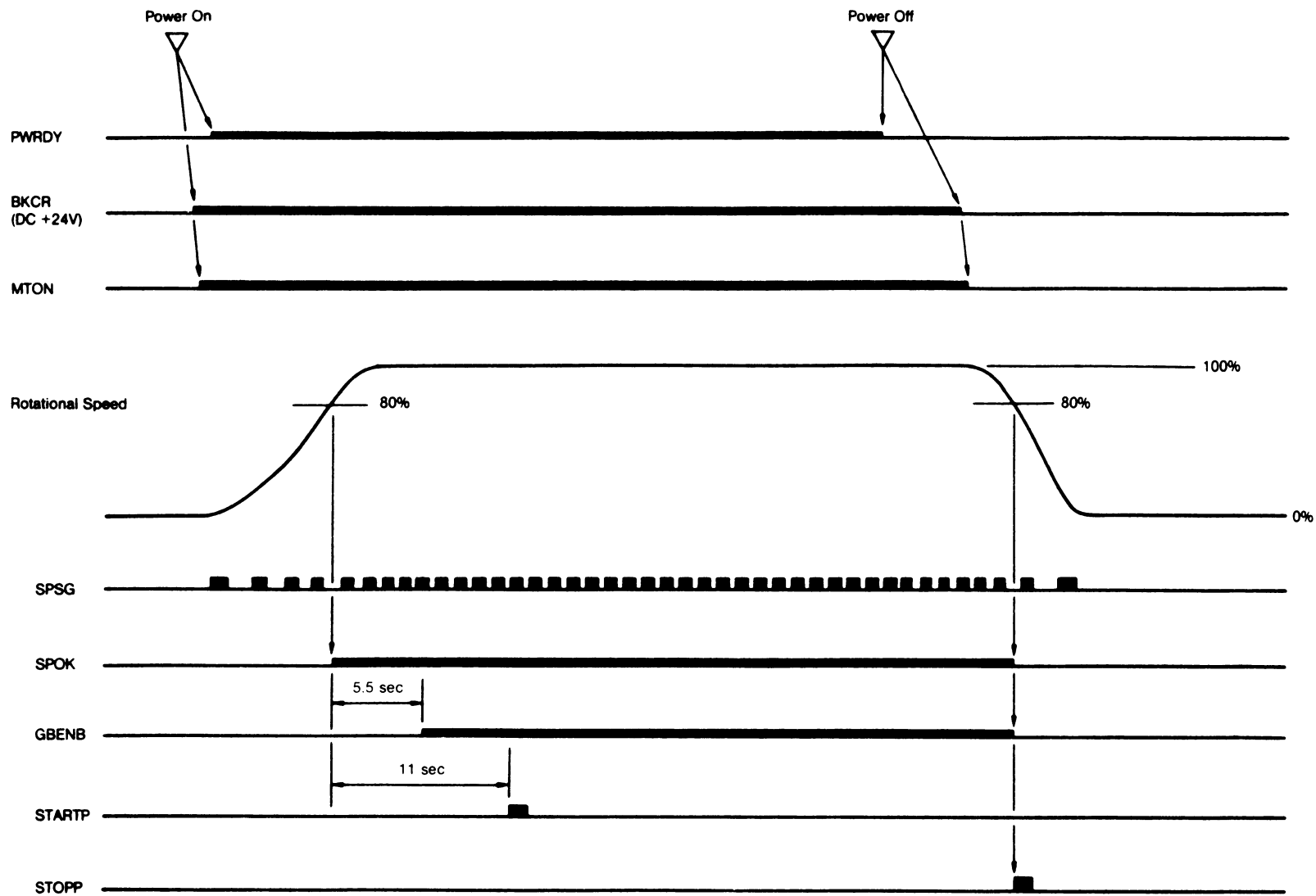


Figure 4.6.2 Start/Stop Timing Chart

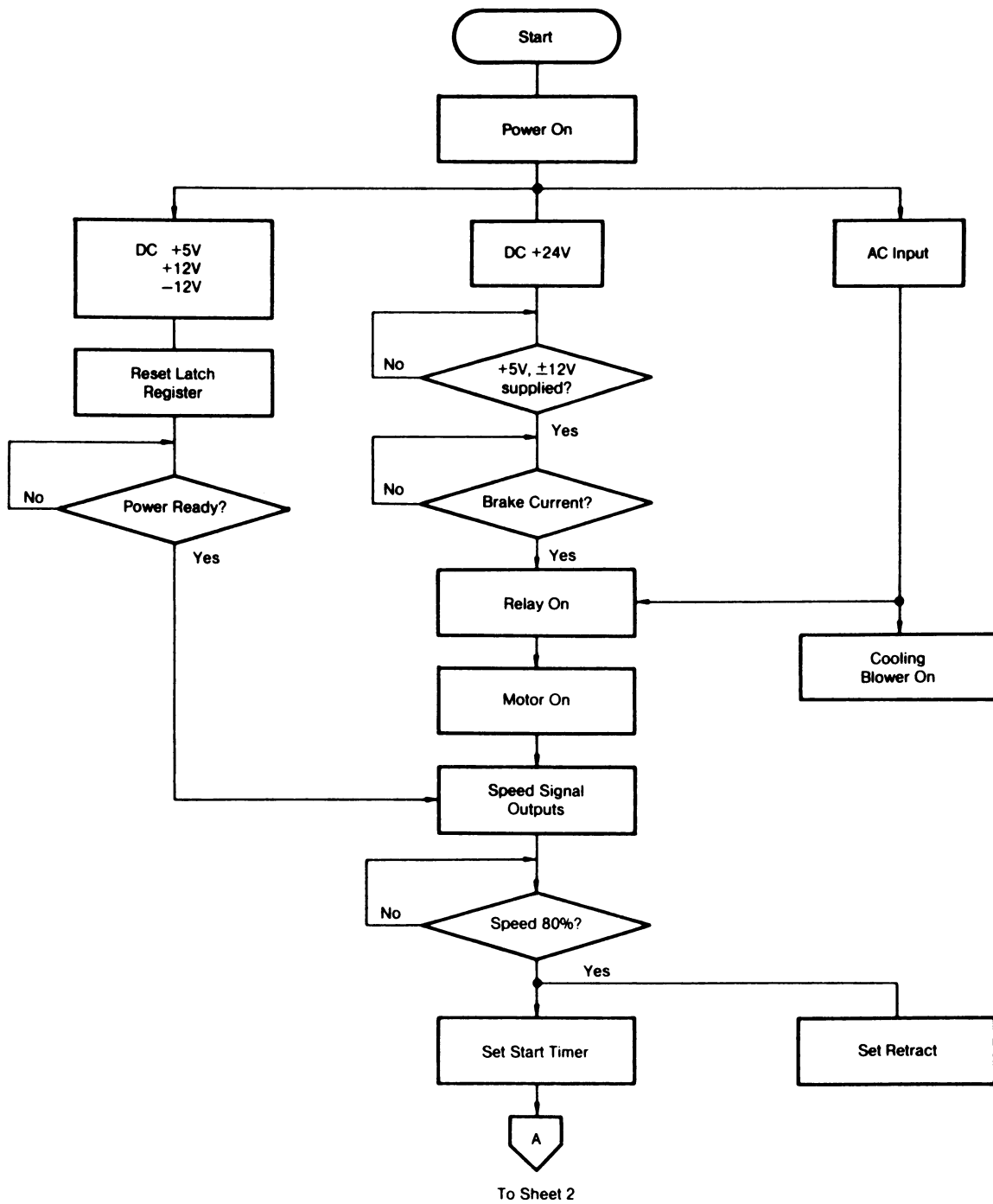


Figure 4.6.3 Start Sequence Flow Chart (Sheet 1 of 2)

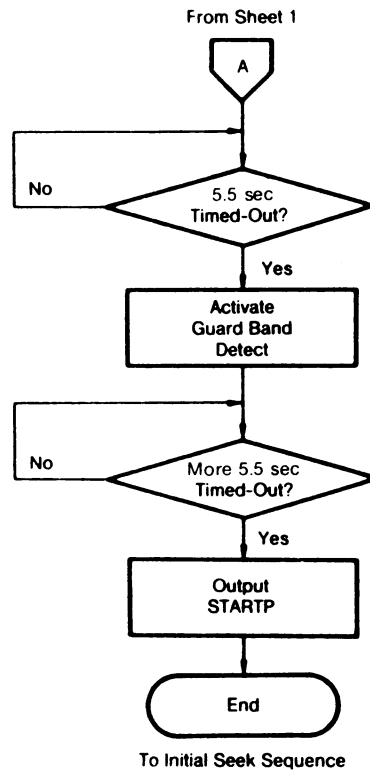


Figure 4.6.3 Start Sequence Flow Chart (Sheet 2 of 2)

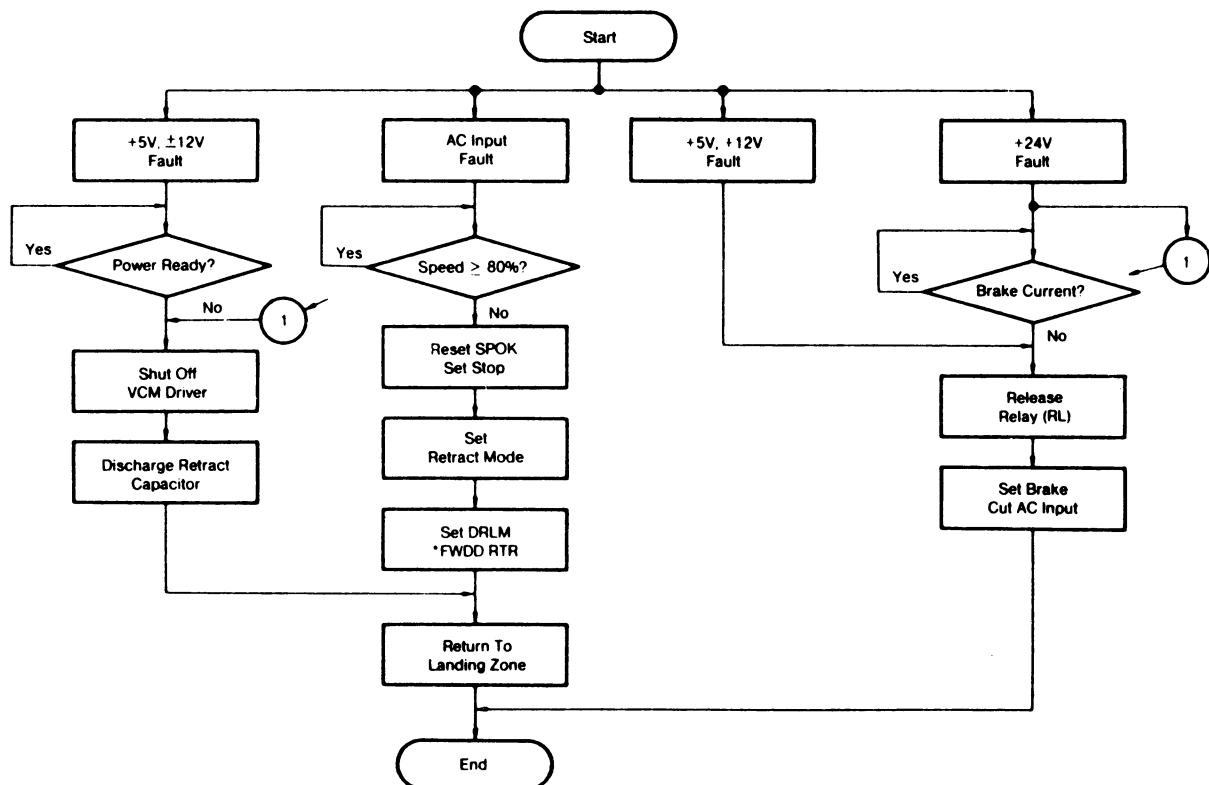


Figure 4.6.4 Stop Sequence Flow Chart

4.6.2 Unit Selection

The FDU must be selected before it will respond to any commands from the control unit. Tag and Bus receivers are not enabled until the unit is selected.

This describes the dual port functions related to selection. They are as follows:

- Unit address select
- Reserve
- Release
- Priority select (unconditional reserve)
- Disable with a maintenance switch

The functional block diagram of dual port is shown in Figure 4.6.5.

4.6.2.1 Unit Address Select and Reserve

A unit is selected or reserved in an identical sequence which is initiated by Unit Select Tag (USLTG) and a unit address signal (Unit select 1, 2, 4: USL 1, 2, 4). However, this sequence cannot start when:

- The unit is selected and reserved by the opposite channel.
- The unit is not selected, but reserved by the opposite channel.
- The channel which has attempted to select the unit is disabled by the maintenance switch on the unit or because the unit is placed in the Priority Select state by the opposite channel.

The select/reserve sequence is as follows:

Suppose that the unit is ready to be selected that is, none of the above three condition exist. A controller sends USLTG and USL 1, 2, 4 to the unit. If the unit address from the channel-A controller agrees with the logical unit number (LUN), the unit sends Unit Selected to the channel-A controller through cable B when Channel-A Compare (CHACMP) is sent to the XCBM printed circuit board. This sequence is the same as with the single-port configuration.

Unless the unit is selected or reserved by channel-B and, as a result, is Busy, CHACMP causes the Channel A Selected signal (CHASLD) to be sent in synchronization with Clock 1 (CLK1) from the oscillator. CHASLD turns on the Channel-A Enable (CHAENB) signal to make the driver/receiver for Channel-A ready for transmission/reception, drive the LED to indicate CHASLD, switch the WDAT/WCLK multiplexer to Channel-A, set Busy to indicate that the unit is selected or reserved by the Channel-A controller, and trigger the Set Reserve (STRSV) one-shot multivibrator to set the reserve latch.

If channels-A and B attempt to select a unit at the same time, CLK1 and CLK2 (clocks with the same frequency and different phases) determine which channel is to access the unit. As a result, Busy is set.

The STRSV one-shot multivibrator output sets the Channel A Reserved (CHARSV) latch about 300 ns after CHASLD. This CHARSV signal turns on the LED on the XCBM printed circuit board, sets BUSY A, and sets Seek End B (SKENDB) to "1" before its transmission to Channel-B. SKEND to Channel-B is kept "1" as long as the unit is reserved by Channel-A.

The unit is kept selected/reserved by Channel-A until Channel-A is disabled by the maintenance switch or until USLTG becomes false. When Channel-B attempts to select the unit, the unit sends BUSY A as a busy signal to Channel-B, and sends also Unit Selected B (USLDB) to indicate that it is selected/reserved by Channel-A.

Even when USLTG from Channel-A goes false after the select/reserve sequence, the unit remains reserved by Channel-A. This reserved state is not reset until a Release command comes from Channel-A, Channel-A is disabled by the maintenance switch, Channel-B performs Priority Select, or the power is turned on/off.

If the opposite channel control unit attempts to select the drive while it is selected or reserved by the other channel control unit (i.e. in Busy state), Tried Latch in the dual port is set. Thus, at the time when the drive becomes neither selected nor reserved, Seek End goes false for 30us so that the opposite channel, having waited, can interrupt.

If the unit is in the Disabled state (due to Priority Select from the opposite channel or by the Disable switch) and the opposite channel attempts to select the unit, no signal response is activated.

The block diagram of the select/reserve circuit is shown in Figure 4.6.6, and the related flowchart and timing chart are shown in Figures 4.6.7 and 4.6.8, respectively.

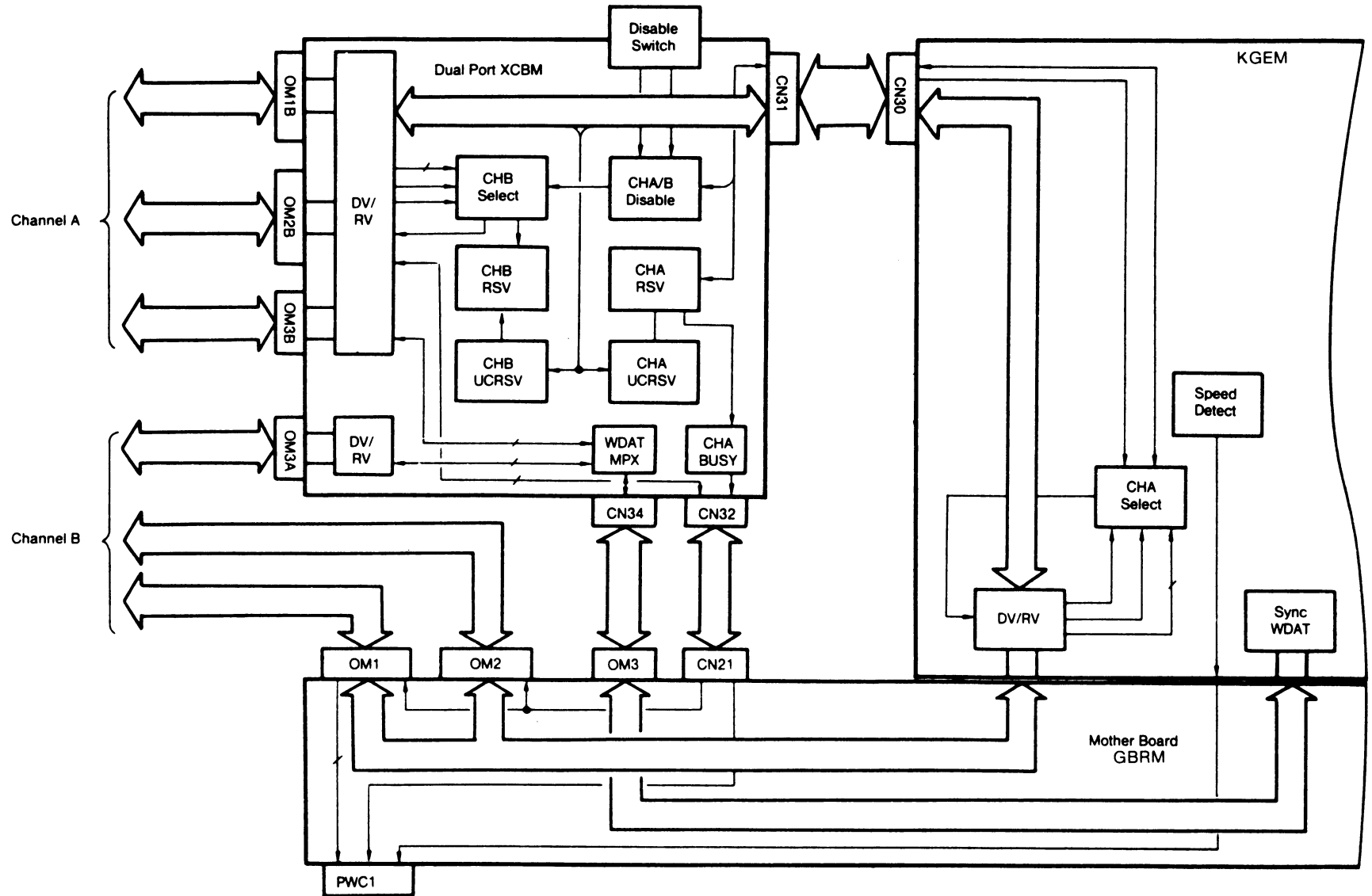


Figure 4.6.5 Functional Block Diagram of Dual Port

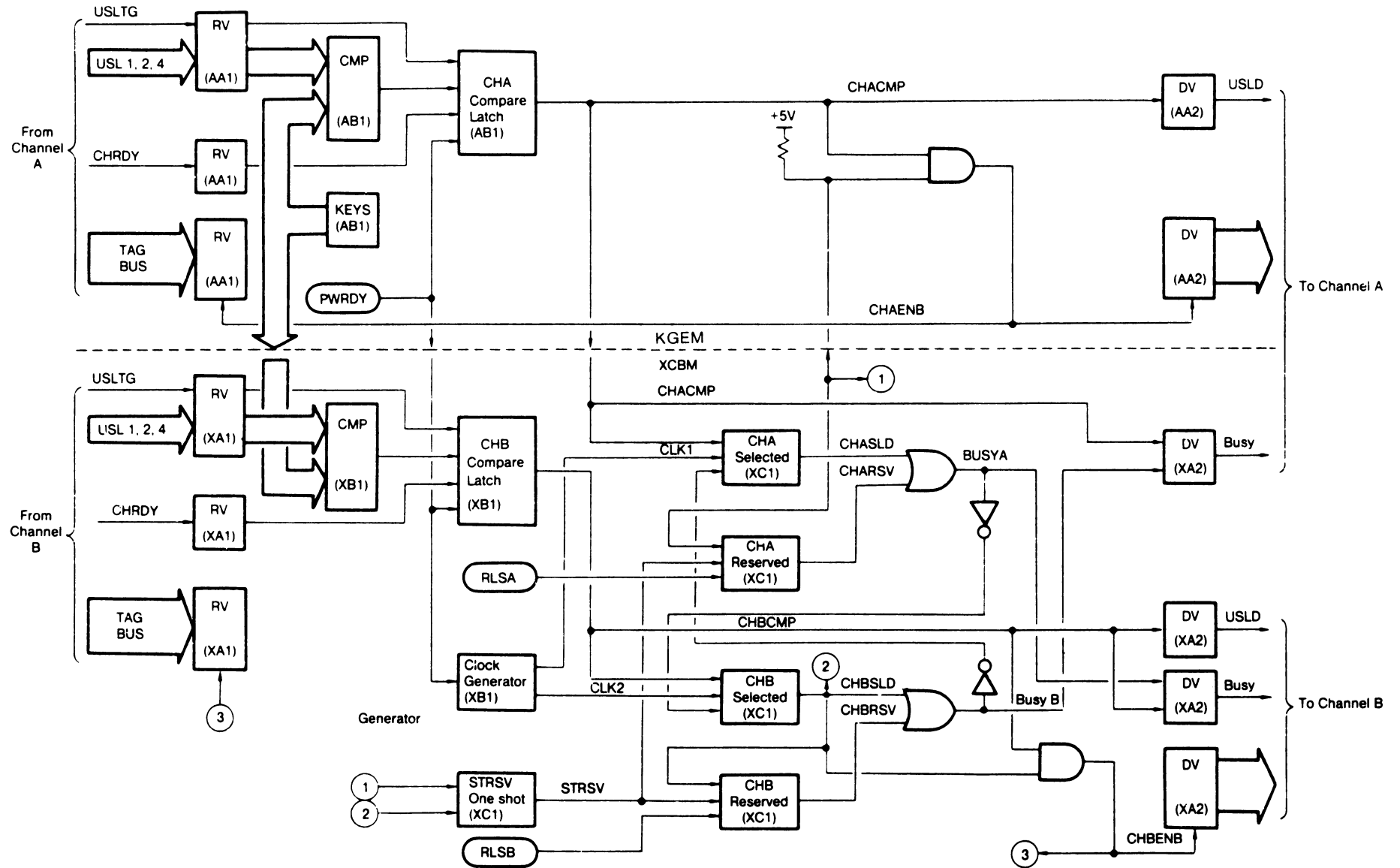


Figure 4.6.6 Functional Block Diagram of Select/Reserve

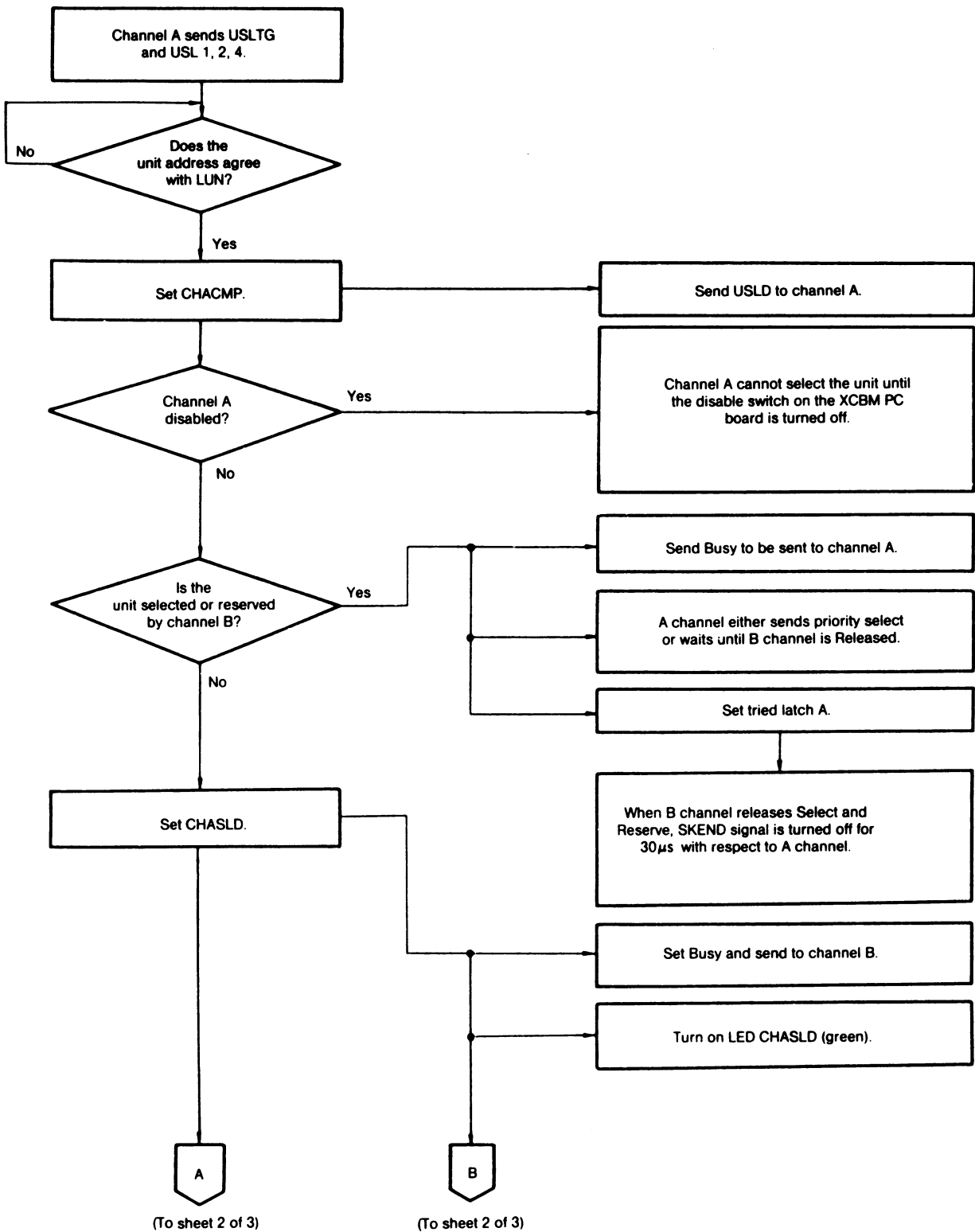


Figure 4.6.7 Select/Reserve Flow Chart (Sheet 1 of 3)

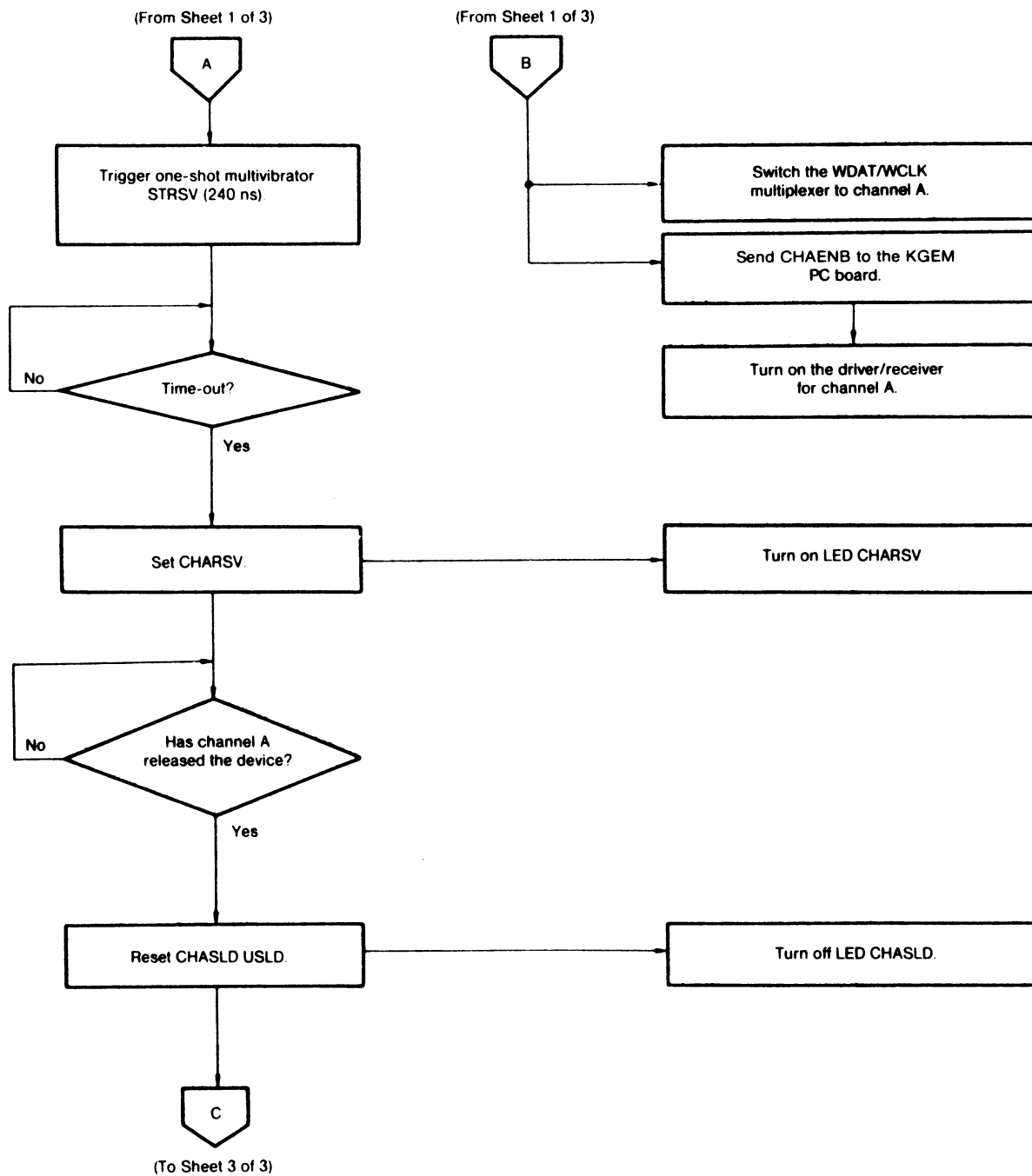


Figure 4.6.7 Select/Reserve Flowchart (Sheet 2 of 3)

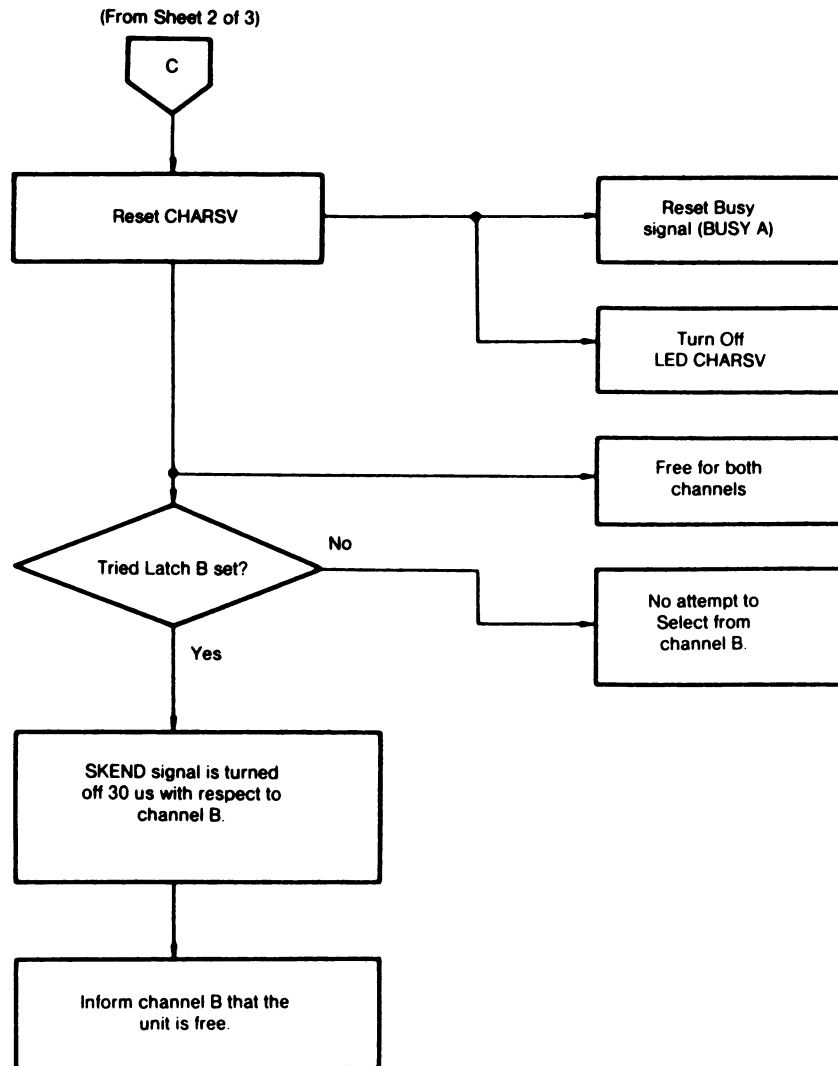


Figure 4.6.7 Select/Reserve Flowchart (Sheet 3 of 3)

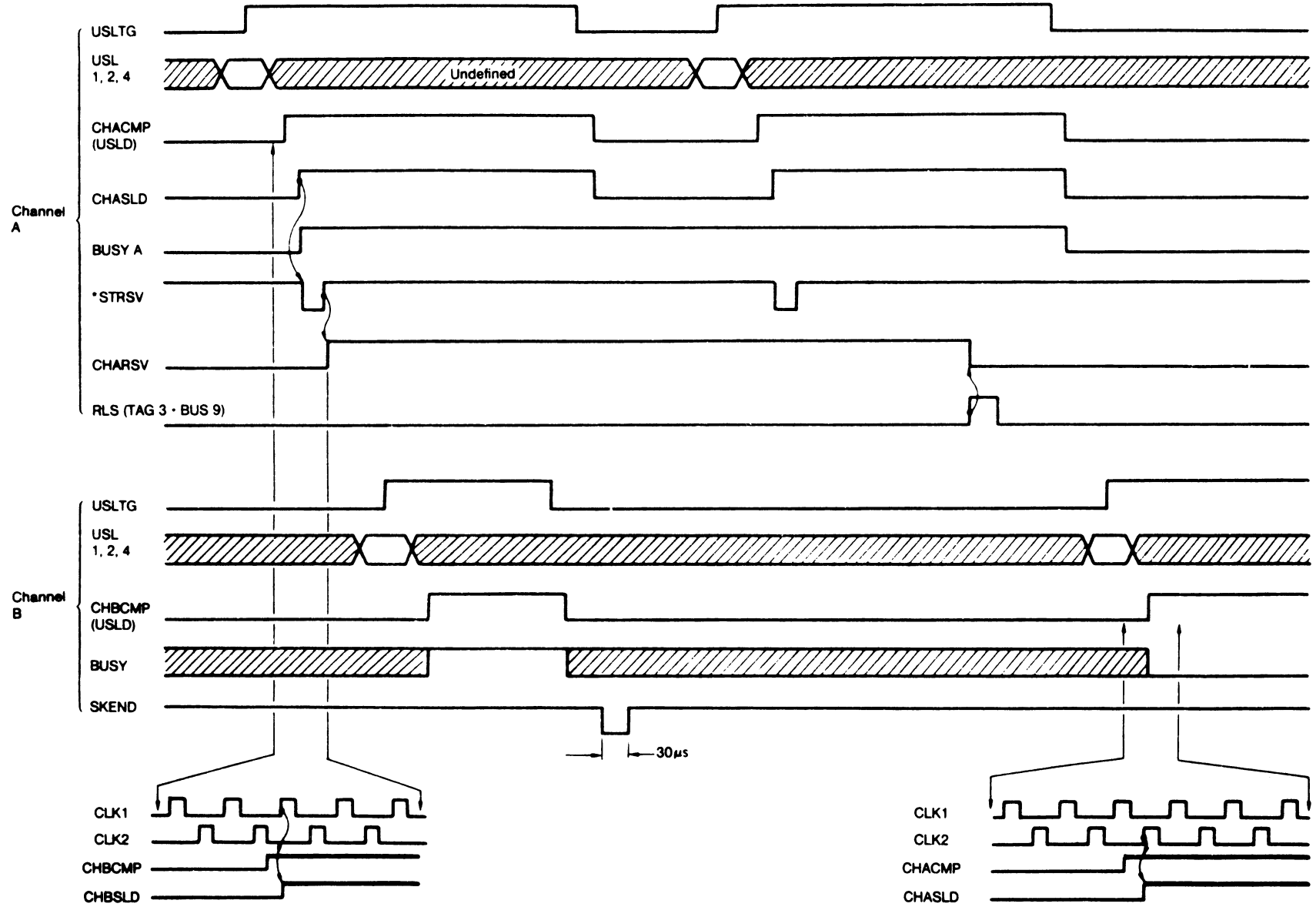


Figure 4.6.8 Select/Reserve Timing Chart

4.6.2.2 Release

The release command resets the reserved and priority select (unconditional reserve) states. Release is executed by the two functions described below. One is a release command from a control unit (Tag 3 Bus bit 9) and the other is the Release Timer of the dual port option.

- (1) **Release command (Tag 3, Bus bit 9)**
Reserve and Priority Select (unconditional reserve) are reset by the leading edge of Tag 3 and Bus Bit 9 sent from the control unit. Thus, it is possible to be accessed from the control unit of the opposite channel.
- (2) **Release Timer**
If the switch on the dual port is set to the RLTM position. The Release function is enabled by the unit itself. If the unit Select Tag signal goes false when the switch is being set at the RLTM position, the Release Timer one-shot of 500 ms is triggered. The Reserve Latch is reset by the trailing edge of the Release Pulse.
If the switch is set to the ABSL (Absolute Reserve) side, the one-shot is disabled.

4.6.2.3 Priority Select (Unconditioned Reserve)

Even if a unit is selected or reserved (except unconditional reserve) by a channel, the opposite channel can switch the unit to this channel by issuing a Priority Select (Unit Select Tag, unit address and Bus Bit 9) command.

The command sets the Unconditionally Reserved (UCRSV) latch to inhibit all signals, Select/Reserve is given to the channel and, at the same time, the channel which was previously connected is disconnected. Once it is set in an unconditional reserve state, all signals are disabled with respect to the opposite channel.

The Unconditionally Reserved is released only by the release command given by the channel exclusively connected.

4.6.2.4 Disable Switch

During maintenance, the interface functions related to channels A and B can be inhibited by using the maintenance switch on the XCBM printed circuit board. This disable function can be done for the two channels separately.

4.6.3 Seek Control Function

Basically, the FDU has five types of seek modes: Initial Seek, Return To Zero (RTZ), Direct Seek by Tag 1, Head Retract and Linear mode.

- (1) **Initial Seek Mode**
The Initial Seek mode causes the head to position onto cylinder zero from the Landing Zone.
- (2) **Return To Zero Mode**
The Return To Zero (RTZ) mode causes the heads to move to cylinder zero, regardless of where they are when the command is received. Basically Return To Zero mode is equivalent to the Initial Seek mode; therefore, they are referred to as the Go To Zero (GTZ) mode.
- (3) **Direct Seek by Tag 1**
Direct Seek mode causes a seek to the cylinder address specified by the Tag 1 and Bus 0 to 9 signals from the control unit.
- (4) **Head Retract Mode**
Head Retract Mode causes the heads to return to the Landing Zone if a power failure or abnormal positioning operation occurs.
- (5) **Linear Mode**
Linear Mode causes the heads to track (follow) the center of the specified cylinder after a seek operation has been completed. An offset operation is included with this mode.

The Seek Control Block Diagram is shown in Figure 4.6.9.

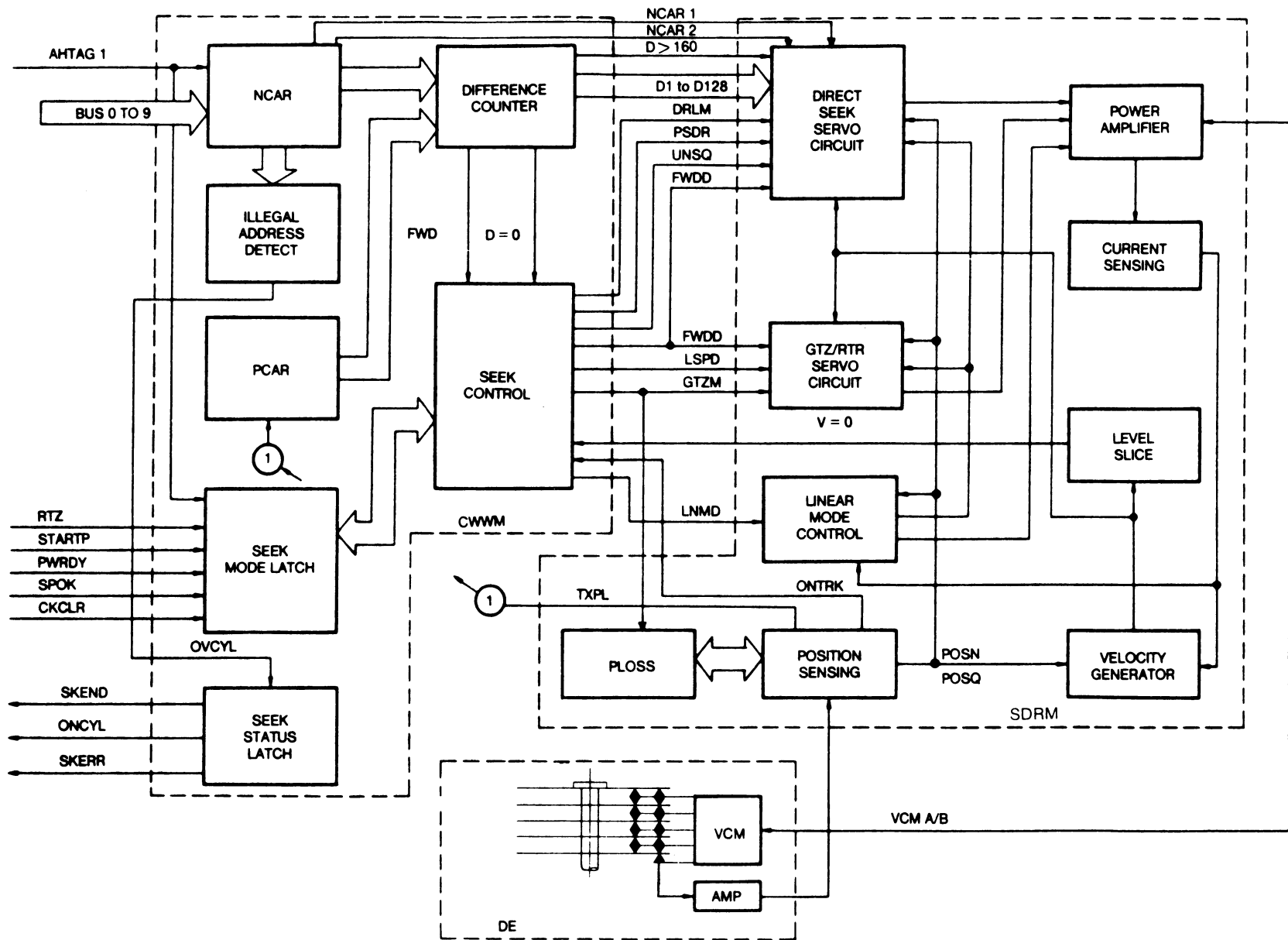


Figure 4.6.9 Seek Control Block Diagram

4.6.3.1 Initial Seek Mode

As mentioned in the Start/Stop Function section, the speed OK (SPOK) signal goes true when the rotational speed is up to 80%. The leading edge of the SPOK signal sets the Retract Mode (RTRM), and Drive Linear Motor (DRLM) signals to keep the heads on the landing zone (IGB2). Five seconds after SPOK, the Guard Band Enable (GBENB) signal goes true to enable decoding of Index and all guard band signals. Ten seconds after SPOK, the Start Pulse (STARTP) goes true; the Retract and Velocity Equals Zero ($V=0$) latches are reset; and the Initial Seek Mode (INSKM), Go To Zero (GTZ), Under Sequence (UNSQ), DRLM, and Forward Drive (FWDD) latches are all set.

At the start of the Initial Seek, the heads move toward the outside of the disk (forward) at high speed by enabling FWDD and disabling Low Speed (LSPD).

When the heads have passed through the IGB2 zone and enter the IGB1 zone, the heads are driven toward the outside of the disk at low speed by enabling the FWDD and LSPD signals.

When the heads have passed through IGB1 zone, the Position Drive (PSDR) goes true, which changes the target velocity to the Position signal. When the velocity reaches the capture range, $V=0$ signal goes true, and then it resets the DRLM latch and sets the Linear Mode (LNMD) latch. When the LNMD signal goes true it keeps the heads precisely on the center of Cylinder 0, that is, the first ODD1-EVEN1 and ODD2-EVEN2 servo track.

The first Index signal under the linear mode triggers the Settling 1 one-shot (STL1: 1.5ms). The trailing edge of the STL1 signal sets the Seek End (SKEND), On Cylinder (ONCYL) and Unit Ready (URDY) latches, and also resets the INSKM, GTZM and UNSQ latches.

If the initial seek has not been performed within 640ms after STARTP, the Device Check goes true under the not ready status. The Device Check Clear signal, under the not ready status, which is commanded from the control unit or the Check Clear key, will cause a retry of the Initial Seek sequence.

The Return To Zero (RTZ) command under the Retract Mode during Ready status initiates the Initial Seek sequence.

The flow chart at Go To Zero is shown in Figure 4.6.10, and the timing chart for Initial Seek is shown in Figure 4.6.11.

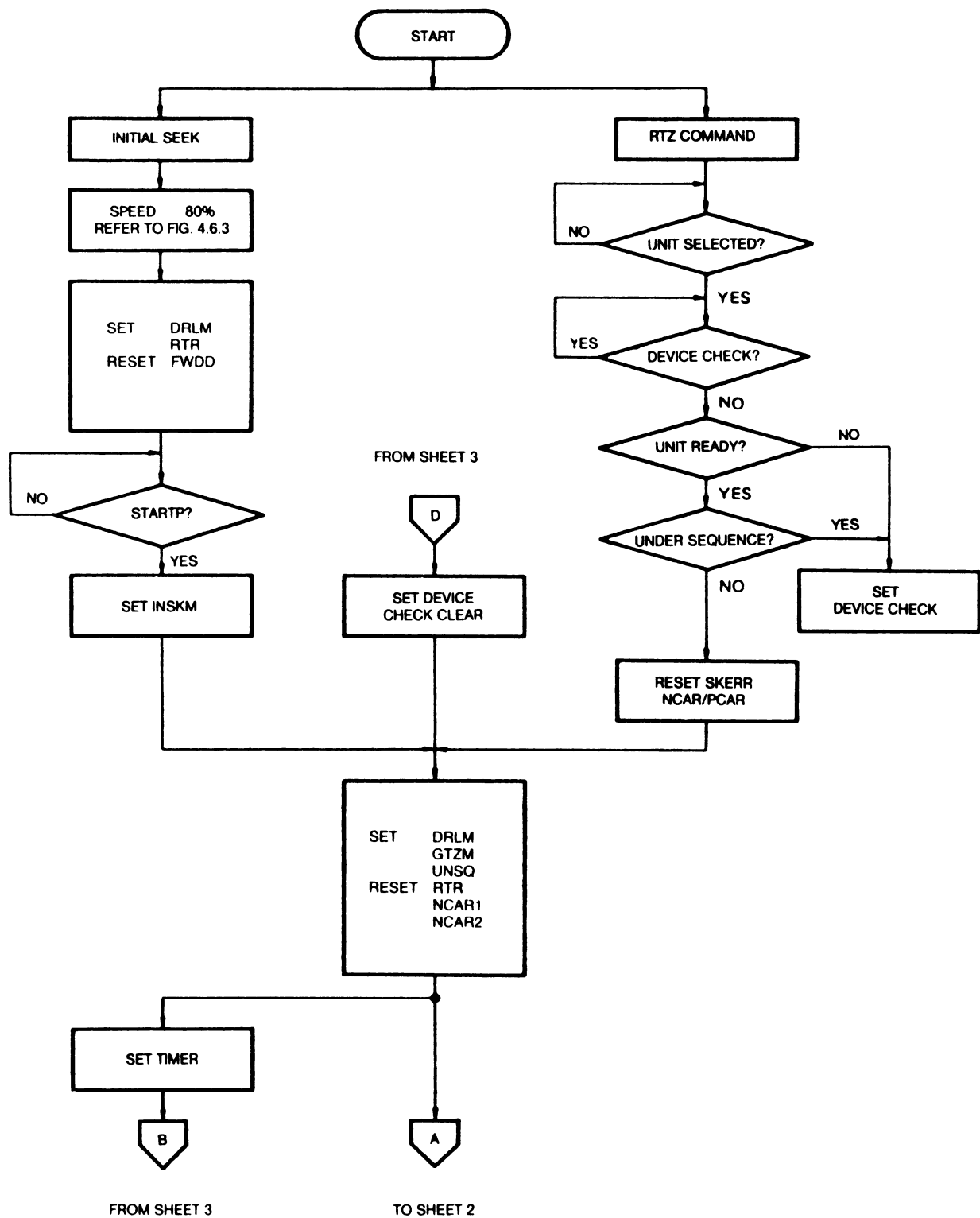
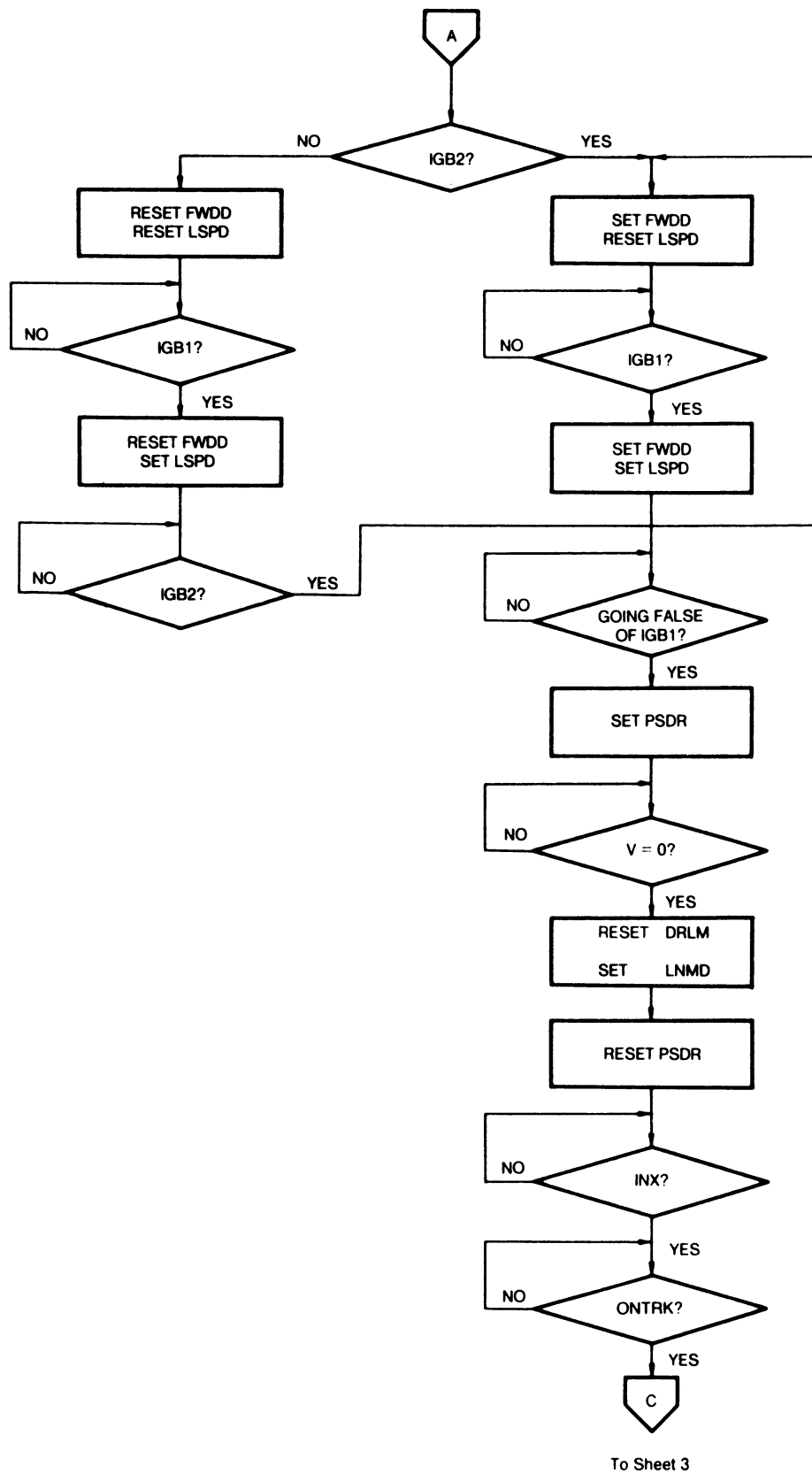


Figure 4.6.10 Go To Zero Flow Chart (Sheet 1 of 3)



To Sheet 3

Figure 4.6.10 Go To Zero Flow Chart (Sheet 2 of 3)

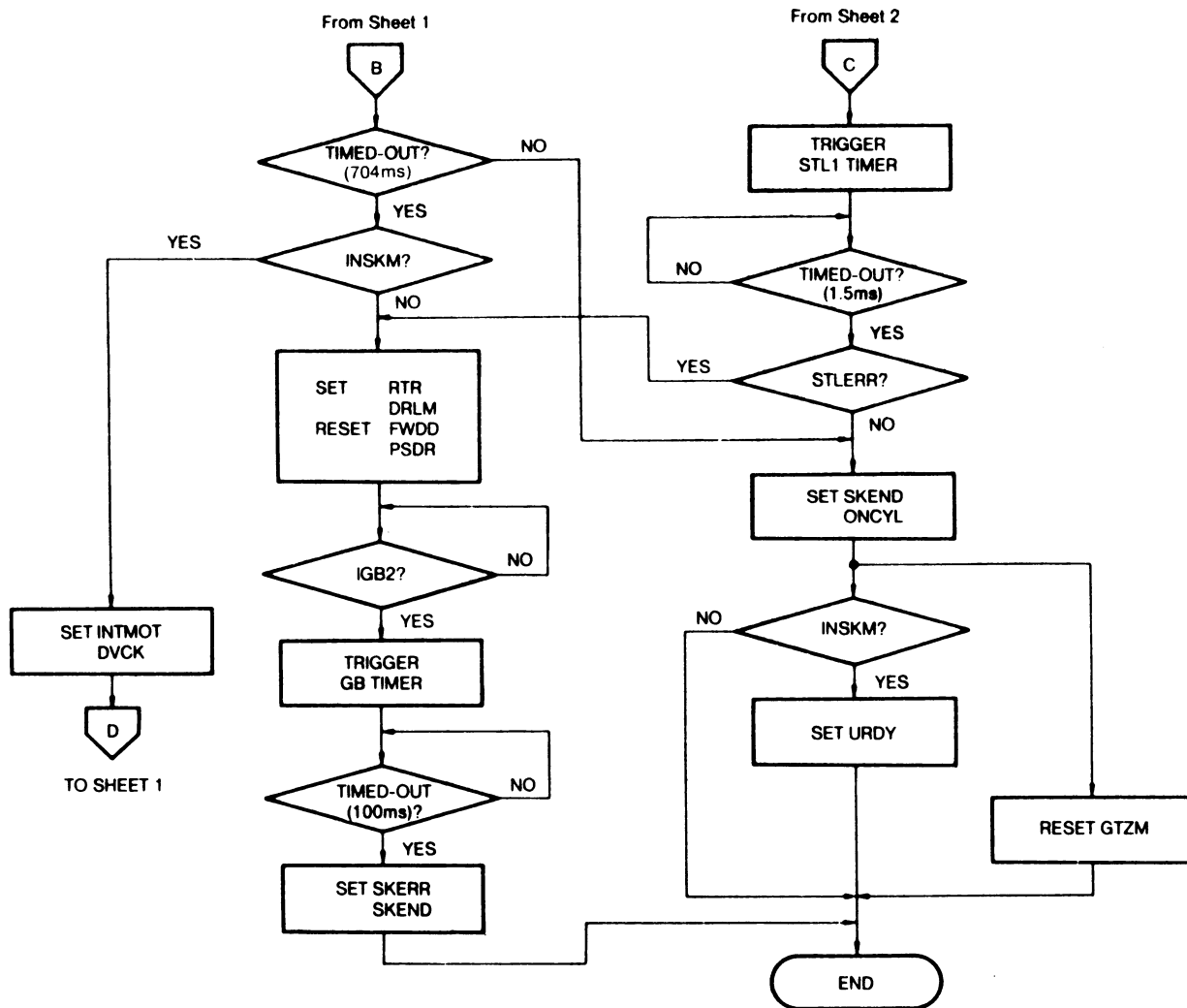


Figure 4.6.10 Go To Zero Flow Chart (Sheet 3 of 3)

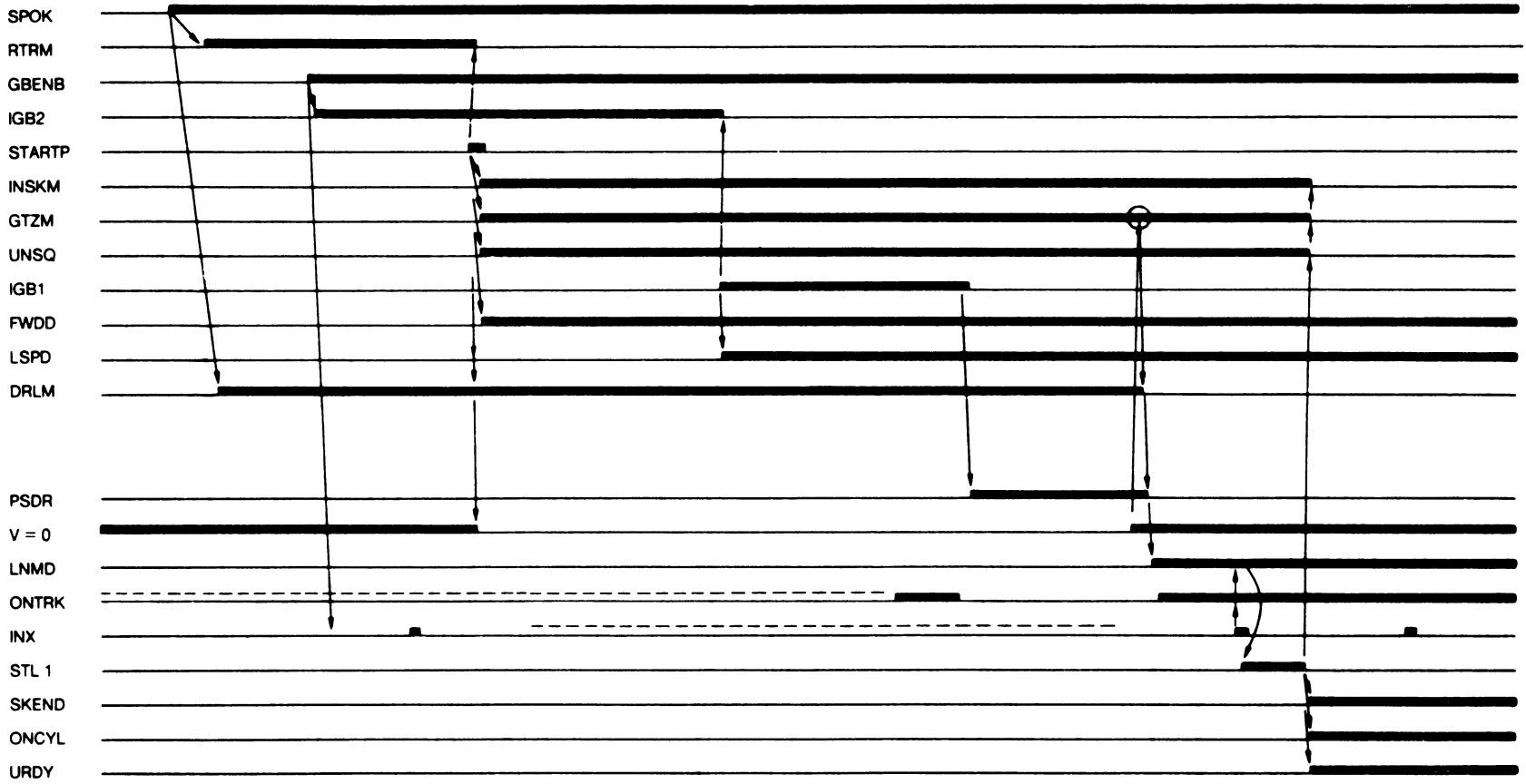


Figure 4.6.11 Initial Seek Timing Chart

4.6.3.2 Return to Zero Mode

The Return To Zero Mode is initiated by the Return To Zero (RTZ) command from the control unit during Ready status and linear mode.

The RTZ command sets the GTZM and DRLM latches and resets the $V=0$, LNMD, NCAR1/2, and Seek End (SKEND) latches.

At the start of GTZM, the heads move toward the center of the disk (reverse) at high speed by disabling the FWDD and LSPD signals.

When the heads have passed through the Servo Zone and enter the IGB1 zone, the heads are driven toward the center of the disk at low speed.

When the heads enter the IGB2 zone, they are driven toward the perimeter (forward) at high speed. When the heads enter the IGB1 zone again, they are driven forward at low speed.

The subsequent sequence is equivalent to the Initial Seek Mode.

The RTZ timing chart is shown in Figure 4.6.12.



4.6.3.3 Direct Seek Mode

Direct Seek mode is initiated by activating the Tag 1 signal.

The leading edge of Tag 1 sets the bus bits 0 to 9 into the Next Cylinder Address Register (NCAR) when the bus contains an address of less than 1023.

When the NCAR output is not equal to the Present Cylinder Address Register (PCAR) output at the trailing edge of the Tag 1 signal (Fall Tag 1: FTAG1), a Direct Seek is initiated.

The FTGA1 signal resets the ONCYL, SKEND, LNMD, and $V = 0$ latches, and also sets the SEKM, DRLM, UNSQ, and direction latches.

NCAR1 and 2 signals are applied to the Servo Control circuit to determine the phase of the target cylinder.

The difference between NCAR and PCAR is equal to the number of cylinders to be moved to the desired address. The difference counter output, binary-coded D1 to D128 and $D > 160$, is sent to the servo control circuit to generate the target velocity.

When the NCAR is greater than PCAR, the forward direction is set, and when the NCAR is less than the PCAR, the reverse direction is set using the FWDD signal.

When the heads start to move to the desired address, the Track Crossing Pulse (TXPL) is sent from the servo circuit to the PCAR counter every time the servo head crosses a cylinder. The PCAR counter is increased by the trailing edge of the TXPL signal in the forward direction, and is decreased in the reverse direction.

When the difference is equal to zero, the Position Drive (PSDR) signal is activated and the velocity follows the position signal. When the $V = 0$ signal goes true, LNMD latch is set, and DRLM and PSDR latches are reset. The successive ONTRK signal triggers the Settling 1 (STL1) one-shot (1.5 ms). The trailing edge of STL1 signal sets the ONCYL and SKEND latches and reset the SEKM and UNSQ latches.

If NCAR is equal to PCAR at the leading edge of Tag 1, a No Motion Seek (NOSEK) signal is activated and triggers Settling 2 (STL2: 5 us) one-shot. The ONCYL and SKEND signals are reset by the trailing edge of the TAG1 signal and then ONCYL and SKEND signals go true at the trailing edge of STL2 signal.

The Direct Seek flow chart is shown in Figure 4.6.13 and the timing chart is shown in Figure 4.6.14.

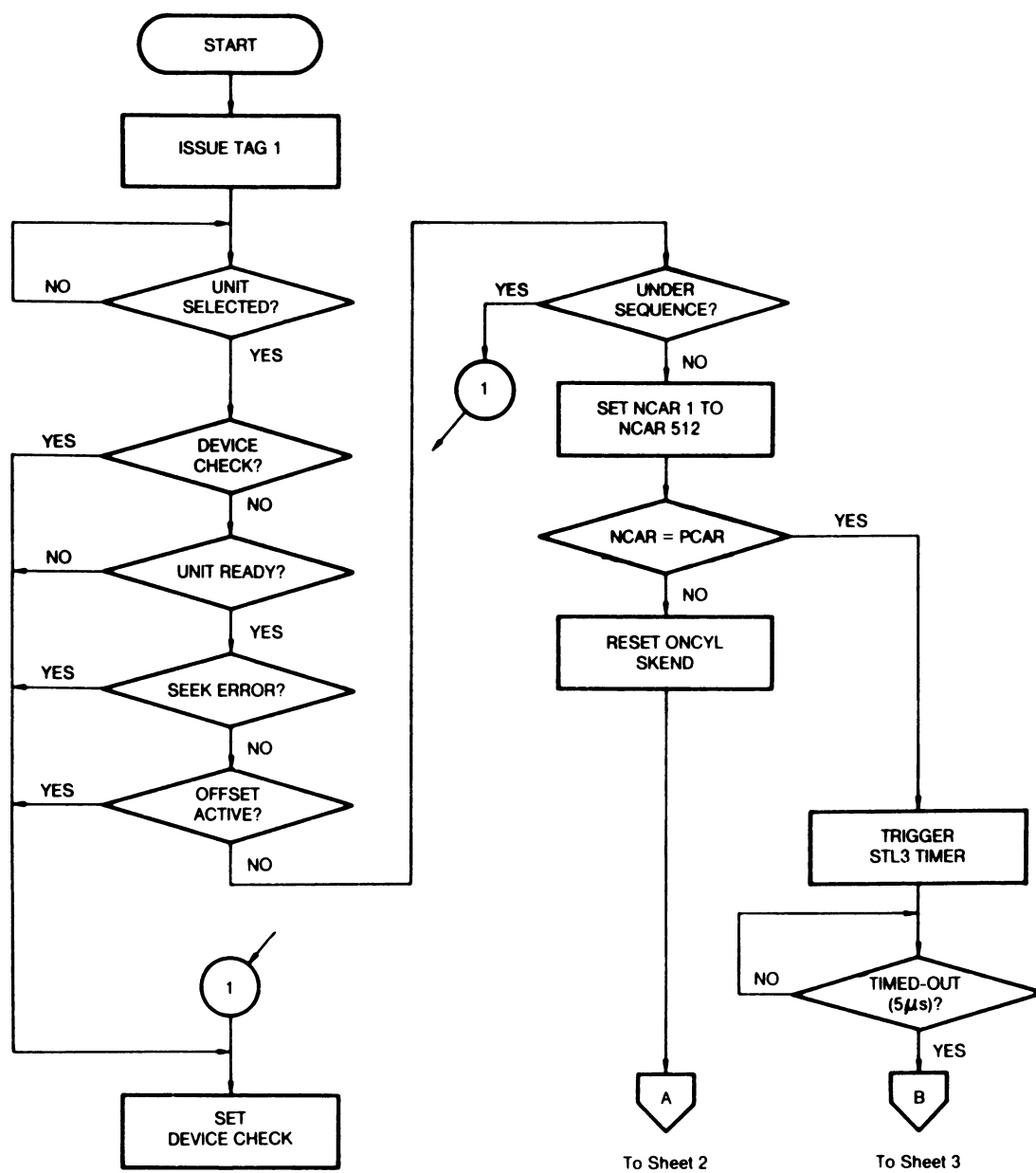


Figure 4.6.13 Direct Seek Flow Chart (Sheet 1 of 3)

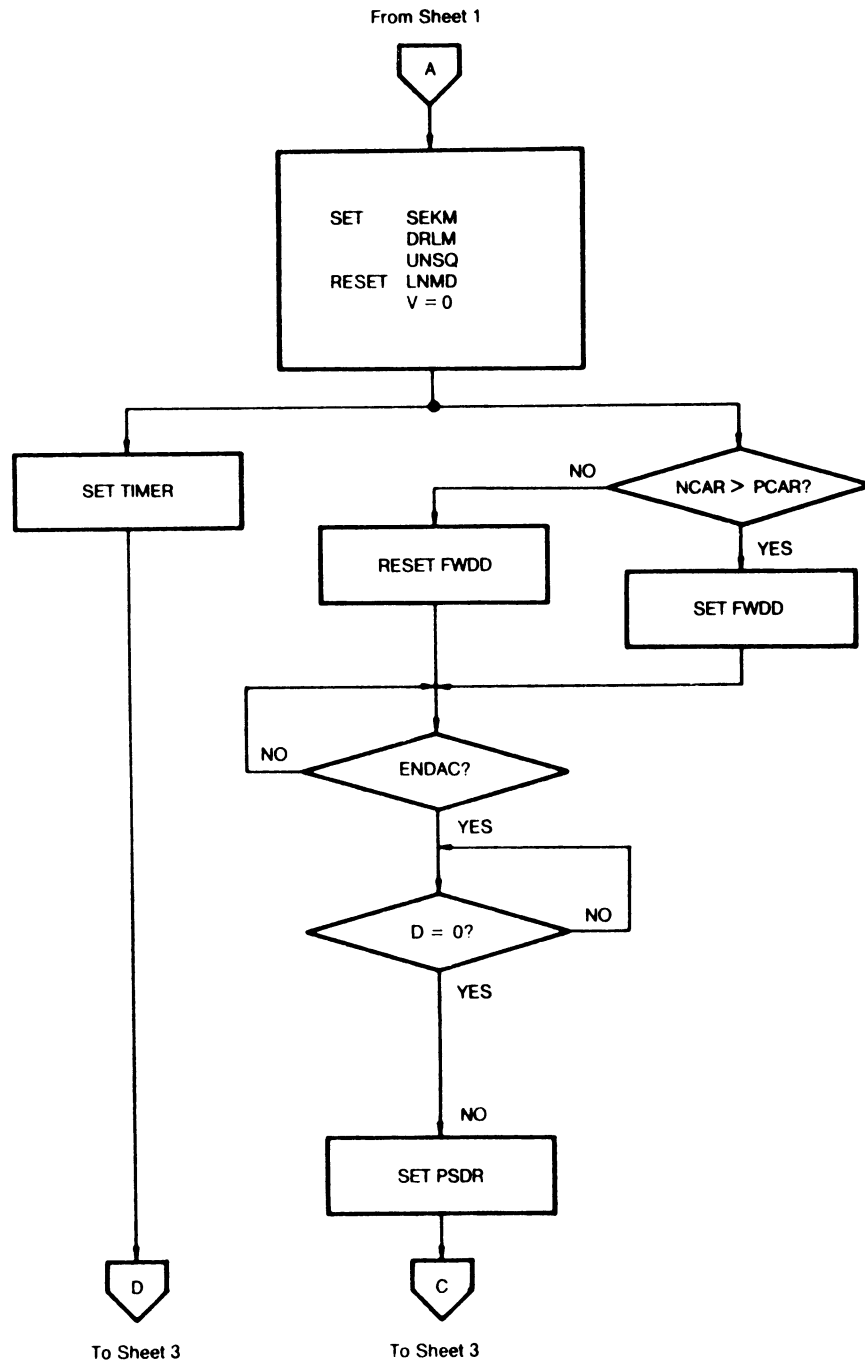


Figure 4.6.13 Direct Seek Flow Chart (Sheet 2 of 3)

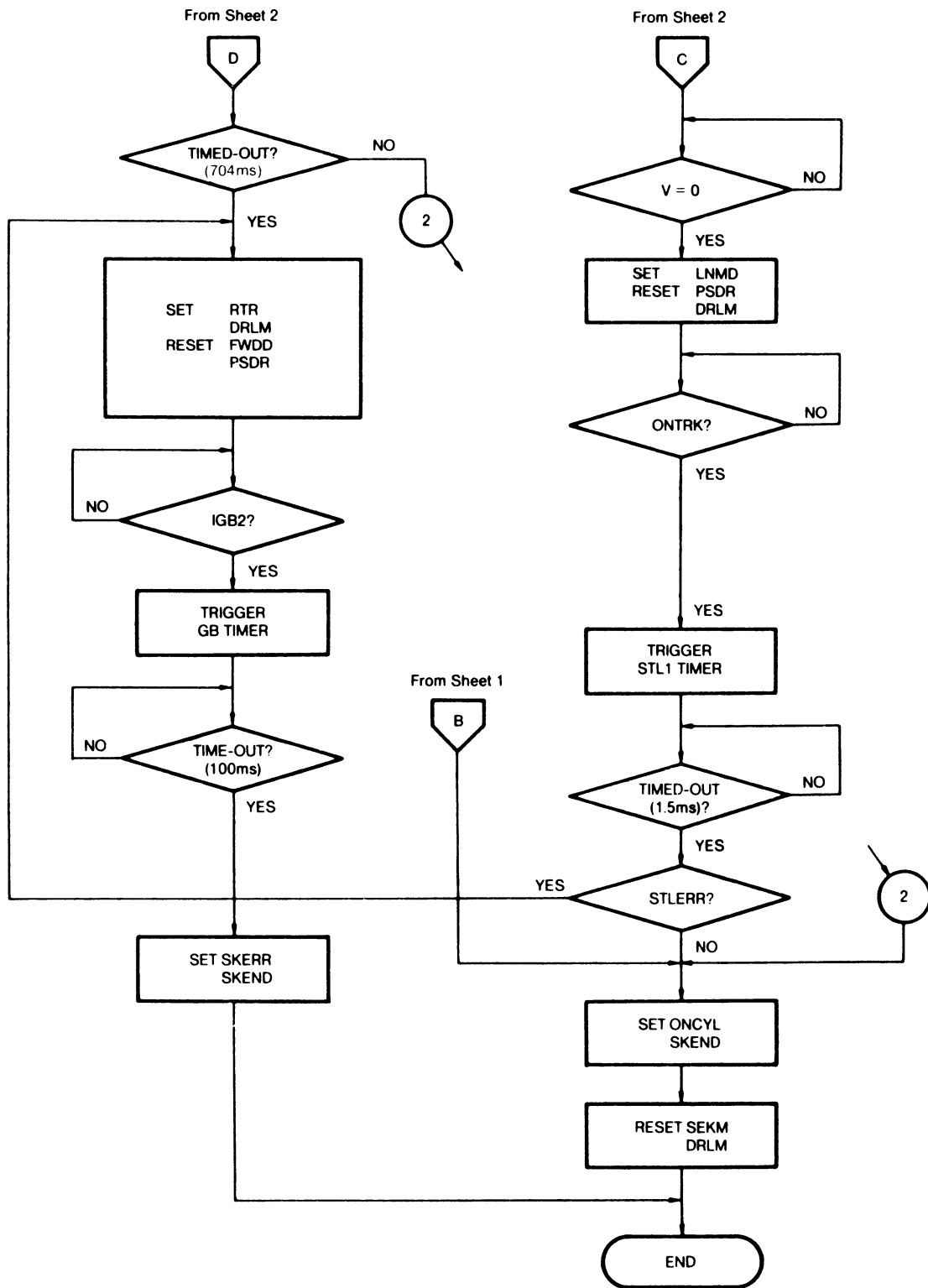


Figure 4.6.13 Direct Seek Flow Chart (Sheet 3 of 3)

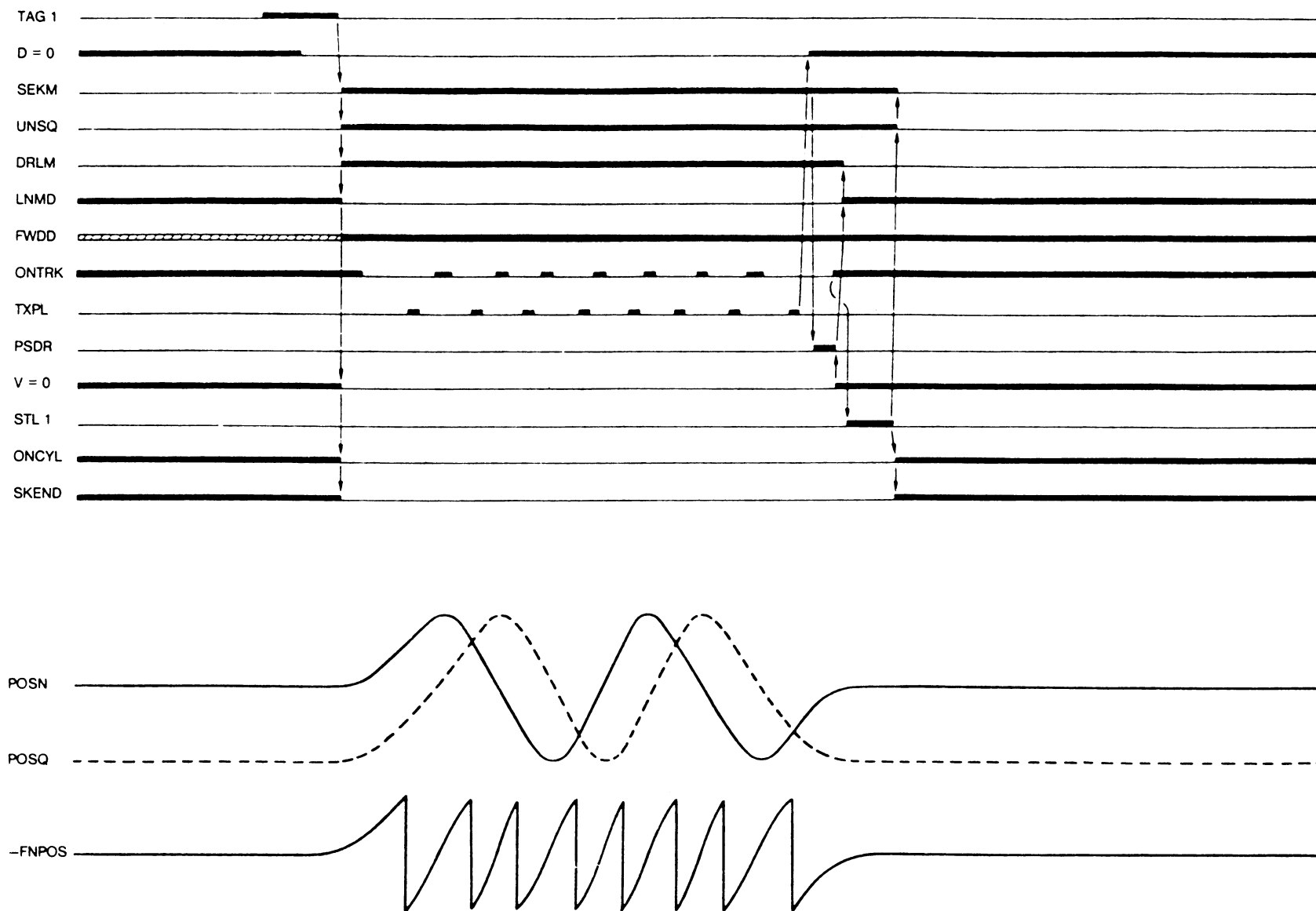


Figure 4.6.14 Direct Seek Timing Chart

4.6.3.4 Retract Mode

If a seek malfunction shown in Table 4.6.1 occurs in the drive, Retract Mode (RTRM) is set, all servo modes (INSKM, SEKM, and LNMD) are reset and the heads move to the Landing Zone by discharging the retract capacitor through the VCM coil.

Table 4.6.1 Seek Malfunctions

ERROR	UNIT STATUS
Initial Seek Time Out	Not Ready
Rotational Speed Low	Not Ready
DC voltage fault	Not Ready
Time Out in Any Seek Mode	Seek Error
Over-shoot in Linear Mode	Seek Error
Any Guard Band in Seek Mode	Seek Error
OGB in Go To Zero Mode	Seek Error
Any Guard Band in Linear Mode	Seek Error

4.6.4 Servo Circuit Function

4.6.4.1 Position Sensing

This section describes the Position Sensing functions from the output of the servo head to the generating the position signal. The Position Sensing block diagram is shown in Figure 4.6.15.

The servo data written on the servo surface is read by the servo head, amplified through the Head-Preamplifier (with a nominal gain of 35), and applied to the Automatic Gain Control (AGC) amplifier on SDRM PCB. The AGC amplifier keeps the output constant with an AGC voltage from the Summing Amplifier, even if the AGC input varies. The AGC output is applied to a Low Pass Filter (LPF), which attenuates the unused high frequencies, and then is amplified by the Carrier Amplifier. The Carrier Amplifier issues the Servo (SERVO) signal of a four-byte interval to the Level Slice and Peak Hold circuits.

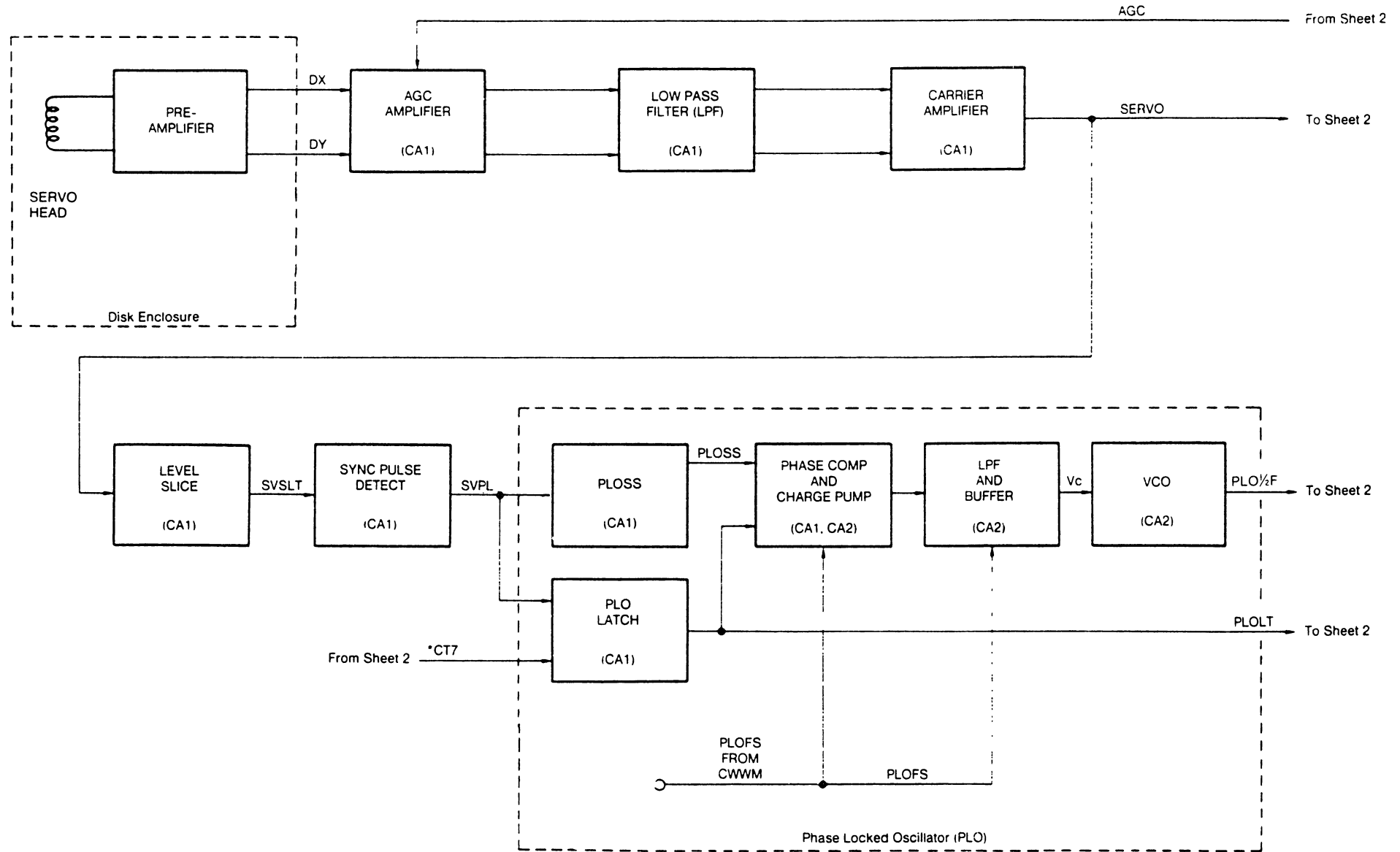


Figure 4.6.15 Position Sensing Block Diagram (Sheet 1 of 2)

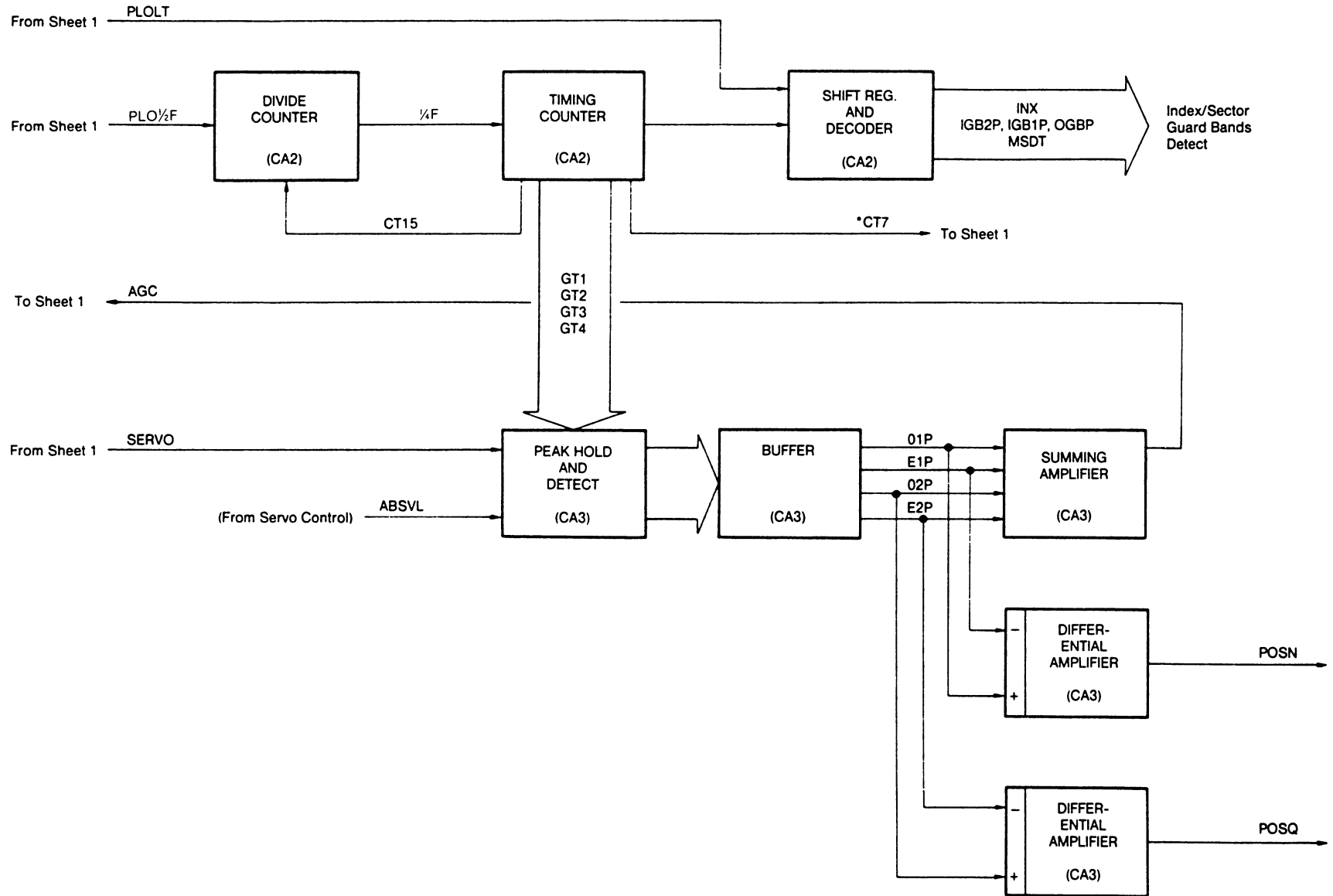


Figure 4.6.15 Position Sensing Block Diagram (Sheet 2 of 2)

The SERVO signal is converted into the Servo Slice Output (SVSLT) signal at a TTL level. The SVSLT signal triggers a 100 ns pulse at its trailing edge and the trailing edge of this 100 ns pulse triggers the 450-ns-long Servo Pulse Window (SVPWD) one-shot. The SVPWD signal separates only the Sync Pulse, that is, it separates the Servo Pulse (SVPLS) signal from the SVSLT signal. The SVPLS Signal is applied to the Phase Locked Oscillator (PLO).

The leading edge of the SVPLS Signal triggers PLOSS one-shot (2.10 μ s) and sets the PLO Latch circuit. The PLO Latch is reset by the leading edge of the Count 7 (CT7) signal, which is the output signal of the Timing Counter, and issues the PLO Latch (PLOLT) signal to the Phase Comparator circuit and the Index Guard Bands sense circuit.

The PLOSS and PLOLT signals are applied to the Phase Comparator circuit of PLO. The Phase Comparator issues an Increase (INC) signal when phase-lag has occurred on the VCO output, or a Decrease (DEC) signal when phase-lead has occurred on the VCO output. The INC and DEC signals are applied to the Charge Pump circuit which converts the phase difference into a DC-level signal. The Charge Pump circuit issues a control voltage to the Voltage Controlled Oscillator (VCO) through the Low Pass Filter (LPF). Thus, the PLO circuit synchronizes with the SVPLS signal and generates a one-bit cell clock, that is, the PLO1F signal. The PLO1F signal is applied to the VFO circuit and the Timing Counter circuit.

The Timing Counter circuit divides the PLO $\frac{1}{2}$ F signal by two into $\frac{1}{4}$ F signal. The $\frac{1}{4}$ F signal generates the Gate 1, 2, 3, and 4 (GT1 to GT4) signals. Count 15 (CT15), which resets the divide counter and the CT7 signal, which resets the PLOLT signal.

The Peak Hold circuit holds the position of the peak signals (Odd 1, Even 1, Odd 2 and Even 2) enabling the GT1 to GT4 timing signals. The Peak-hold outputs (Odd 1 peak, Even 1 peak, Odd 2 peak, and Even 2 peak) are applied to the Summing Amplifier and two Differential Amplifier circuits.

The Differential Amplifiers issue the Position Normal (POSN) signal from Odd 1 peak and Even 1 peak signals, and the Position Quadrature (POSQ) signal from Odd 2 peak and Even 2 peak signals. The Summing Amplifier issues the AGC Control Voltage (AGC) signal for the AGC amplifier. The timing chart for PLO and Peak Hold is shown in Figure 4.6.16. The conversion waveform for Servo signal to dual-phase position signal is shown in Figure 4.6.17, which is valid when the servo head is moving.

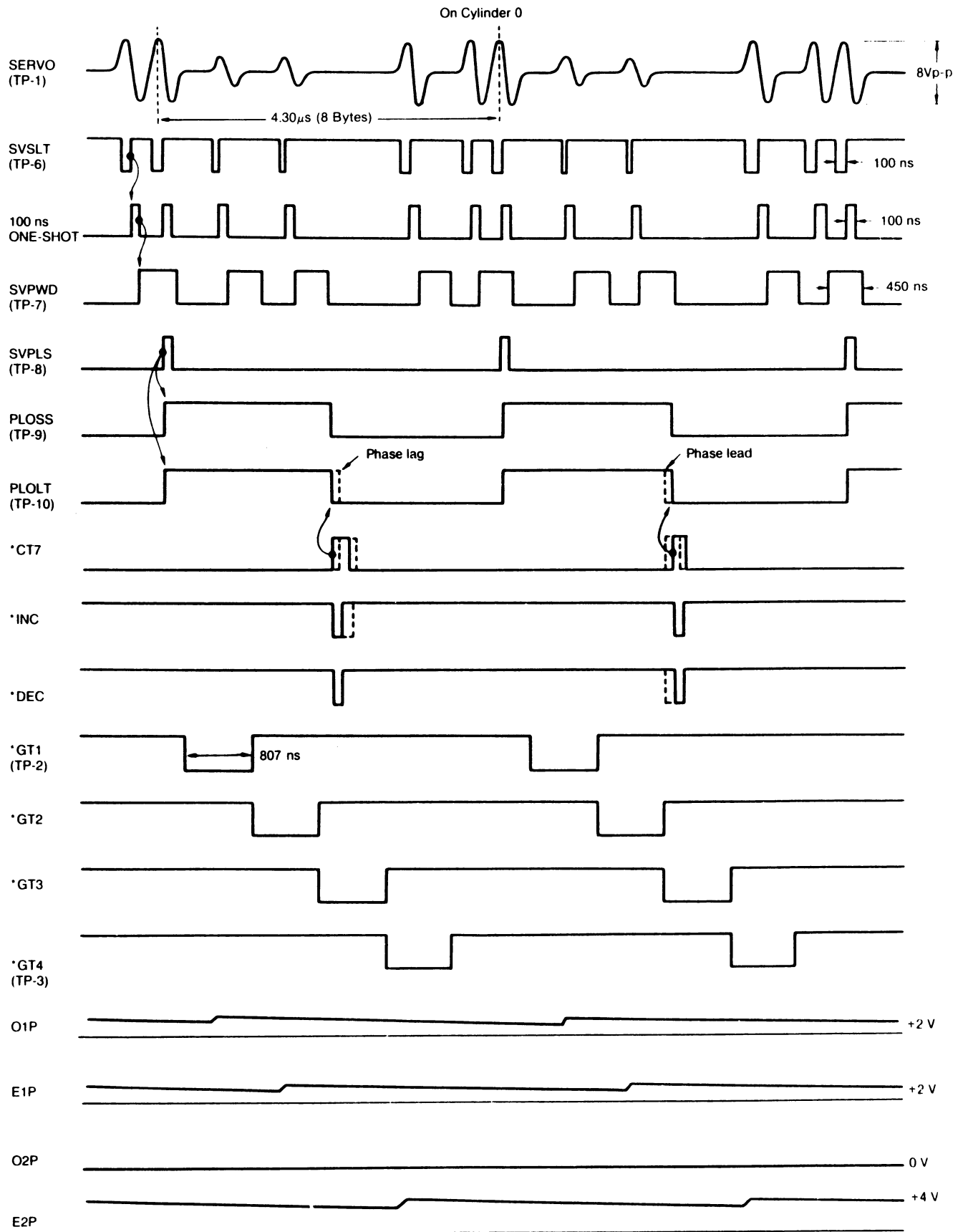


Figure 4.6.16 PLO and Peak Hold Timing Chart (SDRM)

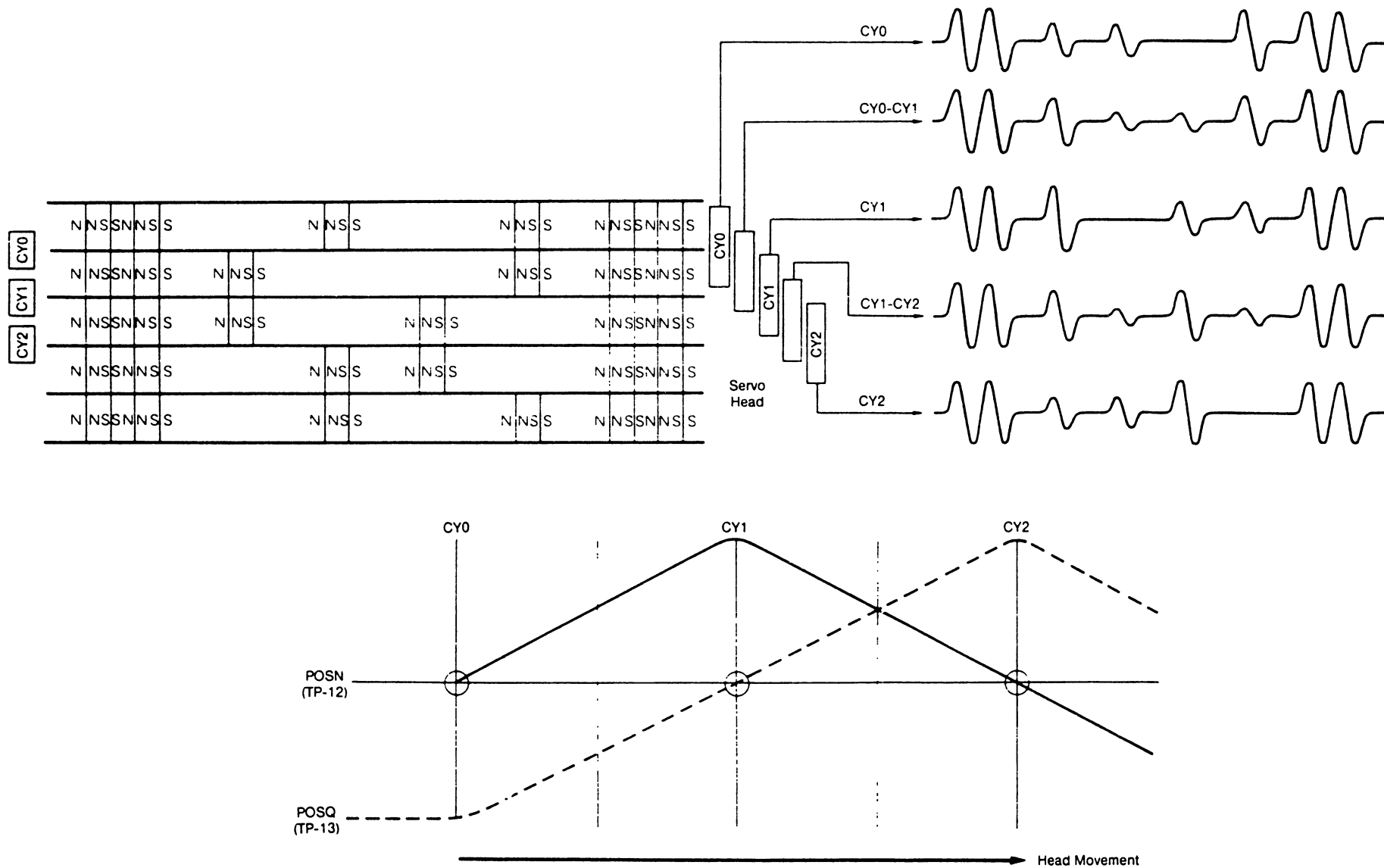


Figure 4.6.17 Servo Signal to Position Signal Conversion (SDRM)

4.6.4.2 Servo Control

The block diagram of the Servo Control circuit after Position Sensing is shown in Figure 4.6.18.

(1) Block Description

(a) Position Signal Slice

The dual-phase position signals, POSN and POSQ, which are demodulated through Position Sensing circuitry, are applied to a level slice circuit. The Position Signal Slice circuit then issues $N > Q$ and $N + Q > 0$ signals which are applied to Position Decoder. It also issues an Off-track (OFTRK) signal which indicates that the servo head positions off from the center of each cylinder.

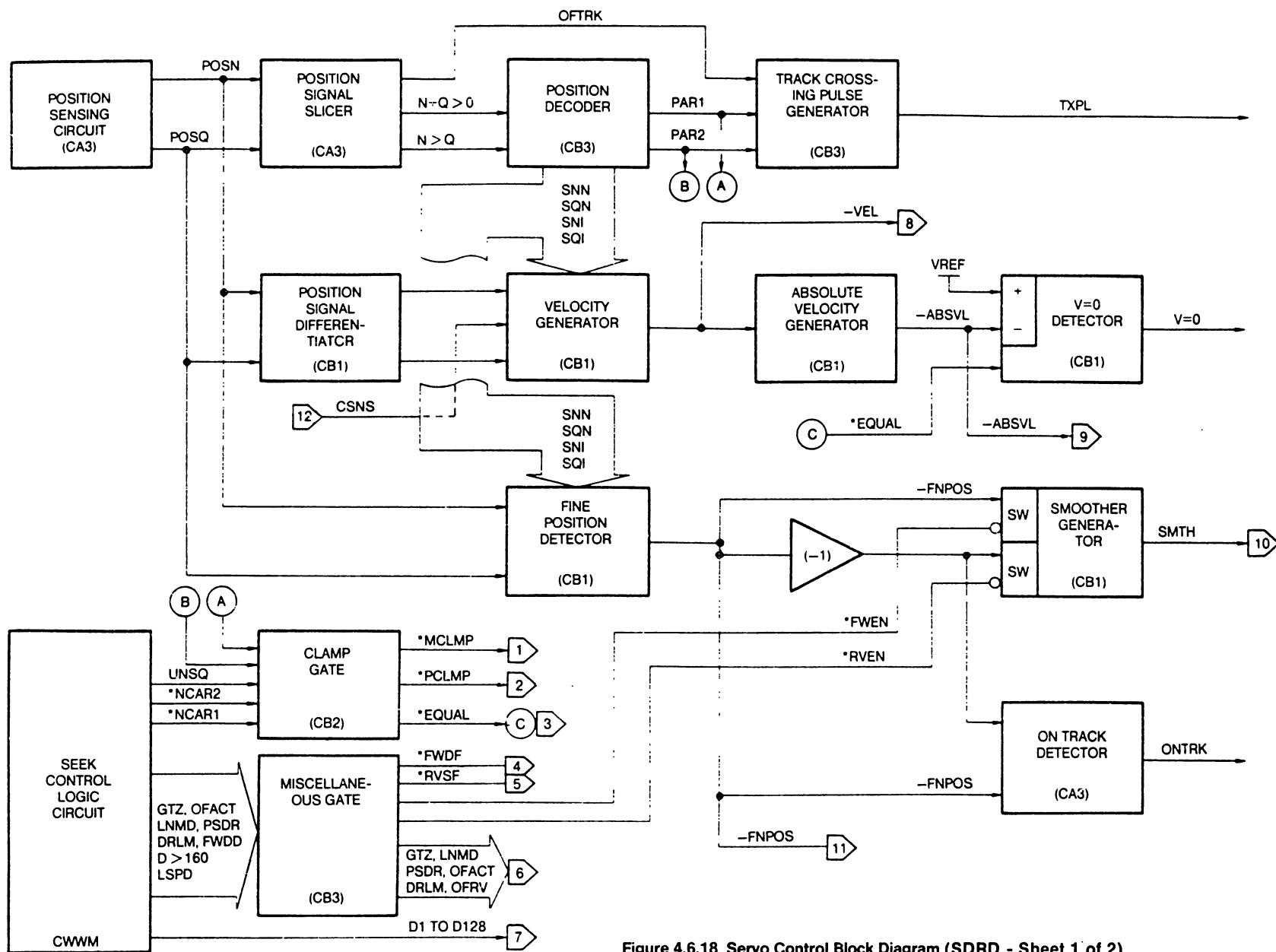


Figure 4.6.18 Servo Control Block Diagram (SDRD - Sheet 1 of 2)

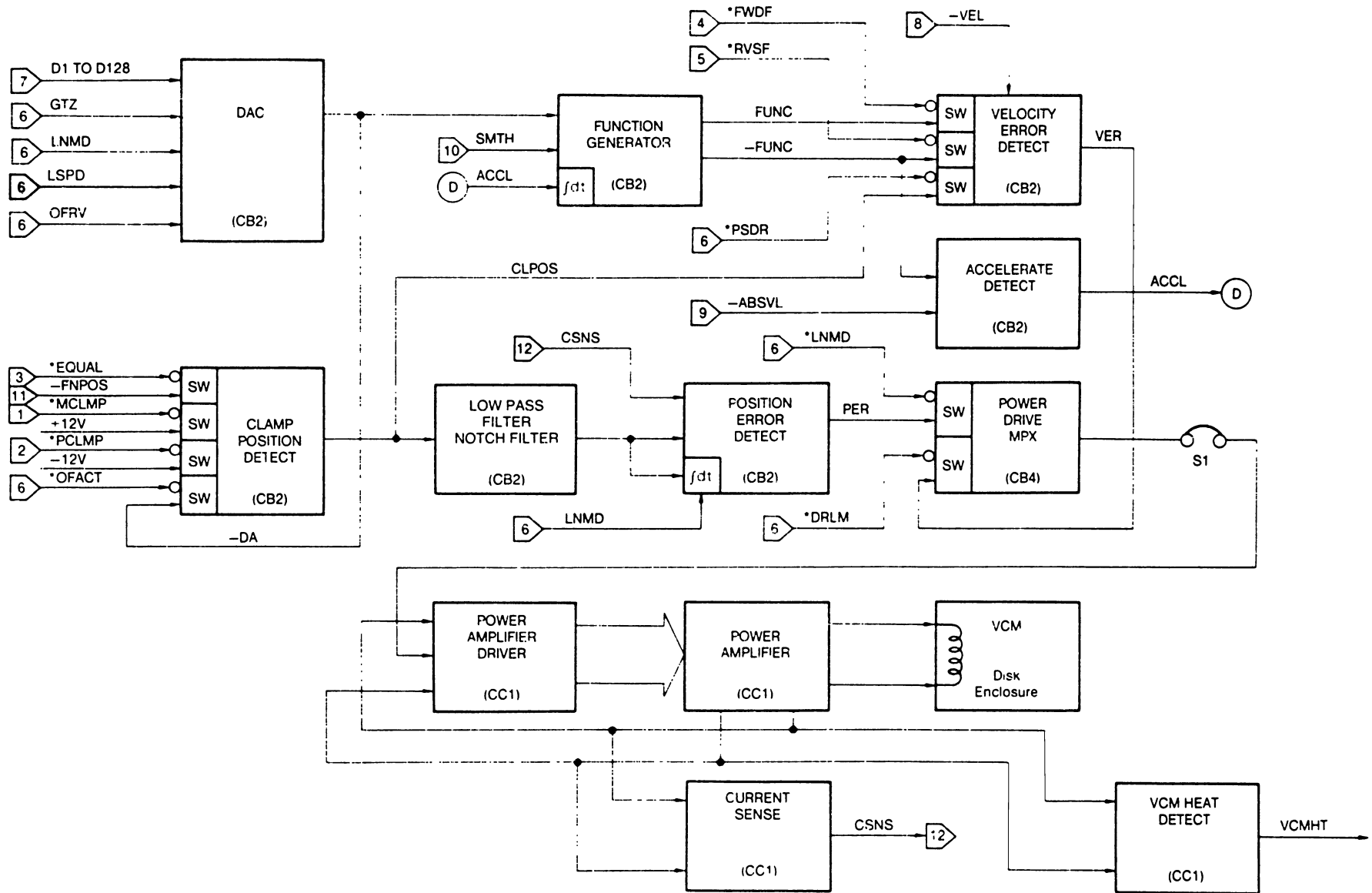


Figure 4.6 18 Servo Control Block Diagram (SDRM - Sheet 2 of 2)

(b) Position Decoder

The Position Decoder circuit issues the two least-significant bits of the current cylinder address, Present Address 2 and 1 (PAR2 and PAR1), which decode the $N > Q$ and $N + Q > 0$ signals. The Position Decoder circuit also issues Select N Non-invert (SNN), Select Q Non-invert (SQN), Select N Invert (SNI), and Select Q Invert (SQI) signals, which control the Velocity Generator circuit and Fine Position Detector circuit.

(c) Track Crossing Pulse Generator

The Track Crossing Pulse Generator circuit issues a 15- μ s-wide Track Crossing Pulse (TXPLS), which is generated by PAR2, PAR1, and OFTRK signals, and which is applied to the Present Cylinder Address Register (PCAR). The PCAR counts up the TXPLS signal when Forward Drive (FWDD) signal is true, and counts down when FWDD signal is false.

The timing chart for items (1) through (3) is shown in Figure 4.6.19.

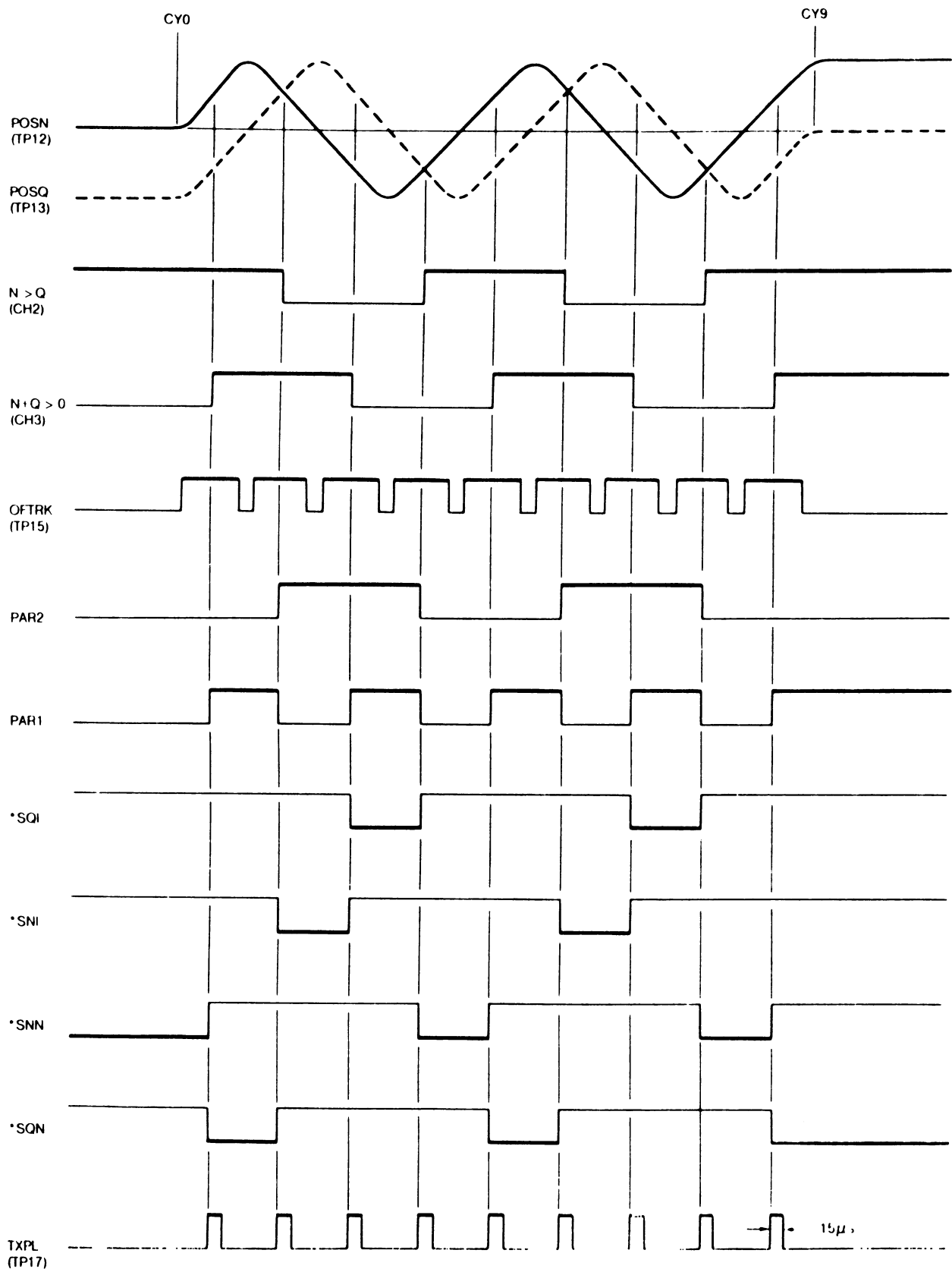


Figure 4.6.19 Position Detect Timing Chart (SDRM)

- (d) **Position Signal Differentiator**
The Position Signal Differentiator circuit differentiates the dual-phase position signals, POSN and POSQ, to generate the actual velocity from the linear portion of the position signal.
- (e) **Velocity Generator**
The SQL, SNI, SNN, and SQN signals, which are issued from the Position Decoder circuit, pull out the linear portion of the position signals; the composed signal and Current Sense (CSNS) signal are then converted into the Velocity (VEL) signal.
- (f) **Absolute Velocity Generator**
The Absolute Velocity Generator converts the velocity signal, with polarity, into the Absolute Velocity (ABSVL) signal.
- (g) **V=0 Detector**
When the Equal signal on the Clamp Gate circuit goes true, and the velocity is within 1 cm/second, the Velocity Equal to Zero ($V=0$) signal is issued to the Seek Control circuit and then the Seek mode is changed to Linear mode by terminating Seek operation.
The timing chart of the Velocity Generator is shown in Figure 4.6.20.

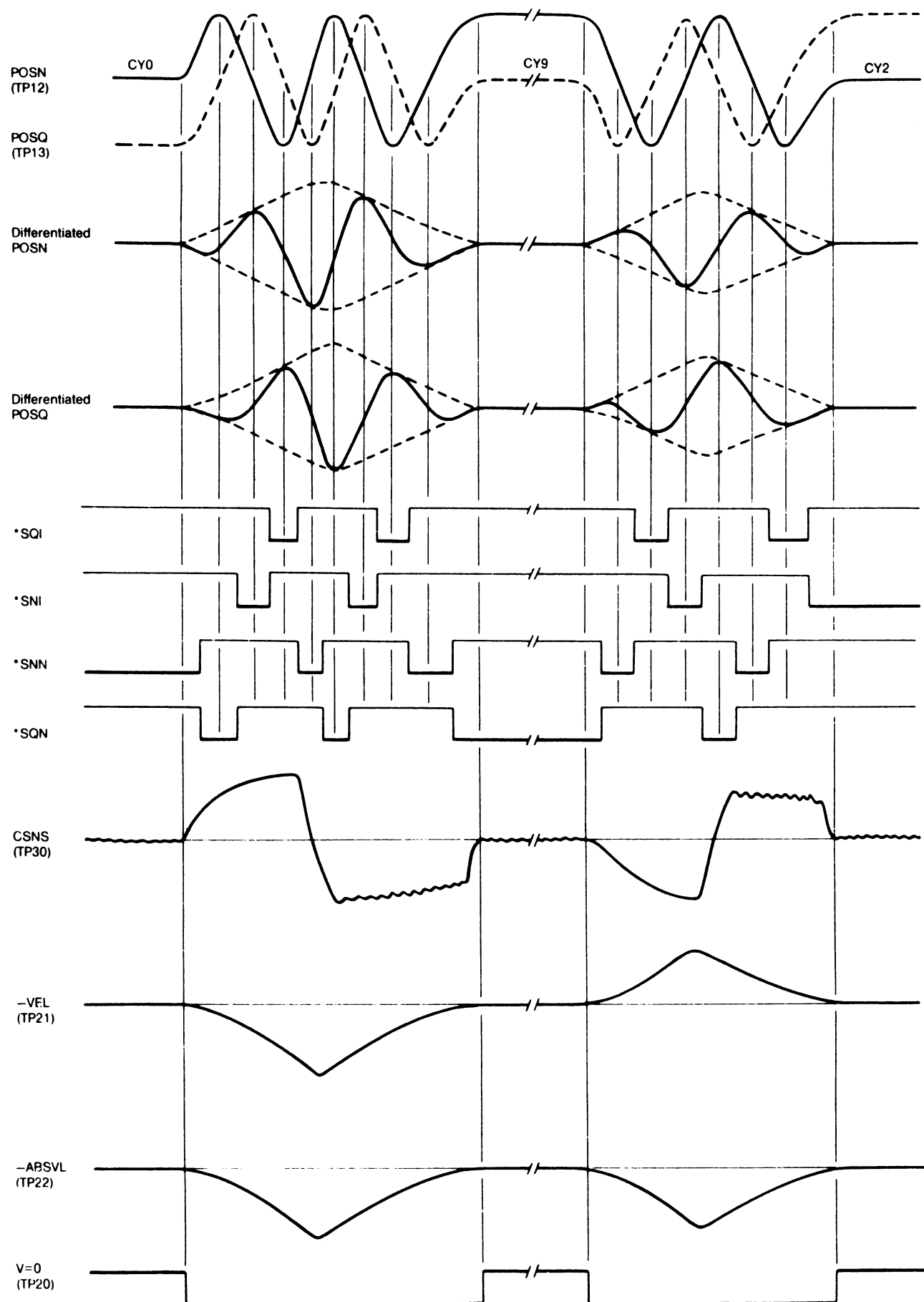


Figure 4.6.19 Position Detect Timing Chart (SDRM)

- (h) **Fine Position Detector**
The Fine Position Detector circuit pulls out the linear position, that is, the Fine Position (FNPOS) signal from the POSN and POSQ signals is controlled by SQI, SNI, SNN, and SQN signals. The FNPOS signal is applied to the Smoother, On Track Detector, and Clamp Position Detector circuits.
- (i) **Smoother Generator**
The Smoother Generator circuit polarizes the FNPOS (the polarity of signal which is in accord with the head movement direction) and issues the Smoother (SMTH) signal. The SMTH signal makes the DA signal smooth through the Function Generator circuit (see item (l), below). When the difference between NCAR and PCAR, however, is greater than 160 during Direct Seek mode, or GTZ mode is activated then the SMTH signal is deactivated.
- (j) **On Track Detector**
The On Track Detector senses the servo head position on the center of each cylinder within $\pm 5 \mu\text{m}$ and issues an On Track (ONTRK) signal to seek control and fault detect logics.

The timing chart of Fine Position Detect is shown in Figure 4.6.21.

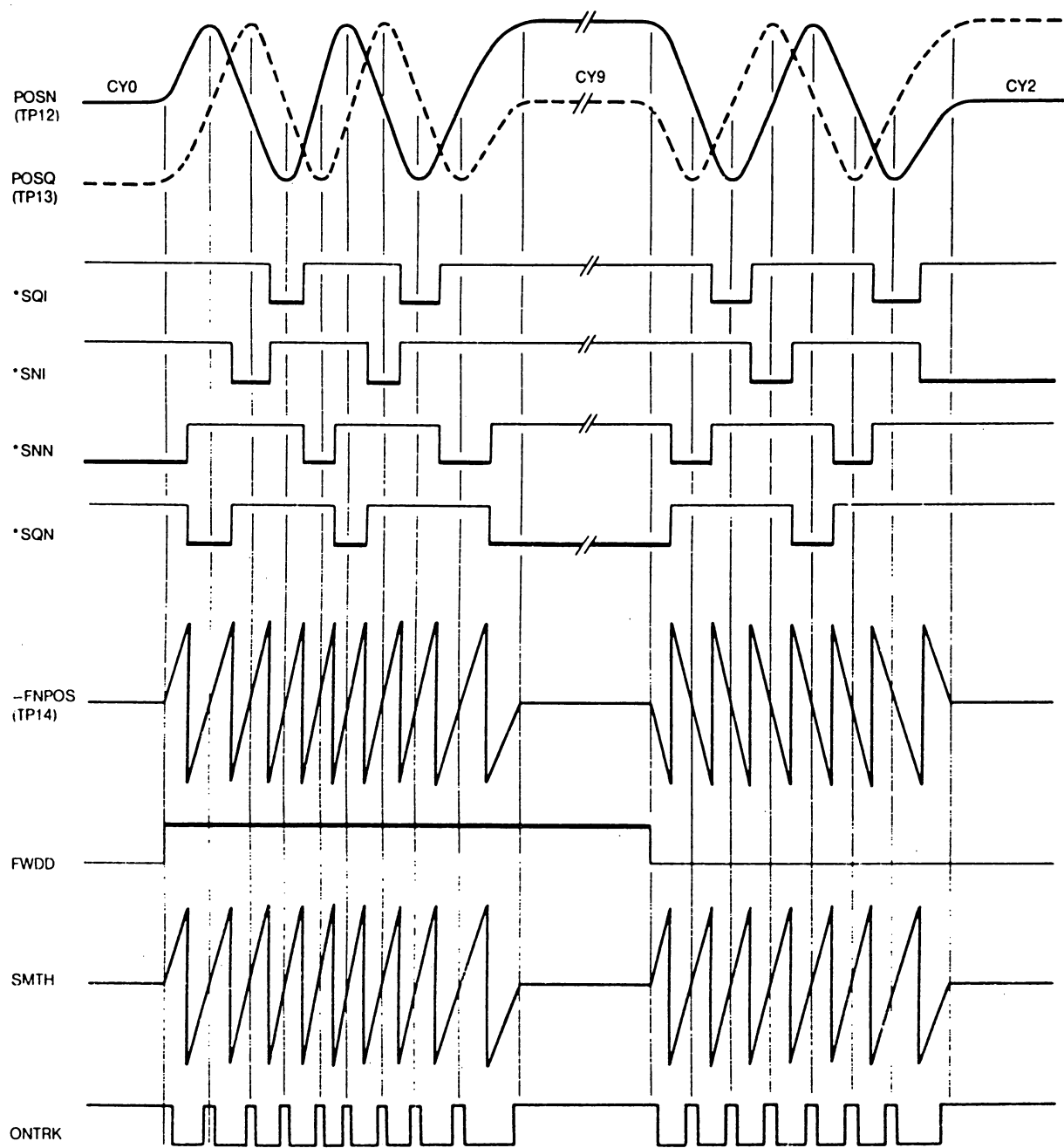


Figure 4.6.20 Fine Position Detect Timing Chart

(k) DA Converter

The DA Converter DAC circuit generates the target velocity during Direct Seek or GTZ operations. When the Direct Seek operation is performed, the Difference Counter bits D1 to D128 are applied to the DAC at the beginning of the seek operation. Whenever the servo head has passed through each cylinder, the TXPLS signal is issued and it decreases the Difference Counter. When the Difference Counter output is equal to or greater than 160, the D1 to D128 signal is clamped to 160 and the DAC output is clamped to -5.6 V .

When the GTZ operation is performed, GTZ and LSPD signals set a target velocity through the DAC.

When the Offset operation is performed, OFACT and OFRVS signals set the offset voltage to a value equivalent to $+3\text{ }\mu\text{m}$ from the center of cylinder. The DAC output, $-DA$ signal, is applied to the Function Generator and Clamp Position circuits.

(l) Function Generator

When the Difference Counter output is less than 160, the Function Generator circuit converts the DAC output into a smooth waveform by adding the SMTH signal. The Function Generator issues a Function (FUNC) signal which is the optimum deceleration curve for position time and the deceleration current profile.

When the servo control is changed to deceleration from acceleration, the Function Generator adds the integrated ACCL signal to the FUNC signal to avoid an excessive force to the actuator.

(m) Velocity Error Detector

The Velocity Error Detector circuit issues the Velocity Error (VER) signal, which is applied to the Power Amplifier which compares target velocity (FUNC) signal and actual velocity (VEL) signal. At the termination of Seek operation, the Clamped Position (CLPOS) signal is applied to the Velocity Error Detector instead of the FUNC signal, which activates the PSDR signal.

(n) Accelerate Detector

The Accelerate Detector output, that is, the Accelerate (ACCL) signal, is set by the leading edge of the DRLM signal and reset when the ABSVL signal is equal to the FUNC signal. The ACCL signal is applied to the Function Generator circuit.

The timing chart of the Target Velocity Generator, for a Direct Seek operation, is shown in Figure 4.6.22, and the timing chart for a GTZ operation is shown in Figure 4.6.23.

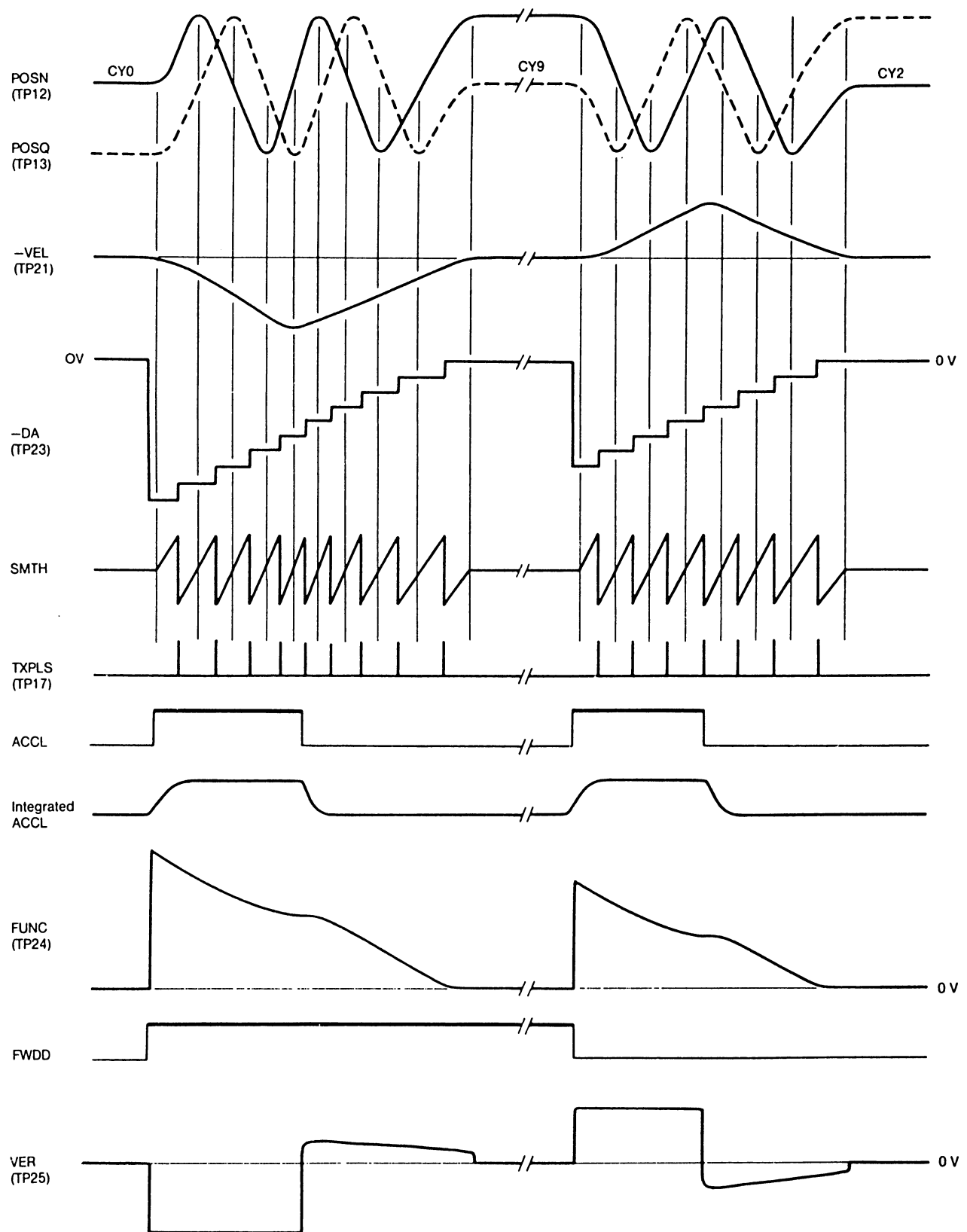


Figure 4.6.21 Direct Seek Target Velocity Generator

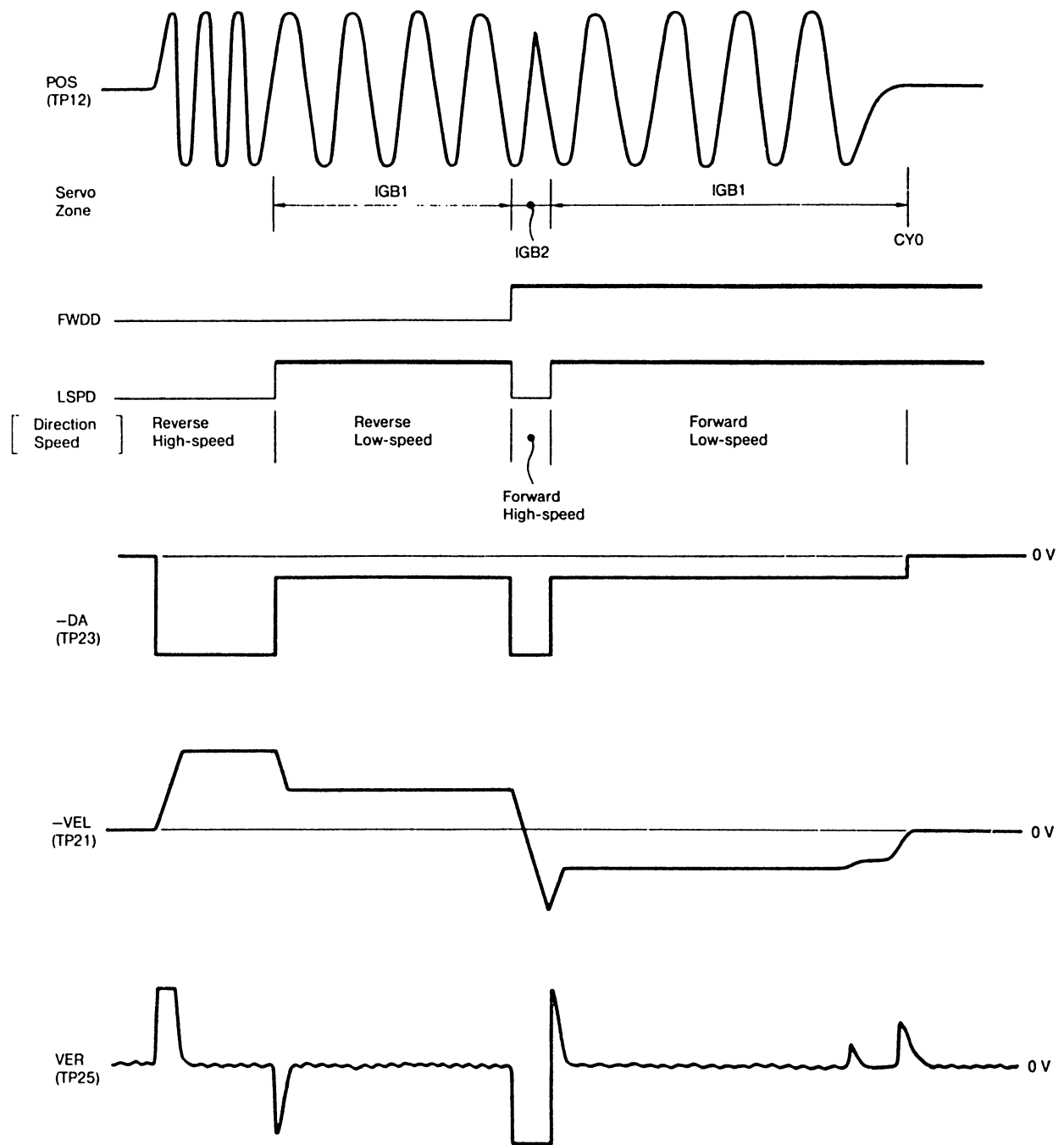


Figure 4.6.22 GTZ Target Velocity Generator

(p) **Clamp Gate**

The Clamp Gate circuit issues Minus Clamp Position (MCLMP), Plus Clamp Position (PCLMP) and Equal (EQUAL) signals through the adder circuit, which compares the two least-significant bits (NCAR2 and 1) of the target cylinder (NCAR2 and NCAR1) with PAR2 and PAR1 signals from the Position Decoder circuit.

(q) **Clamp Position Detector**

The Clamp Position Detector holds the position signal at specified levels when the servo head is positioned within three cylinders of the target cylinder address specified by the two least-significant bits of NCAR and PAR. This extends the area controlled by the servo circuit.

The PCLMP signal sets the Clamped Position Signal (CLPOS) to +2 V, the MCLMP is set to -2 V, and the EQUAL signal enables the FNPOS signal on the CLPOS signal.

The CLPOS signal is applied to the Velocity Error Detector circuit when the PSDR signal goes true at the termination of Seek operation, and is then applied to Low Pass Filter (LPF) when the servo head settles on the specified cylinder.

The timing chart of Clamp Position is shown in Figure 4.6.24.

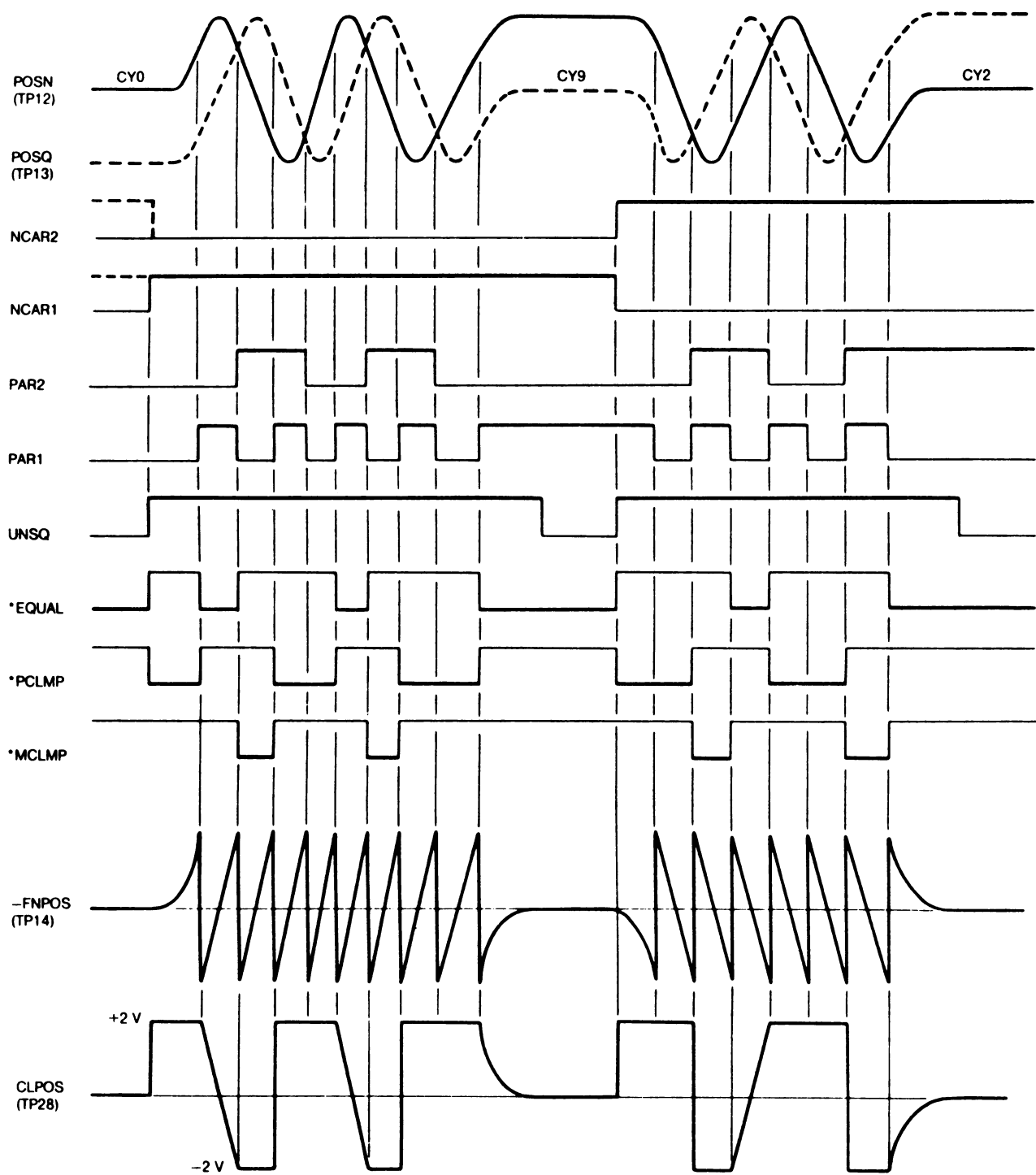


Figure 4.6.23 Clamp Position Timing Chart

- (r) **Low Pass Filter (LPF)**
The servo circuits form a feed-back loop during track following after a Seek operation using the position signal recovered from the servo head.
The LPF circuit attenuates unused high frequencies. The LPF has a resonance frequency at 1.9 KHz.
 - (s) **Position Error Detector**
The Position Error Detector pulls out the phase-compensated Position Error (PER) signal required for the feed-back loop during track following.
The PER signal is composed of a —FVEL (phase-compensating) signal, and an integrated position signal; improves stiffness and following characteristics of lower frequencies.
 - (t) **Power Drive Multiplexer**
The Power Drive Multiplexer circuit passes through either the VER signal, by activating DRLM signal during Direct seek or GTZ operation, or the PER signal, by activating the LNMD signal during track following sequence.
 - (u) **Power Amplifier Driver**
The Power Amplifier Driver circuit drives the last stage of the power amplifier. This circuit controls the base current to the power transistors by comparing the input signal with the feed-back signal from the last-stage transistor current.
 - (v) **Power Amplifier**
The Power Amplifier circuit is a current amplifier which drives the coil of the Voice Coil Motor (VCM). The circuit is composed of four H-type transistors.
 - (w) **Current Sense**
The Current Sense circuit detects the VCM coil current through the voltage bleeder resistors. The coil current is amplified by the differential mode, and then the Current Sense (CSNS) signal is issued.
 - (x) **VCM Heat Detect**
The VCM Heat Detect circuit senses an abnormal current flowing through the VCM.
- (2) **Direct Seek Servo Control**
During a Direct Seek with servo control, the servo head is driven high speed, so that the actual velocity pulled out from the position signal through the servo head is equal to the target velocity controlled by the Difference Counter. Whenever the servo head passes through a cylinder, the target velocity is decreased for optimum speed control. The Direct Seek signal flow is shown in Figure 4.6.25.
- (3) **GTZ Servo Control**
Wherever the head is positioned, GTZ Servo Control returns the head to Cylinder 0. The target velocity is given by the specified velocity, that is, high speed is 8 cm/second and low speed is 3 cm/second.
The GTZ signal flow is shown in Figure 4.6.26.
- (4) **Linear Mode Servo Control**
When the servo head is positioned within capture distance of the specified cylinder, the Servo Control mode is changed to Linear mode. During Linear mode (track following), the feed-back loop is formed to minimize the Position Error Signal.
When an Offset operation is performed, the offset voltage is applied to the Position Error signal through the DAC. The servo head is the offset by $\pm 3 \mu\text{m}$.
The Linear mode signal flow is shown in Figure 4.6.27.

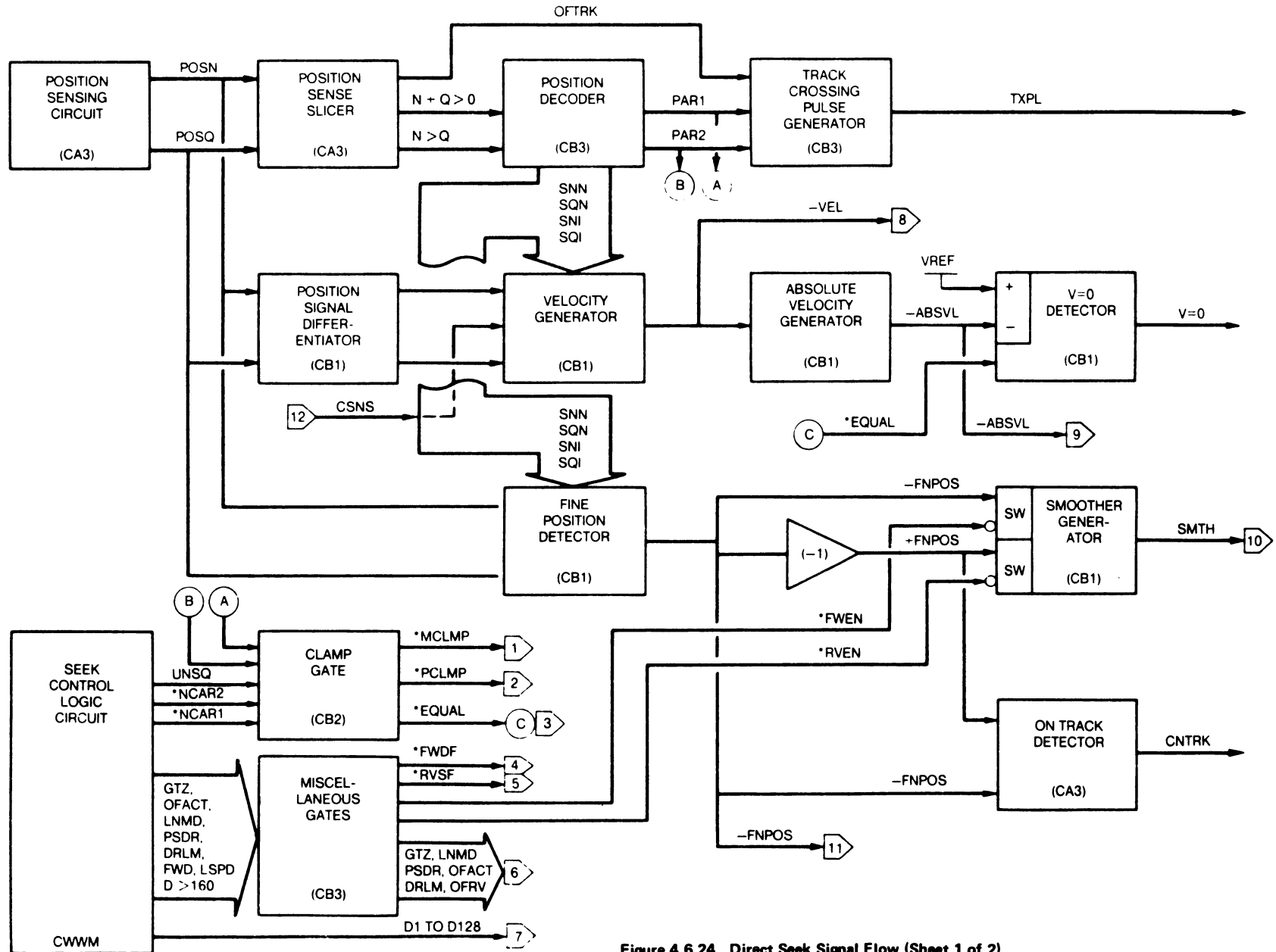


Figure 4.6.24 Direct Seek Signal Flow (Sheet 1 of 2)

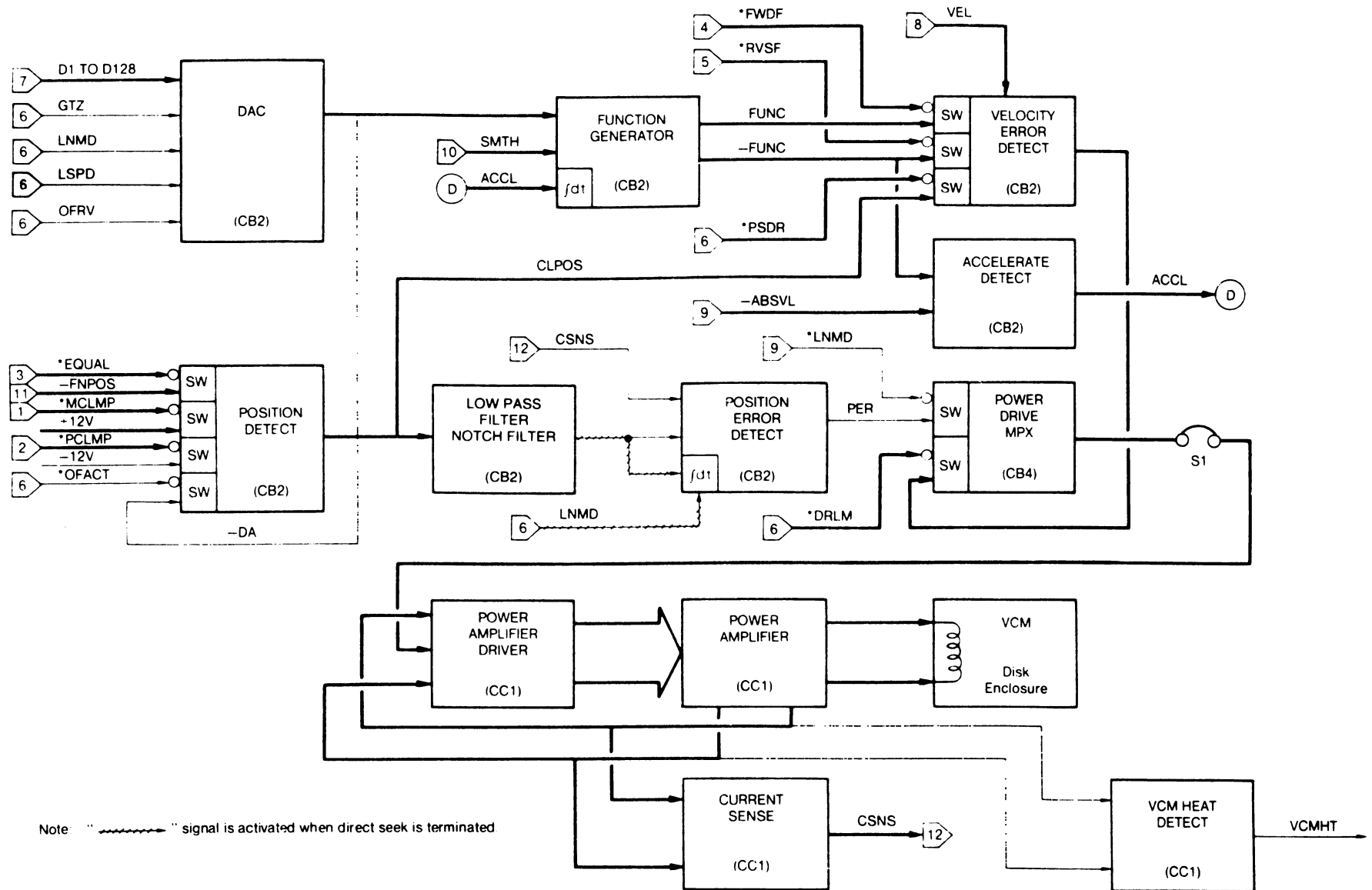


Figure 4.6.24 Direct Seek Signal Flow (Sheet 2 of 2)

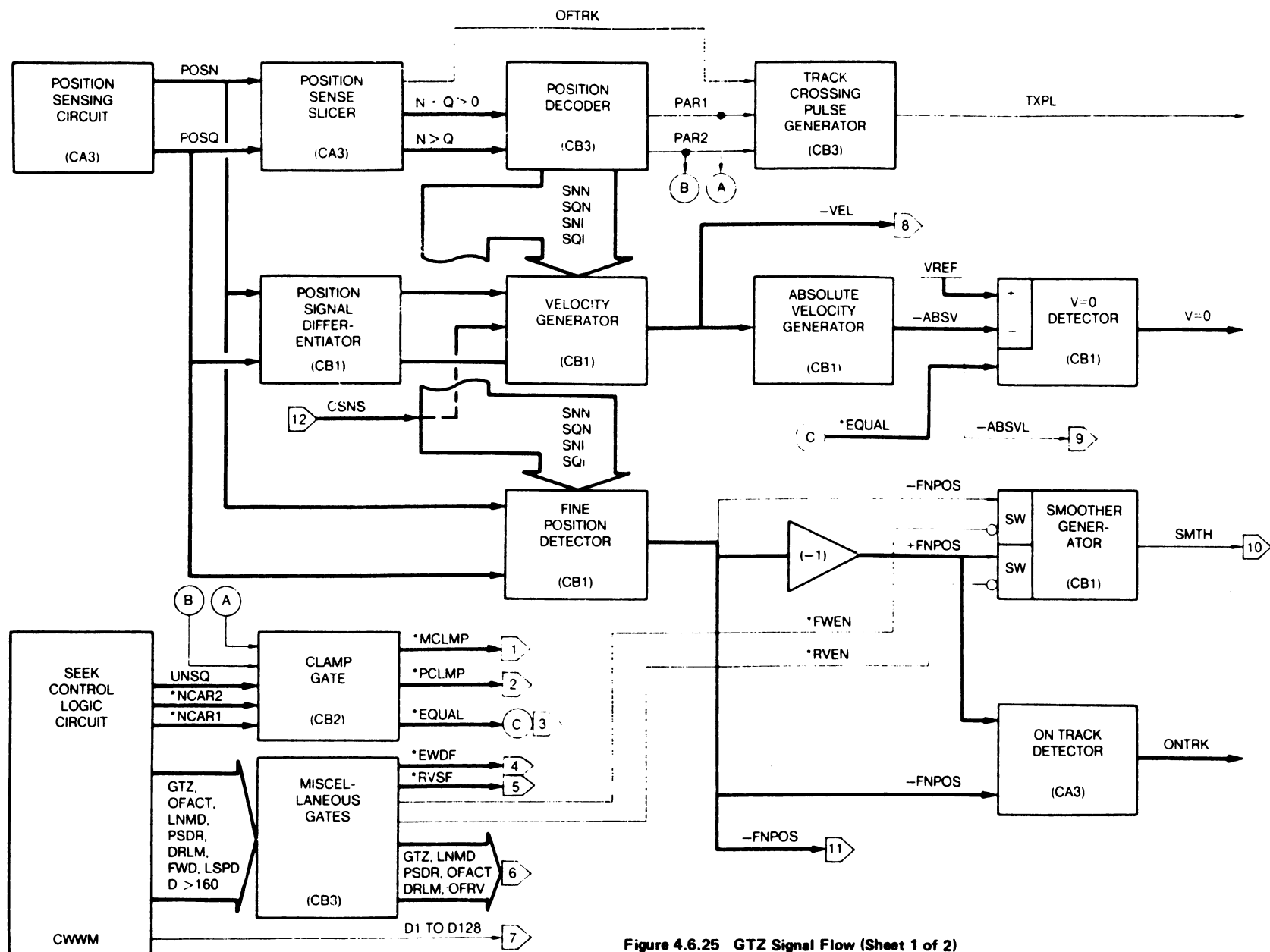


Figure 4.6.25 GTZ Signal Flow (Sheet 1 of 2)

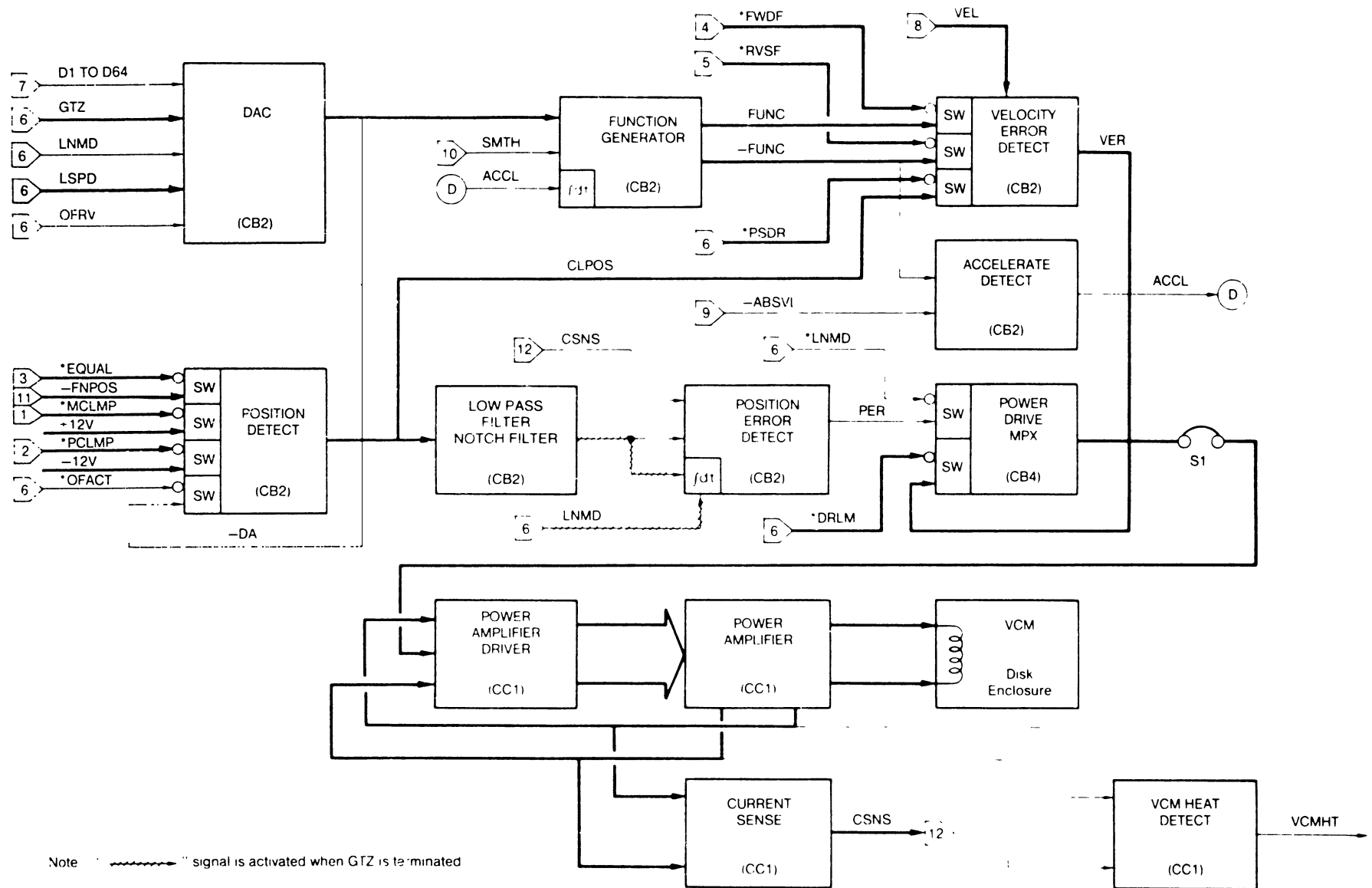


Figure 4.6.25 GTZ Signal Flow (Sheet 2 of 2)

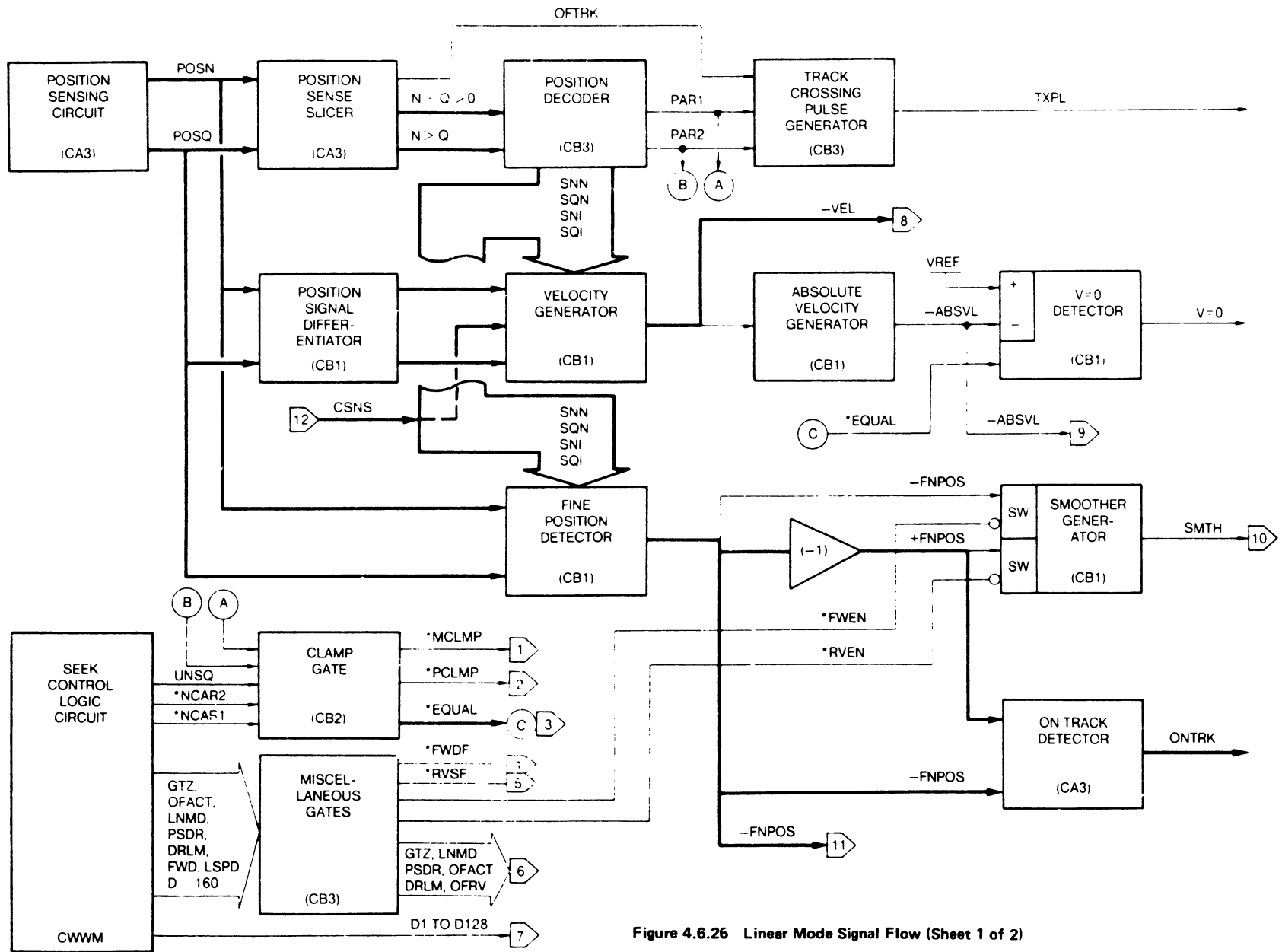


Figure 4.6.26 Linear Mode Signal Flow (Sheet 1 of 2)

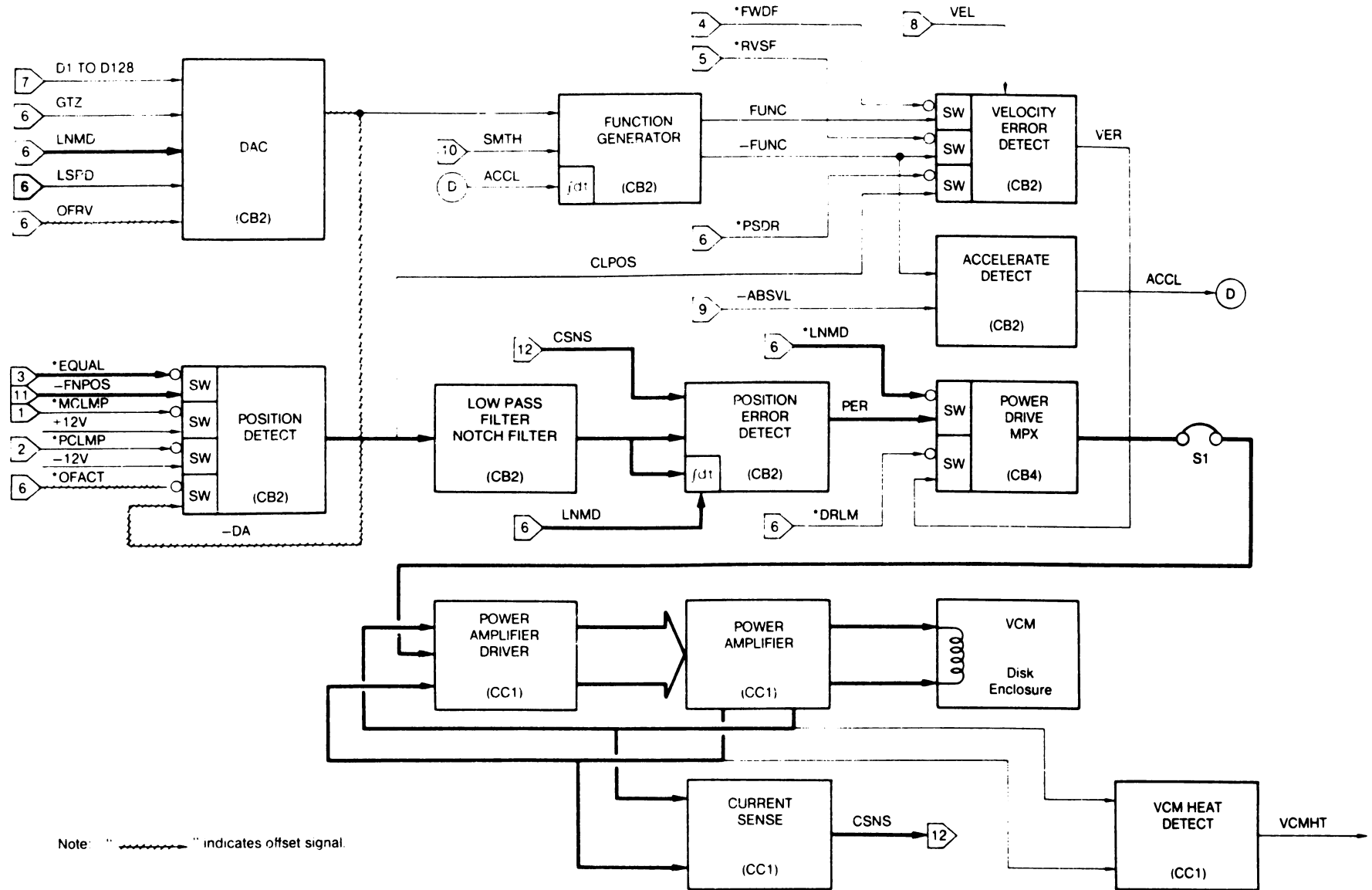


Figure 4.6.26 Linear Mode Signal Flow (Sheet 2 of 2)

4.6.4.3 Retract Servo Control

The Retract servo control block diagram is shown in Figure 4.6.28.

The Retract operation is initiated if Retract (RTR) signal goes true, a power failure occurs, or if Emergency Retract (EMRT) signal goes true.

The Retract signal controls the head movement so that the velocity sensed from the voltage output of the VCM is equal to the reference velocity.

In the case of a DC power failure, the normally used power amplifier is deactivated and the retract capacitor discharges through the VCM coil.

If excessive current flows through the VCM coil, the VCM Heat (VCMHT) signal turns on.

When the VCMHT signal is turned on, the seek control logic issues the Emergency Retract (EMRT) signal, which breaks a relay contact supplying DC+24V to the power amplifier. After breaking the relay contact, the retract capacitor discharges through the VCM coil.

Under above-mentioned conditions, the heads always return to the landing zone and are held there by the stopper magnet.

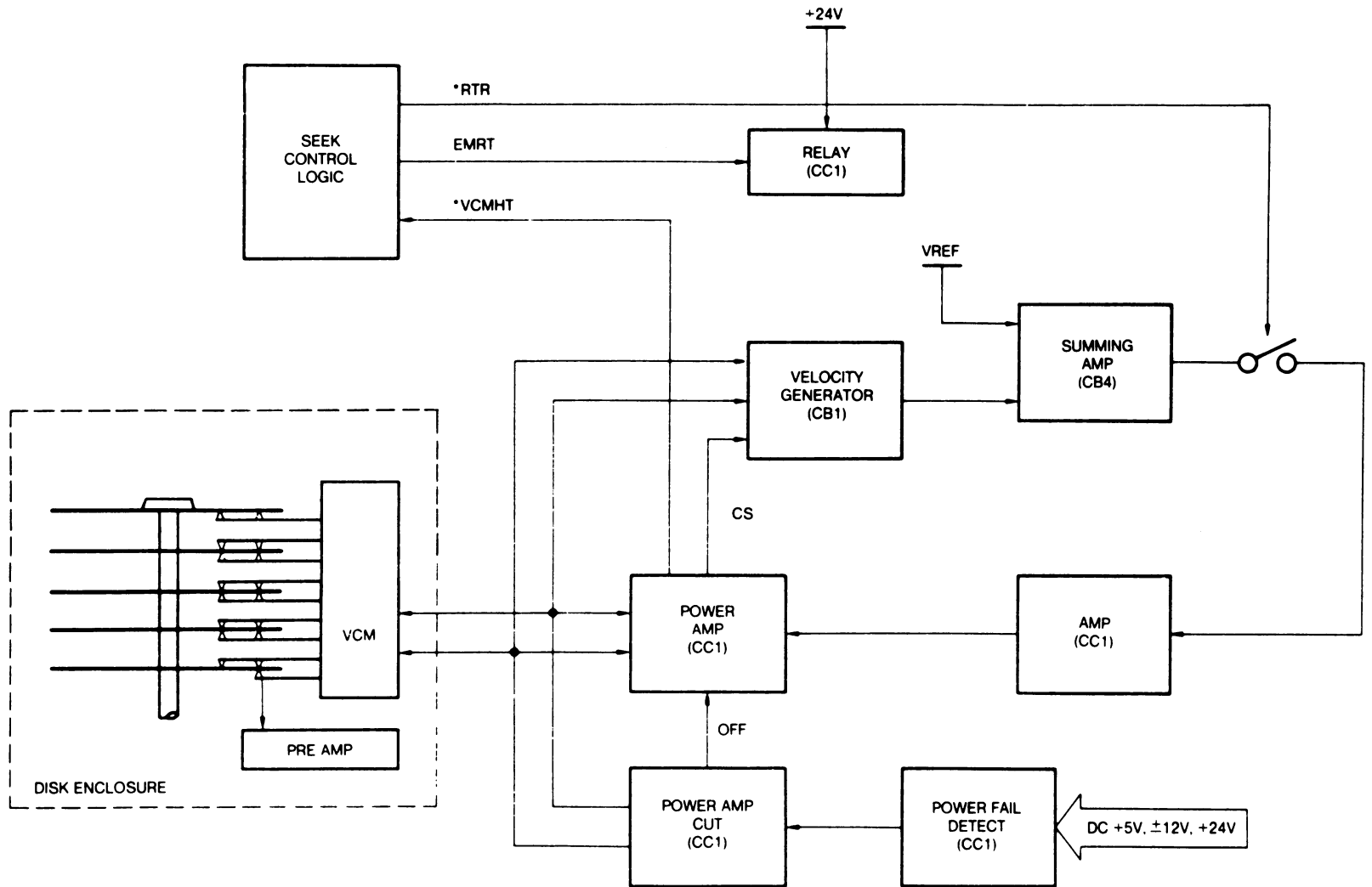


Figure 4.6.27 Retract Servo Control Block Diagram

4.6.5 Index/Sector/Guard Band Generate Function

4.6.5.1 Index Detect

As described in the Position Sensing discussion, the servo signal contains missing Sync Bits. The Servo Pulse (SVPLS) is applied to the Phase-Locked-Oscillator (PLO1) which outputs a 2 Bit Cell Clock ($PLO\frac{1}{2}F$).

The PLO1 latch (POLT) which is set by the leading edge of Servo Pulse and reset by the leading edge at Count 7 (CT7), is applied to a shift register and clocked by the positive going edge of the CT7 signal.

The shift register outputs are decoded into decimal, and then Index, two Inner Guard Band (IGB1, 2) patterns and Outer Guard Band (OGB) are detected by the combination of the decoder outputs. The index detect block diagram is shown in Figure 4.6.29 and the timing chart is shown in Figure 4.6.30 and Figure 4.6.31.

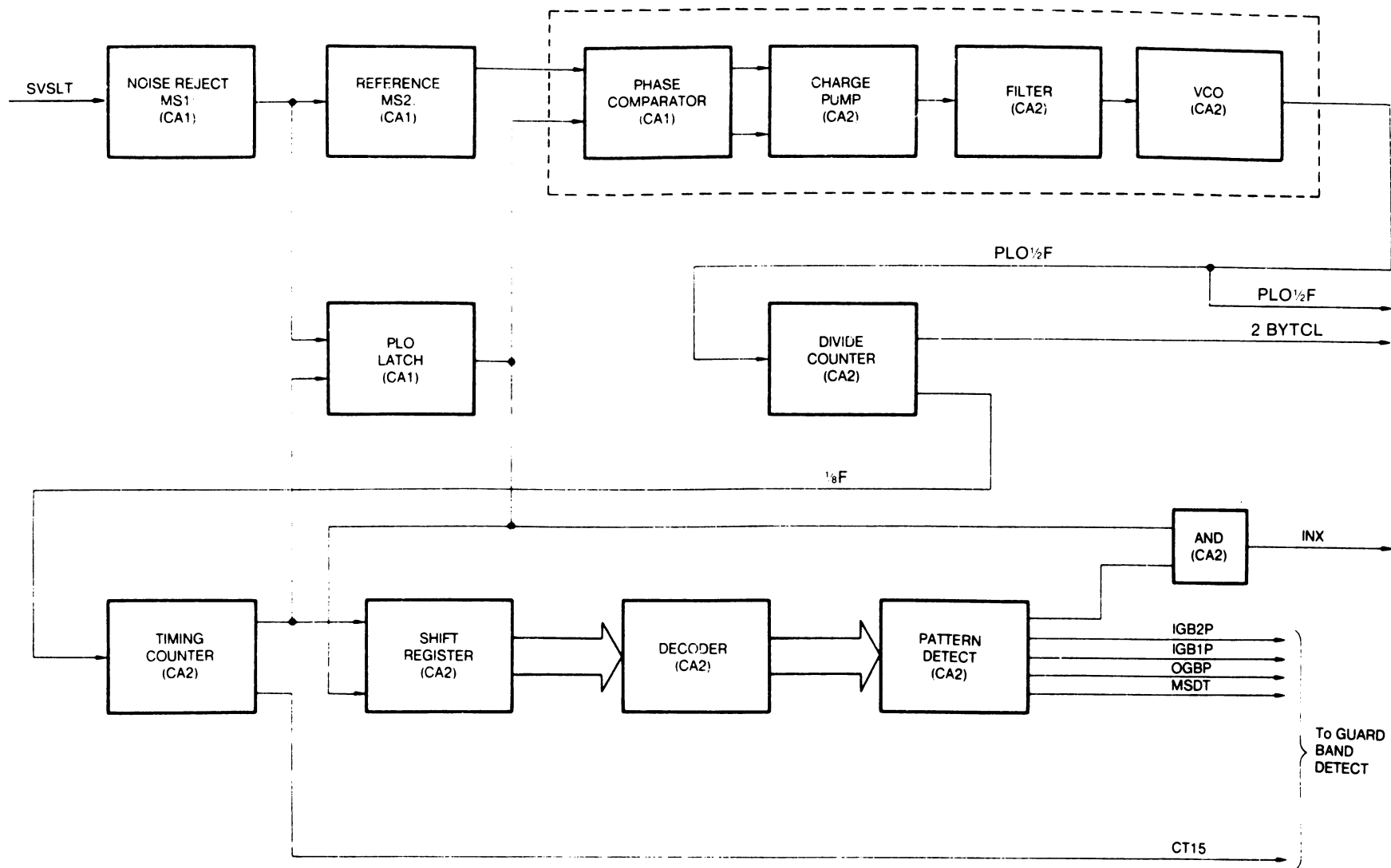


Figure 4.6.28 Index/Guard Band Patterns Detect Block Diagram

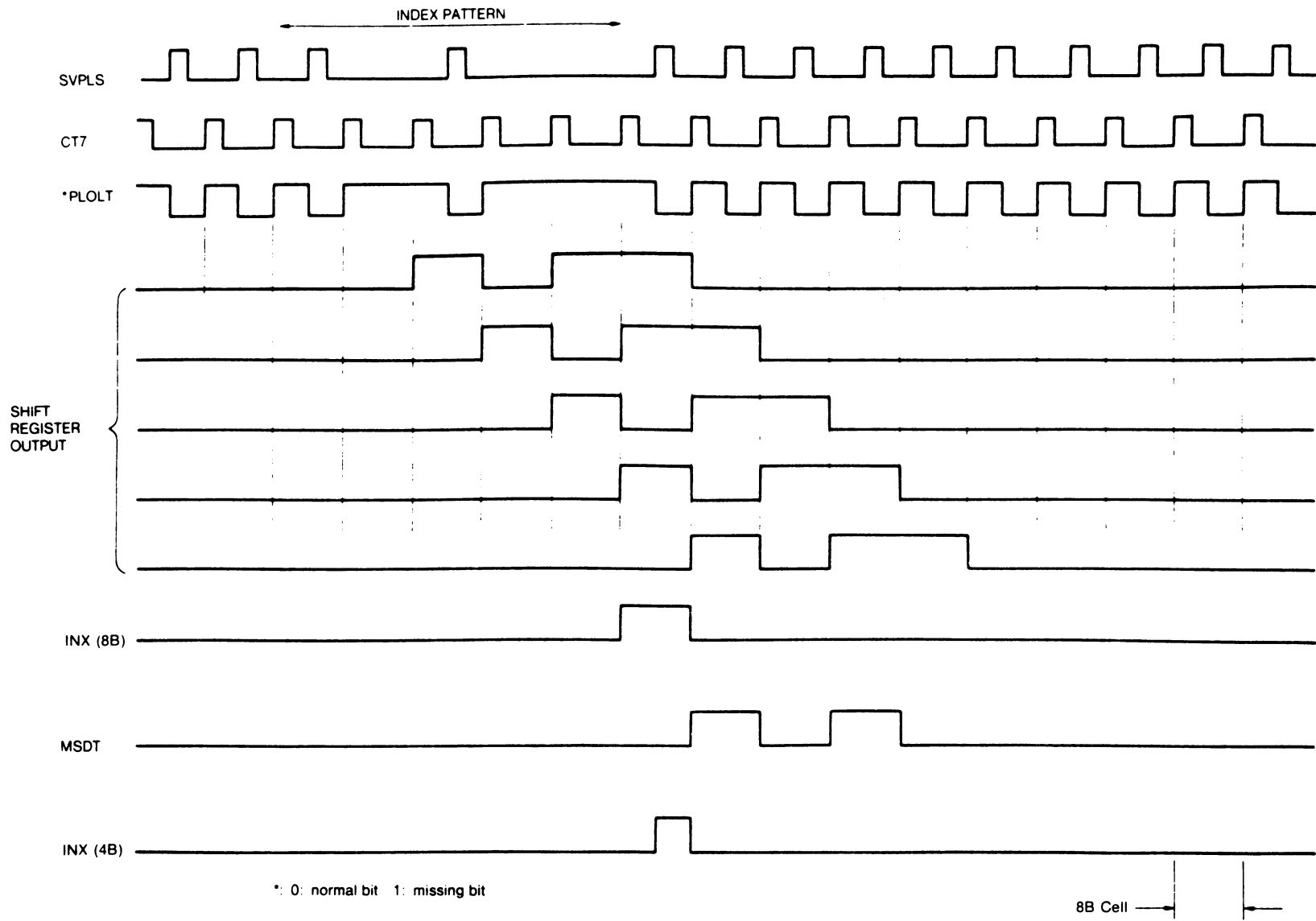


Figure 4.6.29 Index Detect Timing Chart

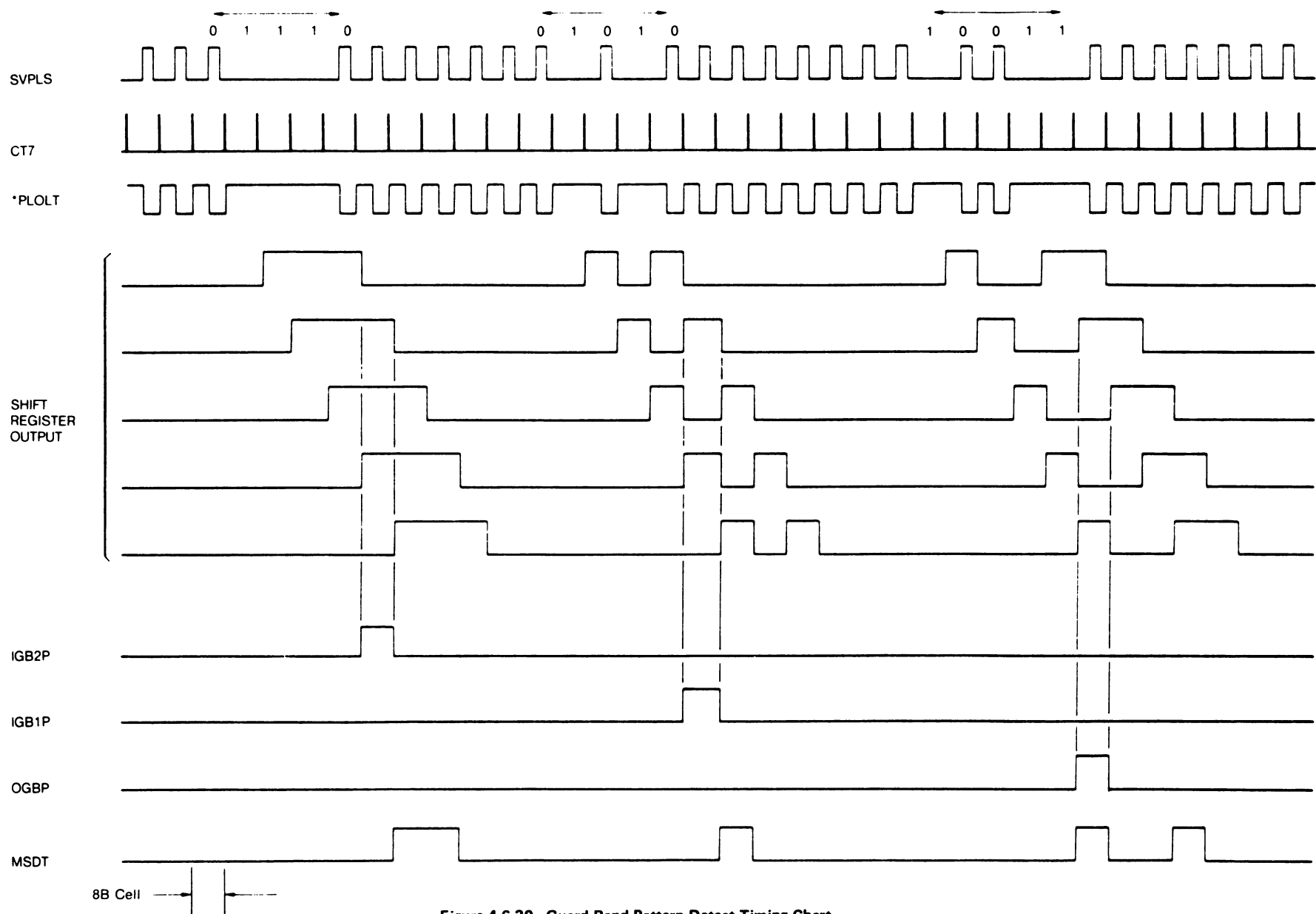


Figure 4.6.30 Guard Band Pattern Detect Timing Chart

4.6.5.2 Sector Generator

The sector pattern is not written on the servo surface. The sector pulse is derived from the Presettable Byte Counter by counting 2 Bytes clock, which is generated by the PLO circuit synchronized with Servo Pulse. One revolution has 40,960 Bytes clocks, and sector length is determined by keys on the VOIM PCB.

The Index signal (4 Bytes) from the PLO circuit enables the Preset Input to the Byte Counter. The value loaded into the Byte Counter is determined by the value of the VOIM PCB keys not turned on. For example, a 256 byte sector length is specified by turning on SW1 keys 1 to 7 and SW2 key 1. The binary value of the keys not turned on (SW2 keys 2 to 7) equals 65,280. The Index signal causes the Byte counter to be preset to 65,280. The counter is then clocked by the positive going edge of $\ast 1/16$ clock until it reaches 65,535 (510 byte clocks). The next $\ast 1/16F$ signal would then cause a carry signal which is used as the Sector Pulse and a new preset enable to the Byte Counter. The process is repeated until the Index signal goes true. Refer to Figure 4.6.32 and 4.6.33.

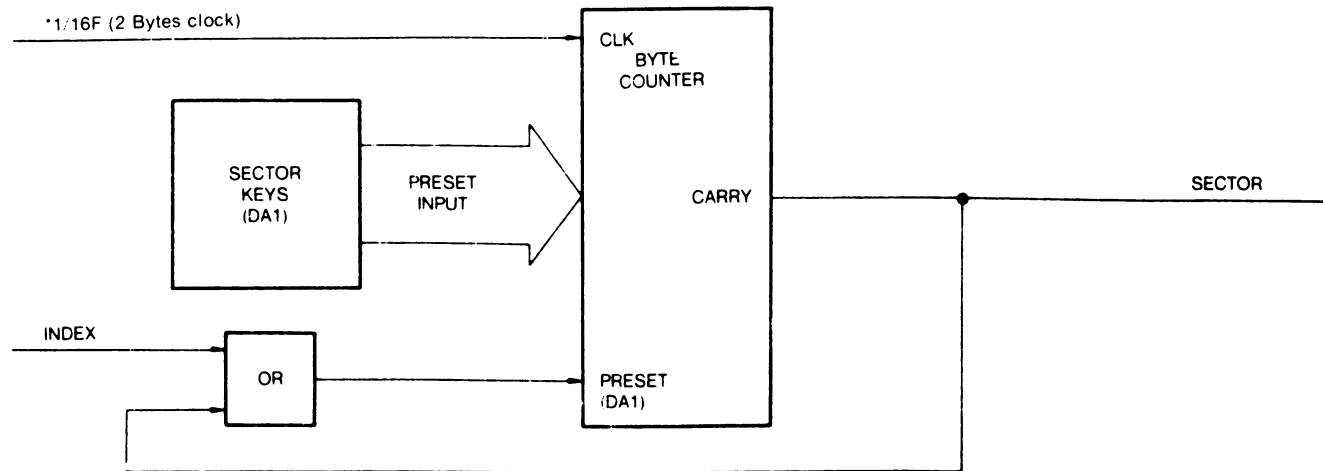


Figure 4.6.31 Sector Generating Block Diagram

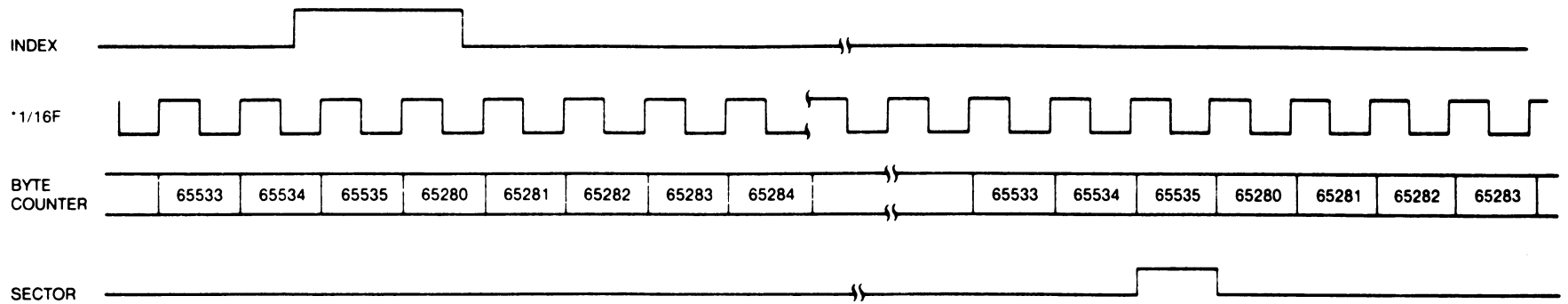


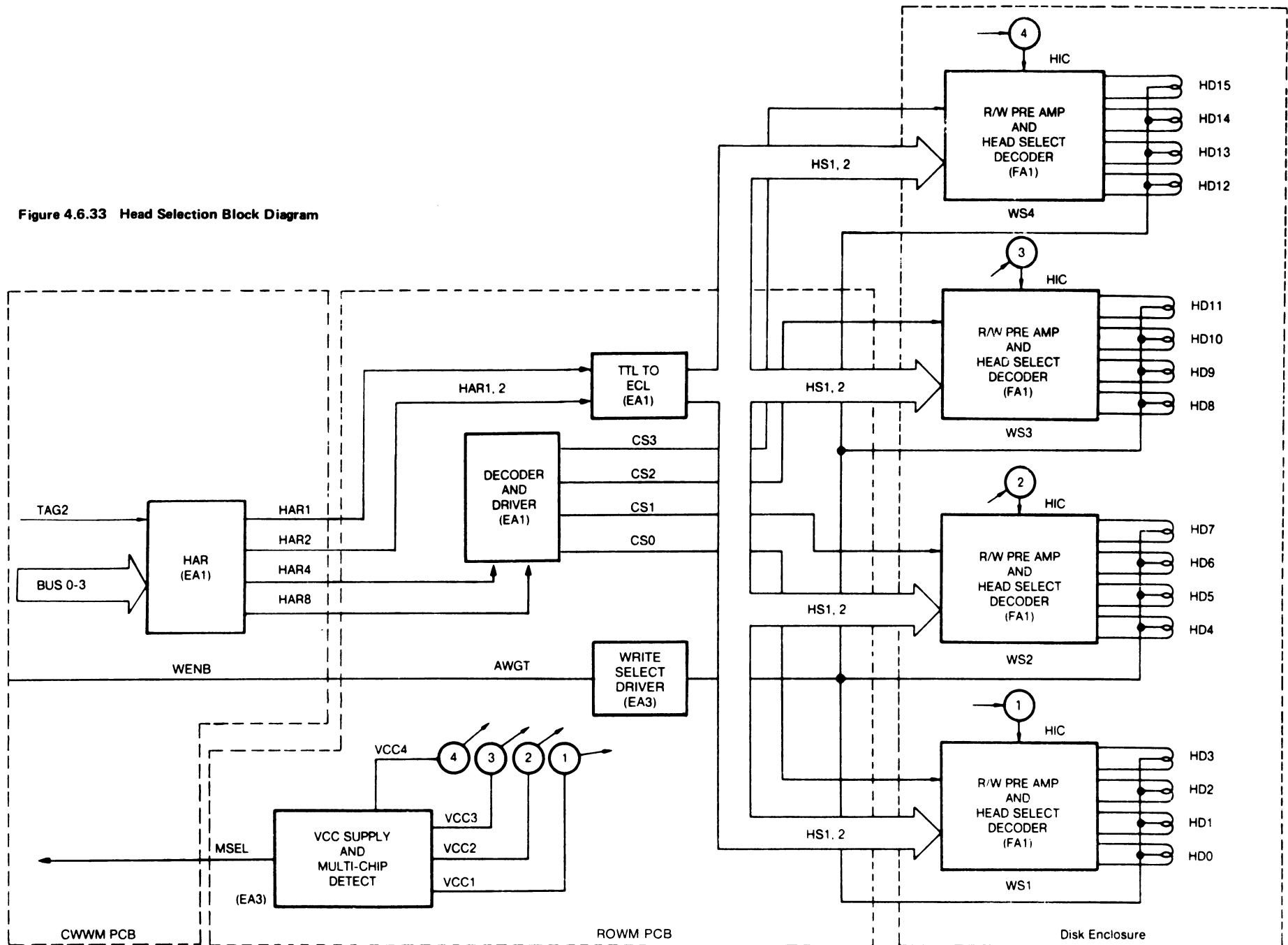
Figure 4.6.32 Sector Generating Timing Chart

4.6.6 Head Selection

A head must be selected before a read or write operation can be performed. The head address is set by the positive-going edge of the Tag 2 signal with Bus bit 0 to 3 at the Head Address Register (HAR). The HAR outputs, HAR1, 2, 4 and 8 signals, are applied to the ROWM PCB. The signals HAR4 and 8 are decoded into chip select 0 to 3 (CS0 to CS3 = ECL level) and then applied to head ICs in the disk enclosure. Lower bits HAR1 and 2 are converted into head select 1 and 2 (HS1 and HS2 = ECL level).

The multiple-chip select or head-short condition is detected by an overload current of Vcc supply. The block diagram of head selection is shown in Figure 4.6.34.

Figure 4.6.33 Head Selection Block Diagram



4.6.7 Read/Write Function

4.6.7.1 Read/Write Basic Principles

When the disk is rotating at 2,722 RPM, Read/Write is performed by means of the R/W heads. The basic principles of the read/write function will be described in the following paragraphs.

(a) Data Write

During a Write instruction, a 0 or 1 is recorded by reversing the direction of the current flowing in the data head coil. When the direction of the current flowing in the head coil is reversed, the magnetic poles of the head are reversed and the direction of magnetic flux at the gap is reversed. The direction of magnetization of the surface of the disk is then reversed. Each flux reversal means that a "1" or "0" has been recorded on the disk.

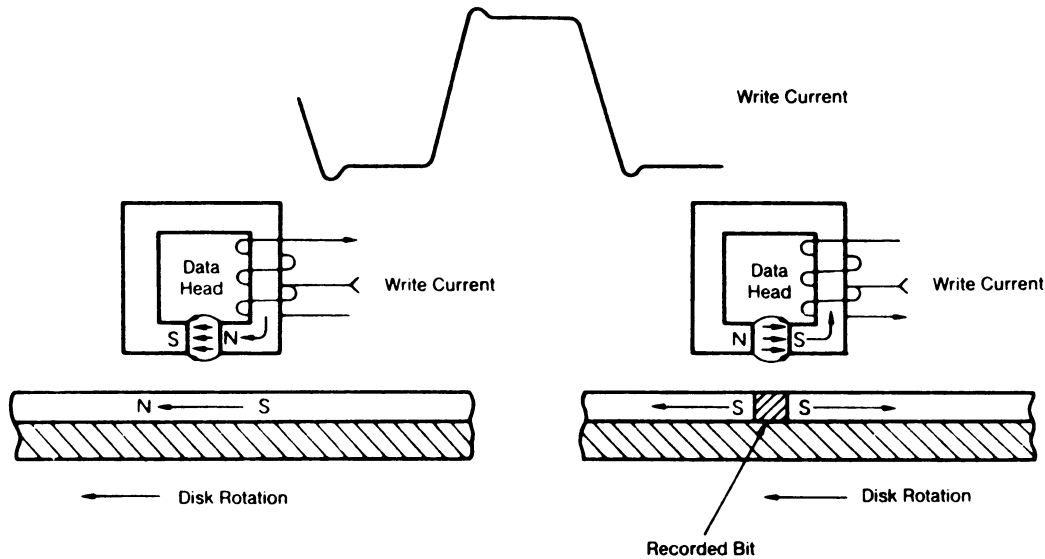


Figure 4.6.34 Data Write

(b) Data Read

During a Read instruction, the transitions recorded on the surface of the disk are detected by the head gap. When magnetized in the same direction continuously, no output is produced. However, when a recorded bit (180 degree flux reversal in the horizontal direction) passes under the head gap, the magnetic flux flowing in the ring and coil is reversed and an output pulse is obtained.

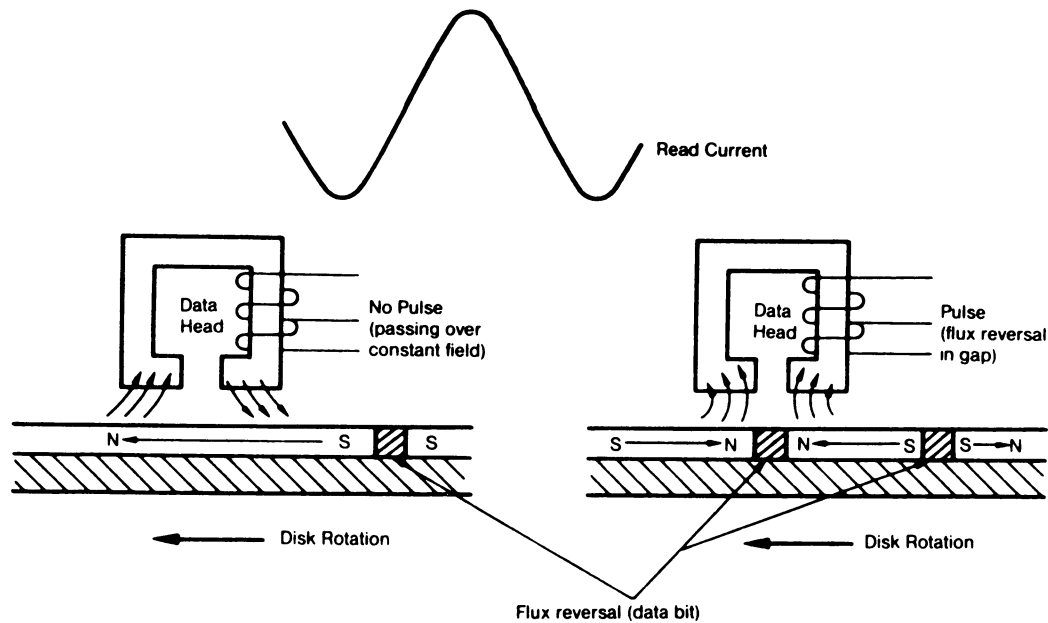


Figure 4.6.35 Data Read

- (c) The M2298 uses the 2-7 recording method. Since data is transferred between the controller and the disk drive unit by NRZ transmission, the NRZ data is converted to 2-7 data by an encoder in the drive, then recorded on the magnetic disk. In read operation, the recorded data in 2-7 code is read and converted to NRZ data by a decoder, then transferred to the controller.

The 2-7 code is a code of 4 to 8 bits in length converted from NRZ data of 2 to 8 bits in length according to the specified rule shown in Table 4.5.2. The 2-7 code contains continuous 0s from 2 to 7 between two 1s.

In the 2-7 code, the minimum code bit period is more than $1.5T$ (T indicates the data bit period) for any input data combination.

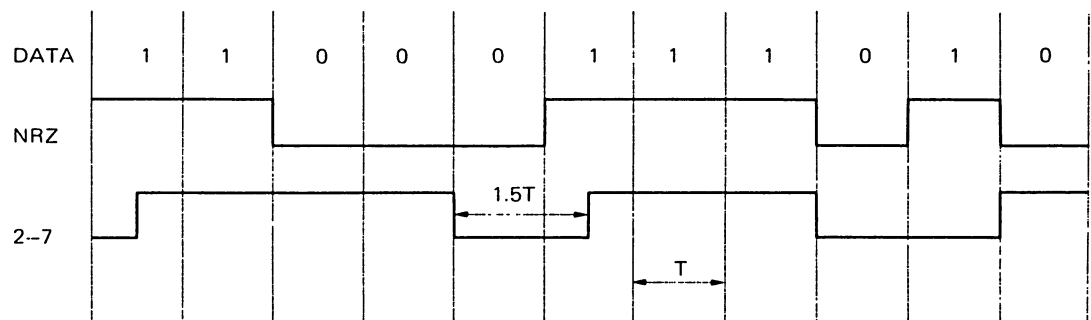


Figure 4.6.36 2-7 coding

Table 4.6.2 Translation Between NRZ and 2-7 Codes

NRZ Code words	2-7 Code words
1 0	0 1 0 0
0 1 0	1 0 0 1 0 0
0 0 1 0	0 0 1 0 0 1 0 0
1 1	1 0 0 0
0 1 1	0 0 1 0 0 0
0 0 1 1	0 0 0 0 1 0 0 0
0 0 0	0 0 0 1 0 0

4.6.7.2 Write Operation

The write circuit block diagram is shown in Figure 4.5.37. The servo data written on the disk are read by the servo head, and the PLO circuit generates 2 bit cell $PLO\frac{1}{2}F$ signal. The $PLO\frac{1}{2}F$ signal is applied to the VFO (variable frequency oscillator).

The VFO is synchronized with the $PLO\frac{1}{2}F$ signal and generates four times the frequency of the $PLO\frac{1}{2}F$; $VFO2F$ signal. $VFO2F$ signal is applied to the ENCODER circuit; $VFO1F$ is also sent to the control unit as the Read Write Clock signal. The control unit must use this Read Write Clock signal in the case of Write Clock (WCLK) and Write Data (WDAT) generation.

When a write command is issued from the control unit after head selection, the WDAT and WCLK signals are sent to the disk drive, and the WDAT signal is clocked by the positive-going edge of WCLK signal.

The clocked WDAT signal is applied to Encoder circuit, WDAT of NRZ code is converted into Encode Write Data (ENCWD) of 2-7 code, (refer to Table 4.5.2), and circuit is converted into Write Data Pulse (WDP).

When the Write Gate signal goes true, the WDP signal is toggled by a flip-flop and passes through the Read/Write Bus Switch IC. It is then applied to the Head IC (HIC) chips as Data X (DX) and Data Y (DY) signals. The write current is supplied to the selected HIC chip through a Write Current (WC) line.

The block diagram of write operation is shown in Figure 4.5.37.

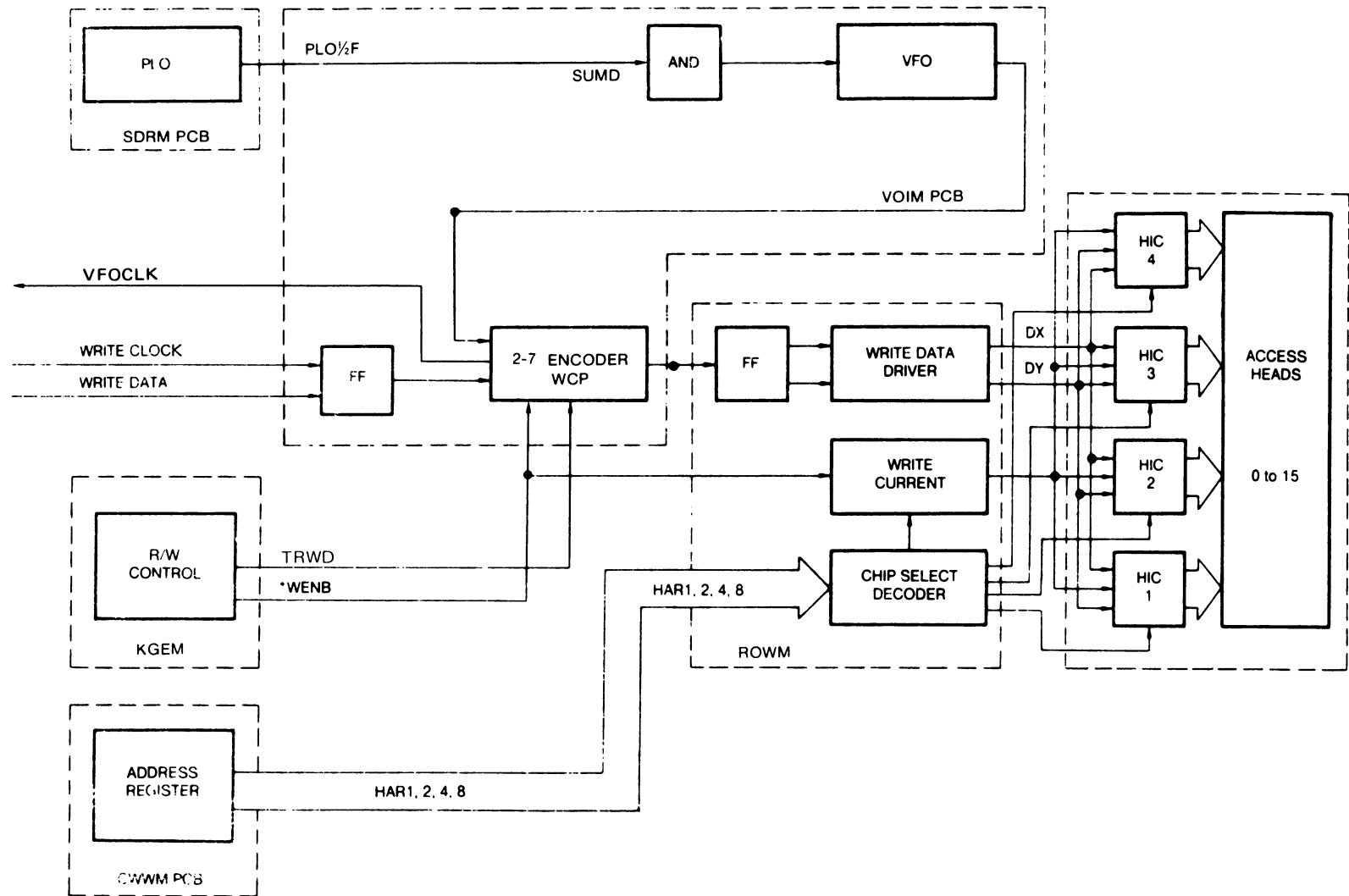


Figure 4.6.37 Write Operation Block Diagram

4.6.7.3 Write Compensation

When the bit density (BPI) is high on a disk surface, and a read operation is performed, a peak shift phenomenon appears, which tends to widen the narrow part of the bit spacing because of mutual magnetic interference of the bits. When such a phenomenon appears, reading of the data will deviate from the correct bit spacing, causing errors. The write compensation circuit measures this peak shift beforehand so the data is written by shifting the peak in the opposite direction of the peak shift appearing during the read operation.

The NRZ write data (WDAT) sent from the control unit is clocked by the positive-going edge of the WCLK signal. It is then synchronized with the internal one-bit cell clock (CLKA) which is issued from the sync decision window circuit, comparing the phase difference between *WCLK and VFO2F by enabling the Write Enable (WENB) signal.

The NRZ data synchronized with the internal clock is applied to 2-7 encoder circuit. The output of the 2-7 encoder circuit is applied to six-bit shift register. Each output of the six-bit shift register is applied to a write compensation circuit and then converted into 2-7 data pulse train with write compensation according to the truth table (as shown in Table 4.5.3). The preshift timing of write compensation is defined by Early (EY), on-Time (OT) and Late (LT) signals.

The block diagram and timing chart are given in Figure 4.5.38 and Figure 4.5.39.

Table 4.6.3 Write Compensation Truth Table

REGISTER STATUS			WRITE COMP			2-7
ENCWD	ESR2	ESR5	EY	OT	LT	DT
1	1	1	0	1	0	1
0	1	1	1	0	0	1
0	1	0	0	1	0	1
1	1	0	0	0	1	1
*	0	*	*	*	*	0

Note: EY: Early Pulse
OT: On-Time Pulse
LT: Late Pulse
DT: Data Pulse

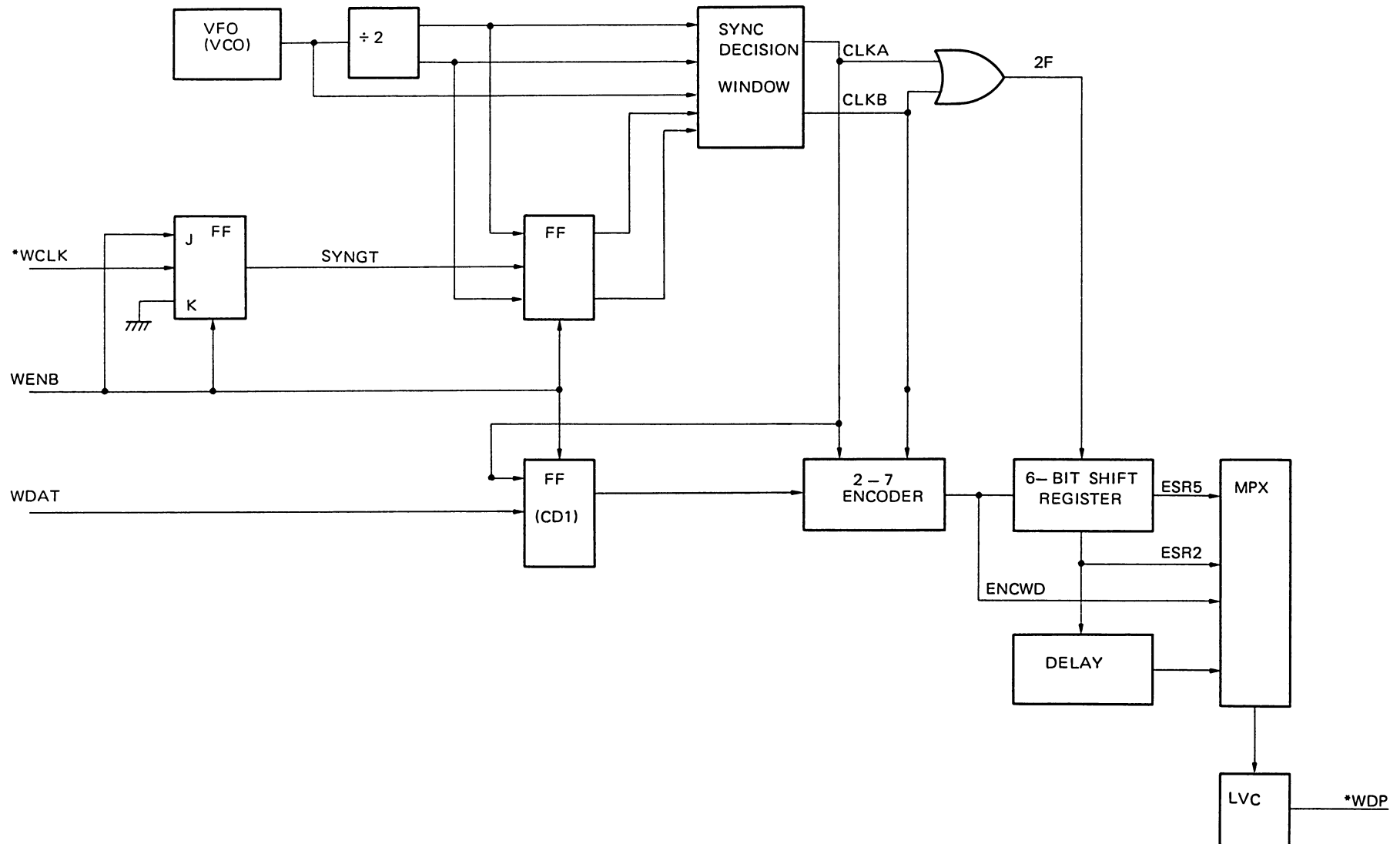


Figure 4.6.38 2-7 Coding, AM Write and Write Compensation Block Diagram

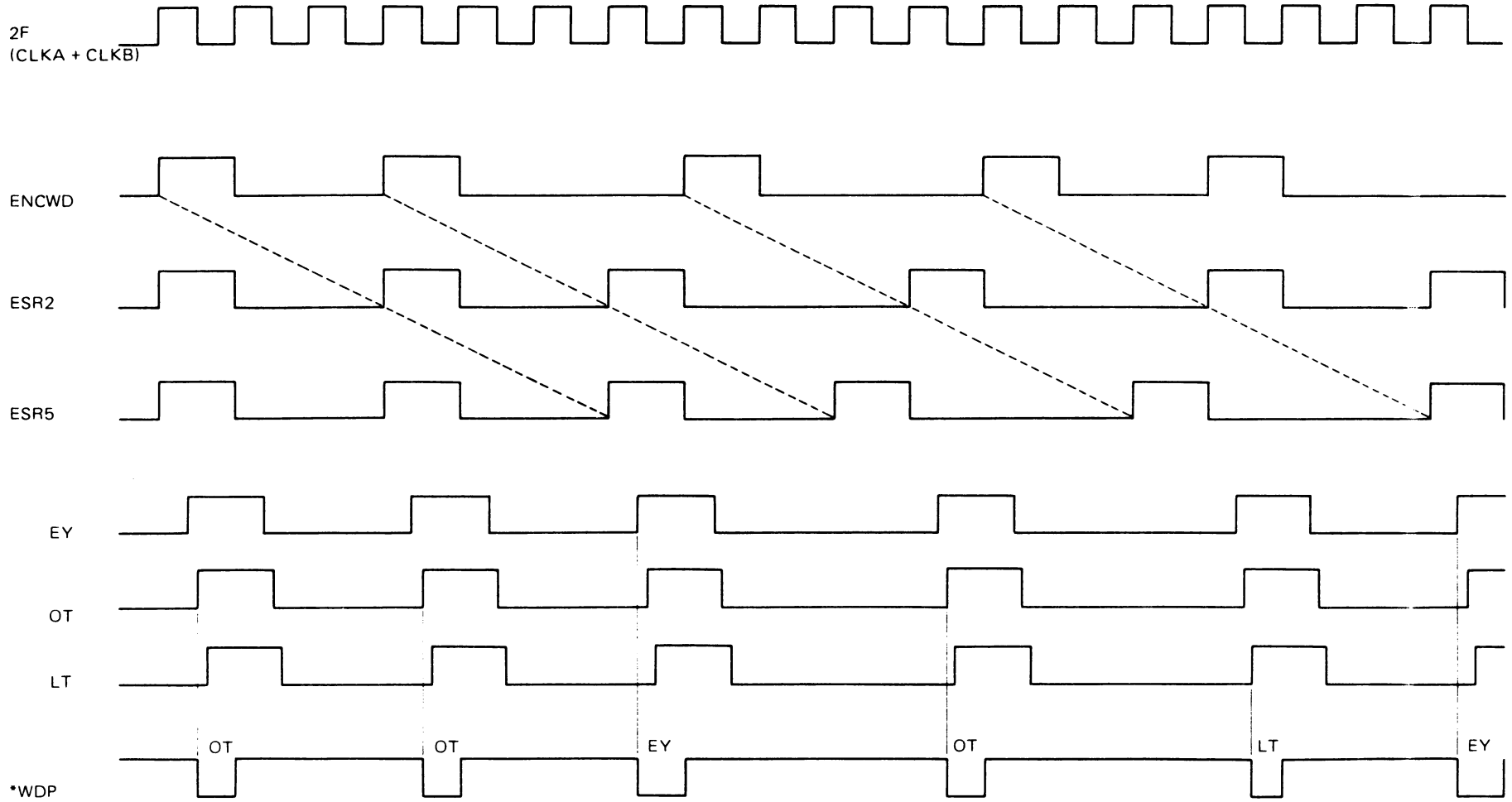


Figure 4.6.39 Write Compensation Timing Chart

4.6.7.4 Read Operation

A Read operation is initiated by enabling Tag 3 and Bus 1 (Read Gate: RG); however, the read analog circuit is enabled by disabling Write Enable (WENB).

The DX, DY HIC outputs are applied to the Read/Write Bus Switch circuit, amplified, and sent to the Low Pass Filter (LPF) (refer to Figure 4.6.42).

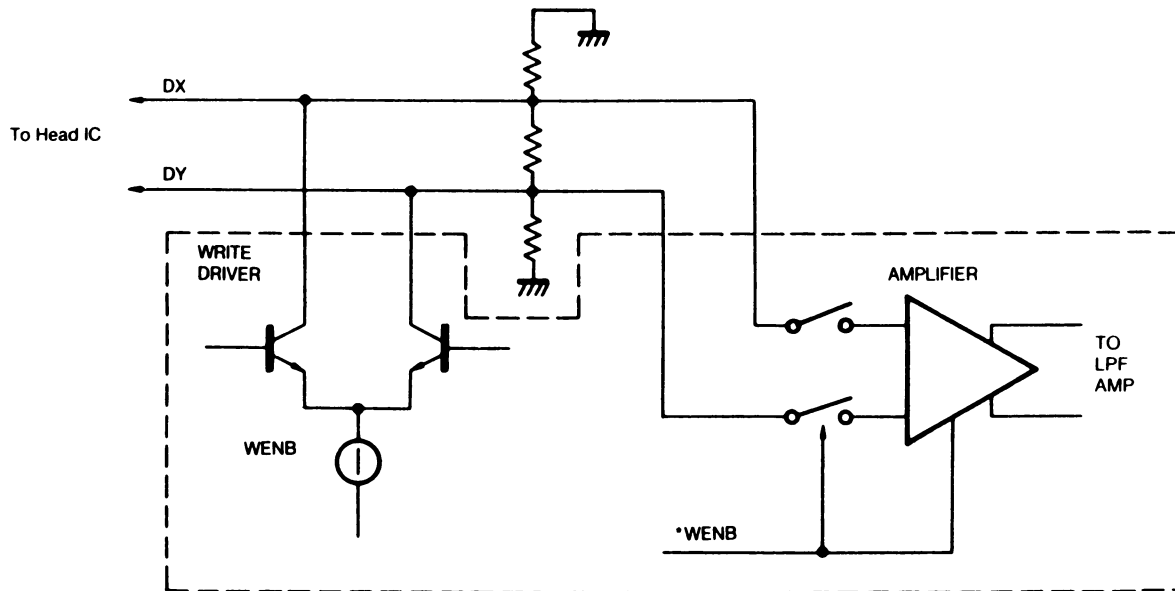


Figure 4.6.40 Read/Write Bus Switch

The output of the Read/Write Bus Switch is applied to a LPF circuit to attenuate the useless high frequency noise, and sent to the Automatic Gain Control (AGC) circuit.

The AGC circuit develops the control voltage to the AGC amplifier and holds the AGC output amplitude (300 mVp-p) at a constant level. The output of the AGC amplifier is amplified by ten amplifications (3.0Vp-p), and then sent to the Pulse Shaper circuit.

After going false at WENB, the read circuit is activated; however, a read-transient which is caused by the DC unbalance of the read pre-amplifier will occur. WENB signal squelches this read transient (refer to Figure 4.6.43).

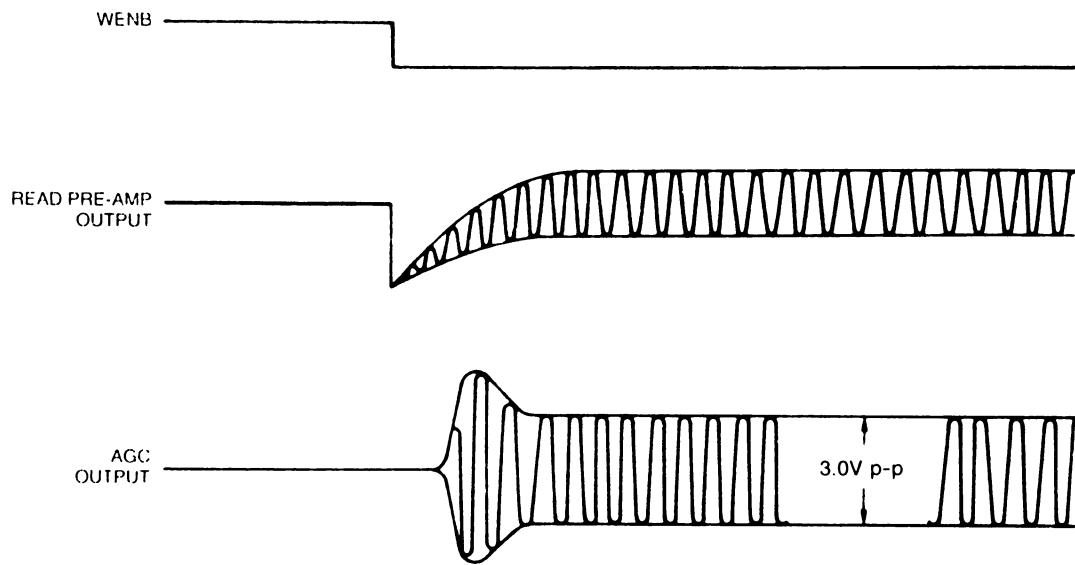
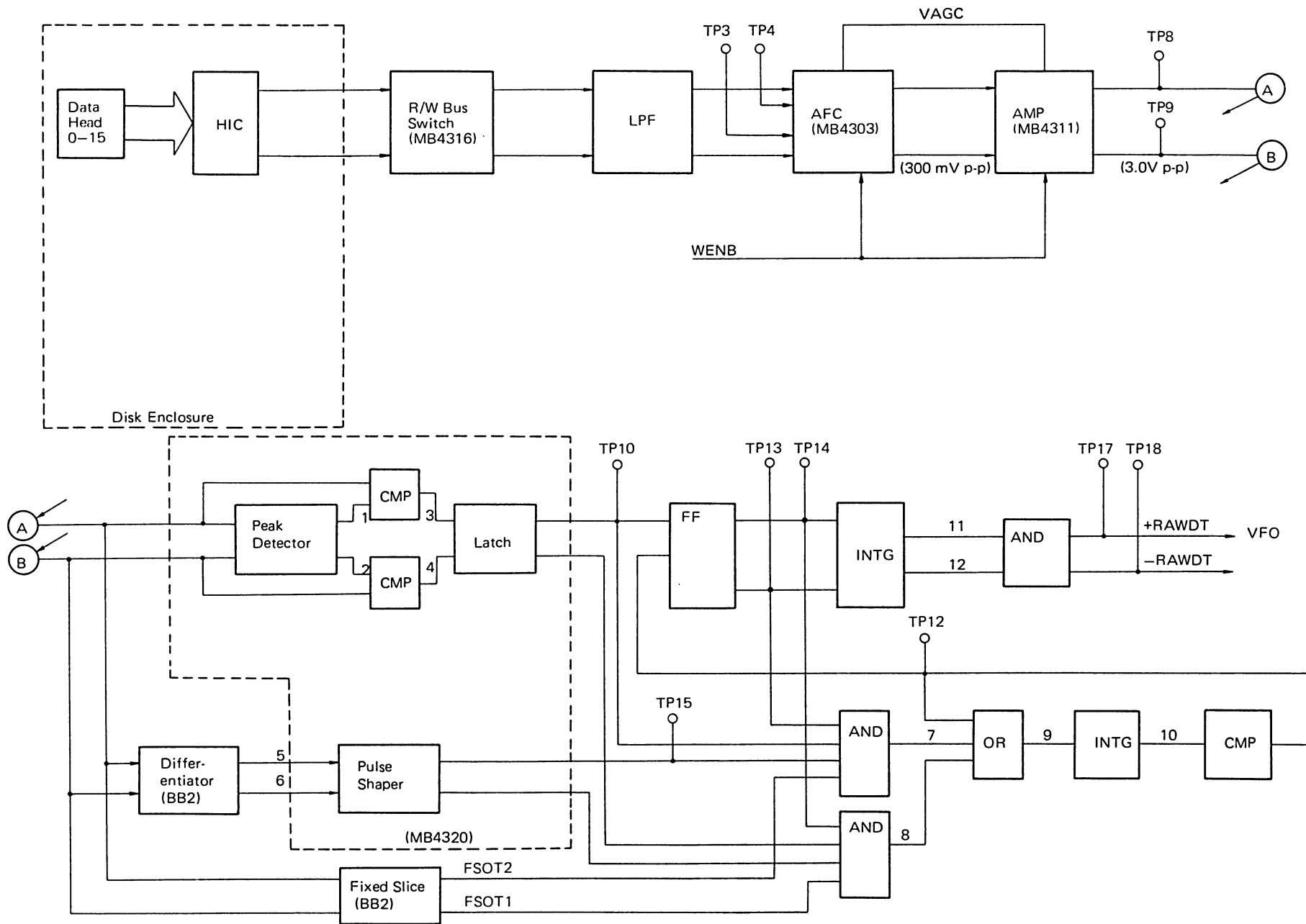


Figure 4.6.41 AGC Squelch Function

The analog to digital convertor circuit, which is called a Pulse Shaper, has two fundamental circuits. One is a Differentiator circuit which differentiates the AGC output signal and then converts the peaks (flux transitions) into zero-crossing signals. The other is an Integrator circuit which AC-slices the AGC output signal (floating slice) and then generates the data window for the 217 read data pulse. The block diagram is shown in Figure 4.6.45 and the detail timing chart is shown in Figure 4.6.46 and 4.6.47.

The output of the analog to digital convertor which is Raw Read Data (RRD 1/2), is sent to the VFO circuit.



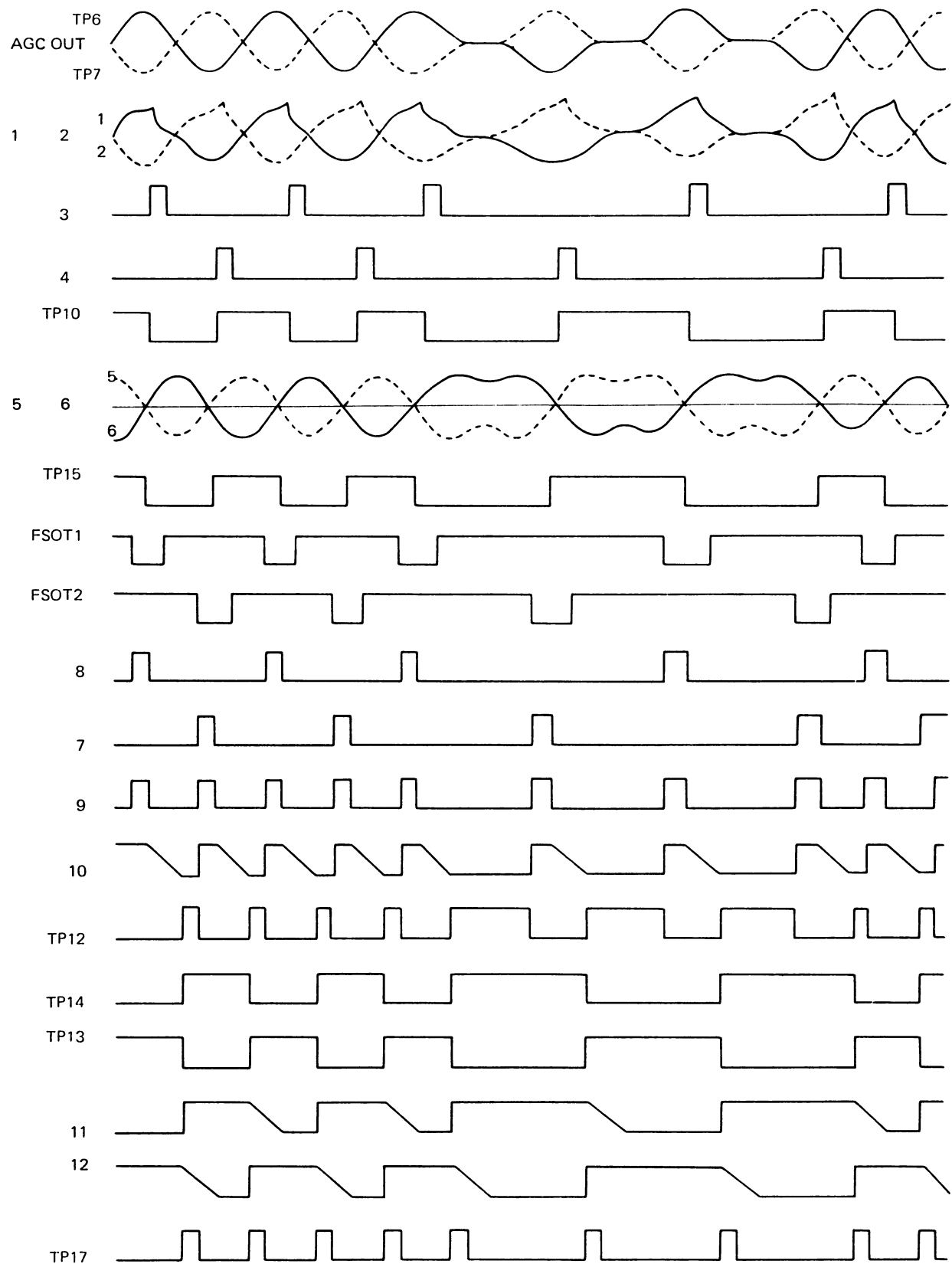


Figure 4.6.43 Read Data Analog to Digital Timing

4.6.8 VFO

4.6.8.1 VFO

The Variable Frequency Oscillator (VFO) output is synchronized with $PLO\frac{1}{2}F$ signal from the servo information during non-read operation, and with the Raw Data (RAWDT) signal from the data track during a read operation. The block diagram of the VFO circuits is shown in Figure 4.5.44.

The VFO are composed of the following circuit.

- (1) VFO Input Multiplexer
- (2) Time-Margin Measurement (TMG) One-Short
- (3) Reference One-Shot
- (4) Phase compare Latch
- (5) Phase Comparator and Charge Pump
- (6) Low Pass Filter and Buffer
- (7) Voltage Controlled Oscillator (VCO)

(1) VFO Input Multiplexer

The VFO input multiplexer controls the VFO input. During an initial seek operation or a RTZ operation, this circuit inhibits an input of data into the VFO circuit by enabling the Filter Squelch (FLTSQ) signal. This causes the VCO to oscillate at a free-running frequency. After an initial seek operation or a RTZ operation, the VFO Input multiplexer controls the transmission of the $PLO\frac{1}{2}F$ or RAWDT signals into the VFO circuit.

During a non-read operation, the $PLO\frac{1}{2}F$ signal is applied to the VFO circuits by the enabling of the Servo Mode (SVMD) signal. During a read operation, the RAWDT signal is applied to the VFO circuits by disabling the SVMD signal. The VFO input multiplexer output, Data Input 1 (DTIN1), is applied to the TMG One-shot circuit.

(2) TMG One-shot

The TMG One-shot circuit issues a Data Input 2 (DTIN2) signal to the Phase Comparator, and Reference One Shot circuit. It also issues Delayed Data (DLDT) signal to the Data Window circuit. The timing relation between DTIN2 and DLDT signals adjusted by potentiometer RV3 determines the read margin. (Refer to Figure 4.5.46)

(3) Reference One-shot

The leading edge of the DTIN2 signal triggers the Reference One-shot, which issues a 17 ns Reference Pulse (REFP) signal to the Phase Comparator Charge Pump circuit.

(4) Phase-Compare Latch

The leading edge of the DTIN2 signal sets the Phase-Compare Latch and the negative-going edge of $-2F$ Clock ($-2F$ CLK) resets it. The Phase-Compare Latch issues a Phase-Compare Latch Output (PCLO) signal to the Phase Comparator Charge Pump circuit.

(5) Phase Comparator and Charge Pump

The Phase Comparator Charge Pump circuit issues a Decrease frequency (DEC) signal when the VFO input phase is lagging, and an Increase frequency (INC) signal when the VFO input phase is leading, comparing the phases between DTIN2 signal and PCLO signal.

The INC or DEC signal drives the constant-current circuit to charge or discharge the filter circuit (LPF and Buffer).

(6) LPF and Buffer

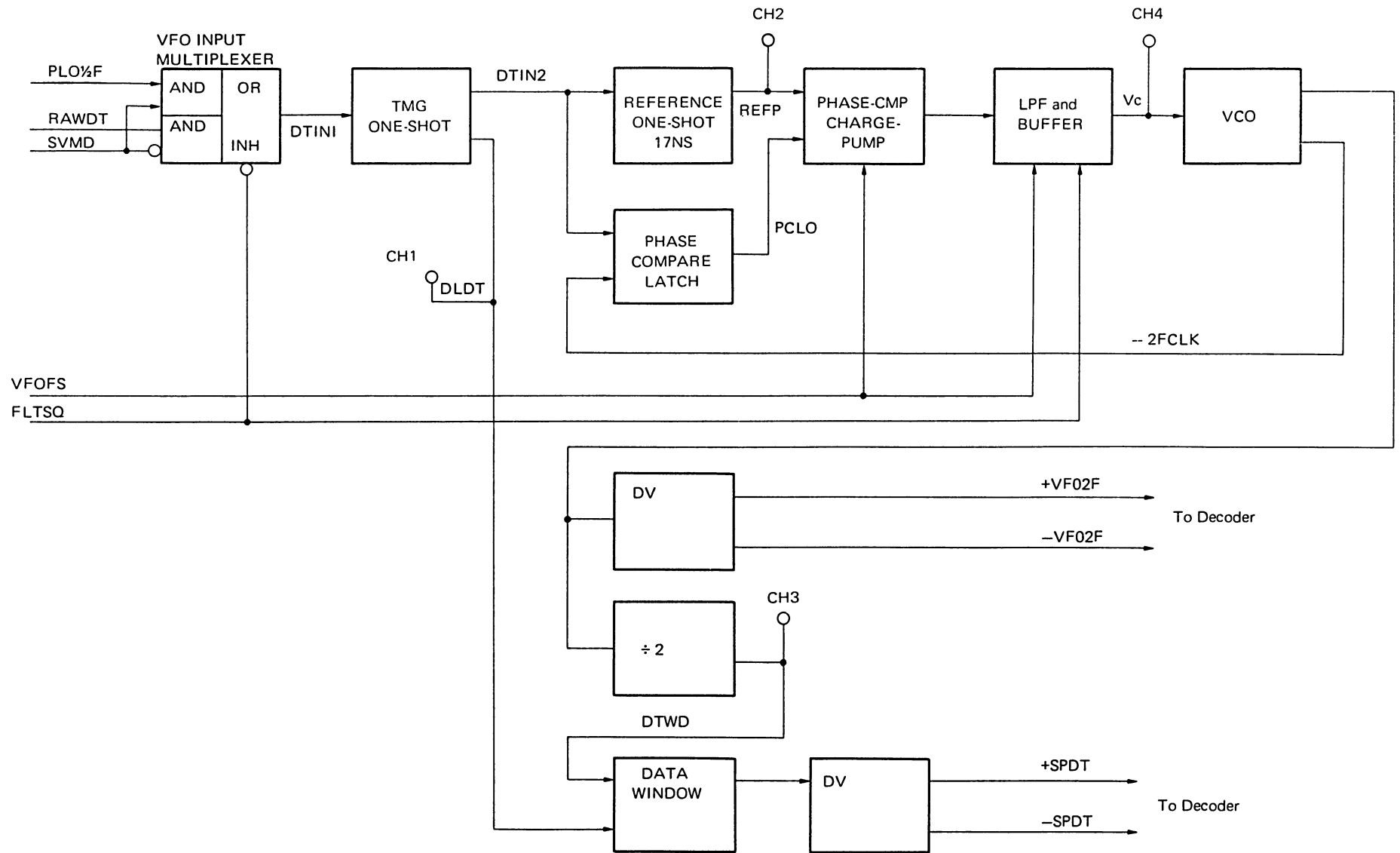
The charge pump output is applied to a Low Pass Filter (LPF) and converted into DC voltage to control the VCO. During an initial seek operation or RTZ operation, the FLTSQ signal clamps the charge pump output to 0V to recalibrate the VFO function.

During an initial data read operation, a VFO Fast-Sync (VFOFS) signal is issued to the VFO circuit which increases the loop gain of the VFO circuit to widen the pull-in range, and to shorten the pull-in time for synchronization to the RAWDT signal. At termination of the data read operation, the same function is activated for synchronization with the $PLO\frac{1}{2}F$ signal.

The LPF and Buffer output is applied to two stages of an emitter-follower circuit. It controls the VCO frequency as a Control Voltage (V_c) signal.

(7) Voltage Controlled Oscillator

The VCO issues ECL level output. Refer to Table 8.3.3.



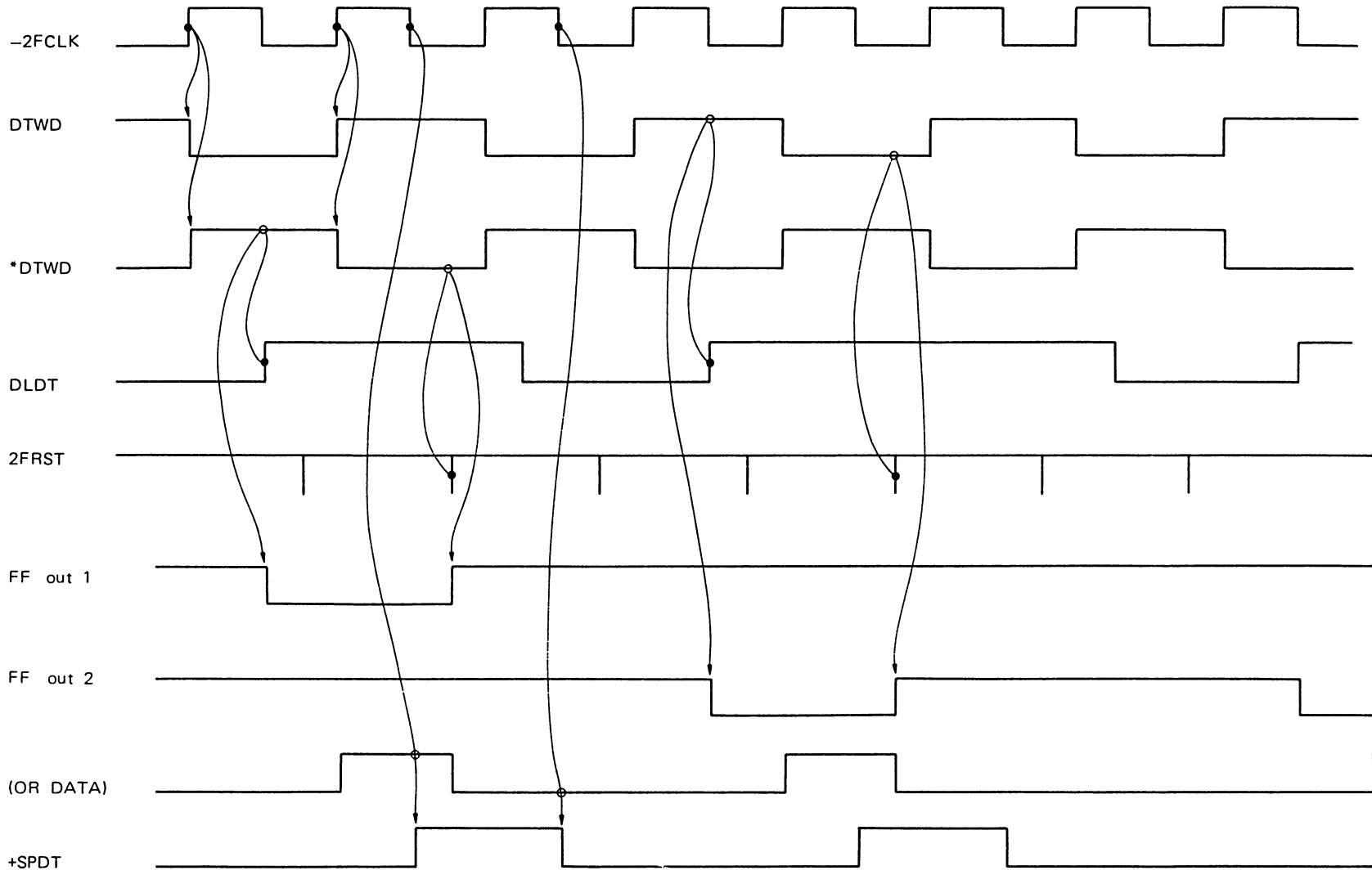


Figure 4.6.45 Data Window Timing Chart

(6) VFO Control

The VFO Control circuit controls the input to the VFO circuit, that is, the PLO output PLO1F or recovered read data, RAWDT, also generates VFO Fast Synchronization (VFOFS) for faster VFO synchronization with the input signal RAWDT or PLO1F.

In the start-up sequence, when the Start Pulse (STARTP) is applied to the Seek Control circuit, Initial Seek (INSK) is initiated and the heads move towards the servo zone. From the leading edge of INSK to the going false of IGB2 detect, PLO Fast Synchronization (PLOFS) is applied to the PLO circuit on the SDRM PCB. PLOFS enables faster synchronization of the PLO circuit with 2B clock and also initiates the PLO counter.

The Initial Seek completion sets Linear Mode (LNMD), and also VFO Lock (VFOLK) to enable the synchronization of the VFO circuit. The leading edge of VFOLK triggers the VFO Fast Synchronization (VFOFS) one-shot (11.3 us). VFOFS sets the PLO Latch so that the PLO output, PLO $\frac{1}{2}$ F, is applied to the input of the circuit and also activates faster synchronization of the VFO circuit. When the heads are retracted to the Landing Zone, VFOLK is reset to disable the synchronization of the VFO circuit. The timing chart of Initial Seek VFO control is shown in Figure 4.6.56. When an RTZ command is issued to the unit, RTZ Enable (RTZE) is set and VFOLK is reset. The completion of an RTZ operation activates the LNMD signal, VFOLK and VFOFS signals. The timing chart of an RTZ VFO control is shown in Figure 4.6.57.

During a non-read operation, the VFO circuit synchronizes with the PLO output, PLO1F, and generates VFO clock (VFOCLK). In Hard Sector mode, at the beginning of a read operation, Read Gate is applied to the RG True Detect circuit after 4-bits and is clocked by the trailing edge of the $\frac{1}{2}$ -Byte clock, CLK2. Rise Red Gate (RRG) signal, which is an output of the RG True Detect circuit, is applied to a 3-Byte Shift Register and then its output presets Ten on the Lock-To-Data counter to generate a 6-Byte Lock-To-Data (LDATA) signal. The LDATA signal is sent to the VFO Latch circuit so that the VFO circuit synchronizes with RAWDT.

At the end of Read Gate, a 1-Byte Fall Red Gate (FRG) is detected and applied to the Lock To PLO Counter to generate a 6-Byte Lock To PLO (LPLO) signal. The LPLO signal is sent to the VFO Latch circuit so that the VFO Circuit synchronizes with PLO $\frac{1}{2}$ F.

LDATA and LPLO signals are converted into the VFO Fast Synchronize (VFOFS) signal and applied to the VFO Filter circuit to decrease the time constant of the Filter. This promotes faster synchronization of the VFO circuit with RAWDT or PLO $\frac{1}{2}$ F.

The VFO control block diagram and timing chart are shown in Figure 4.6.58 and 4.6.59 respectively.

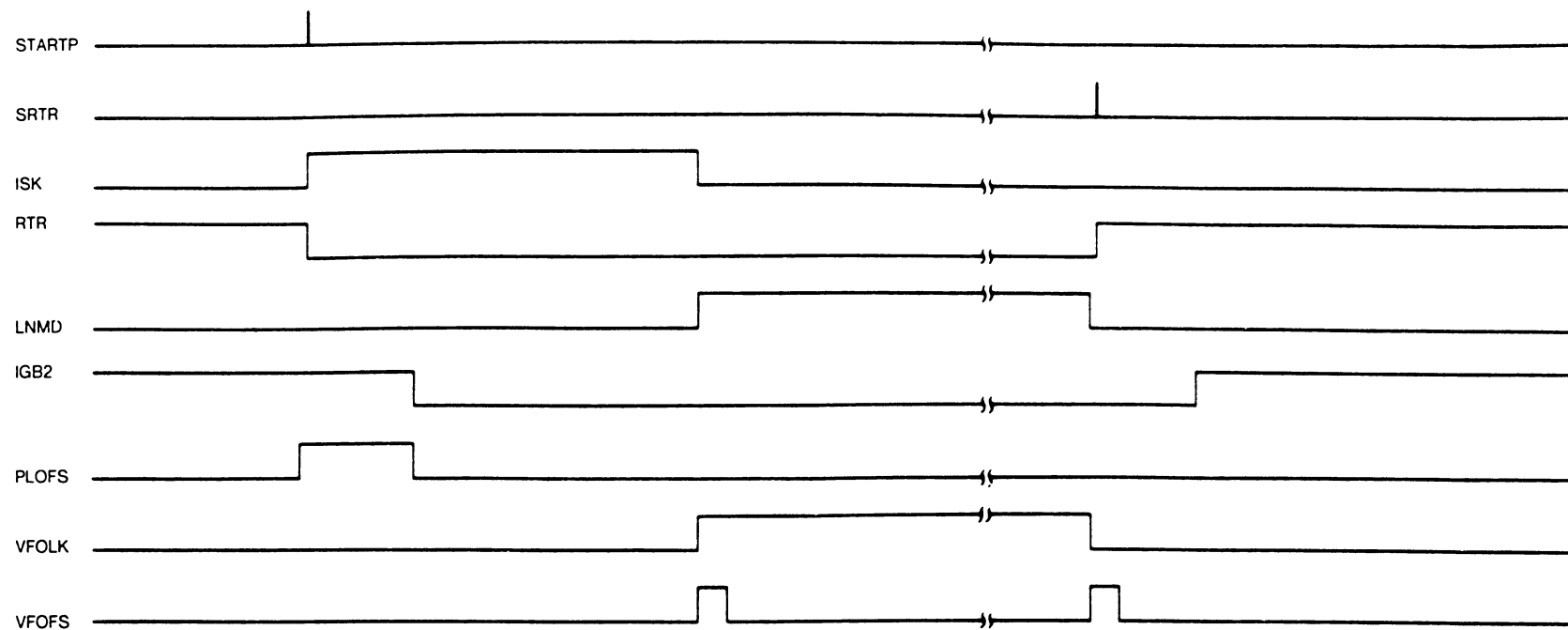


Figure 4.6.46 VFO Control During Initial Seek/Retract Operation

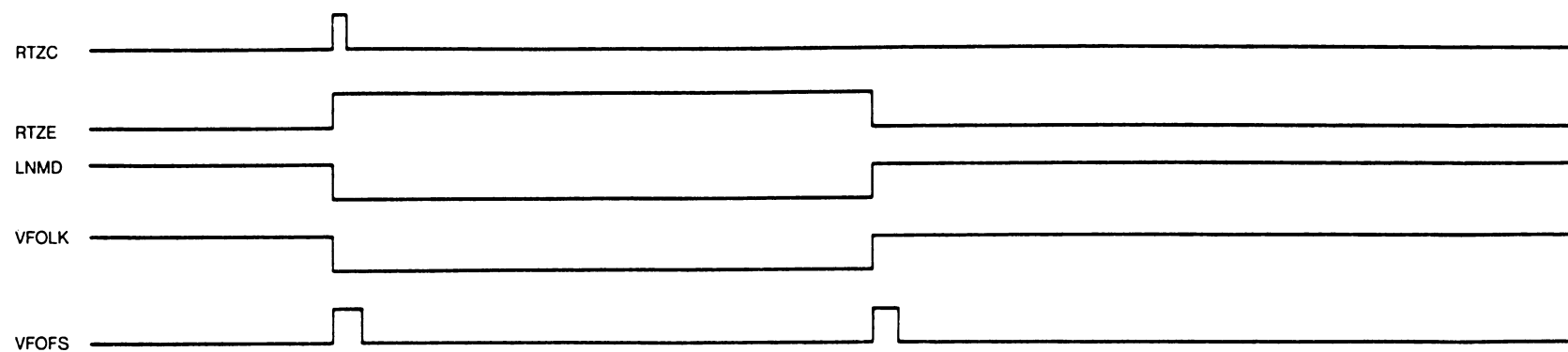
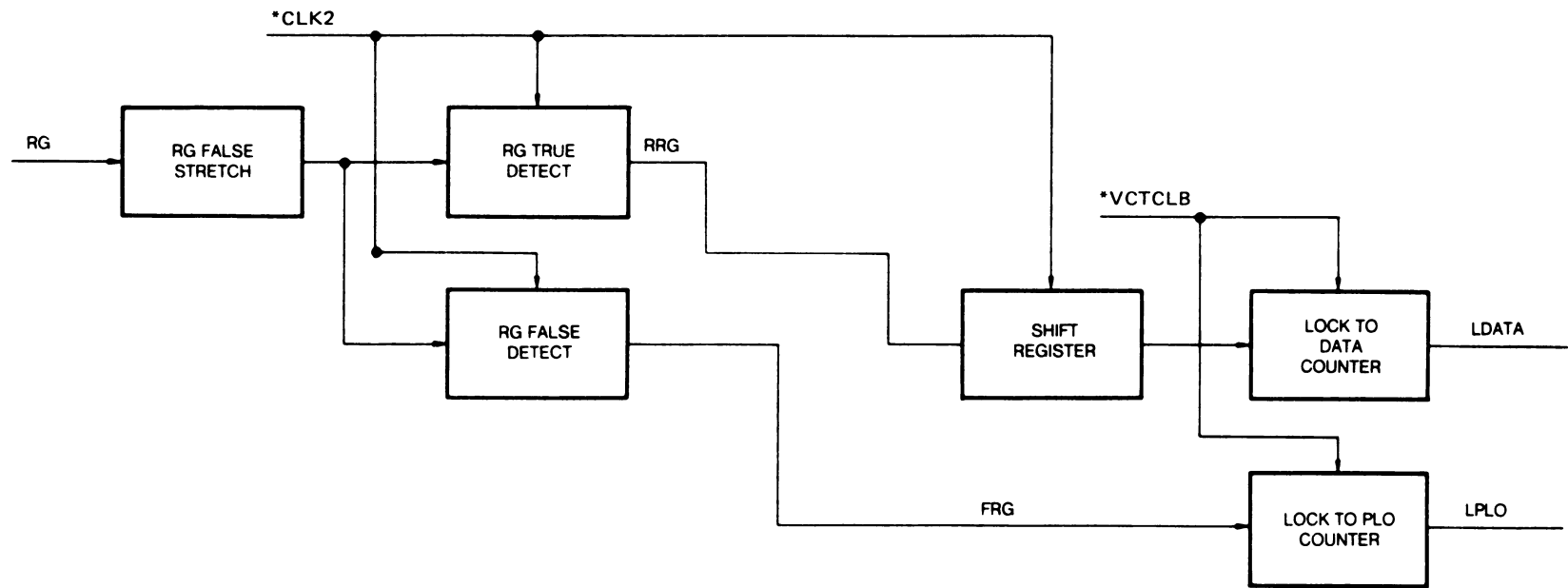


Figure 4.6.47 VFO Control During RTZ Operation



Note: All functions are included on the VOIM.

Figure 4.6.48 VFO Control Block Diagram

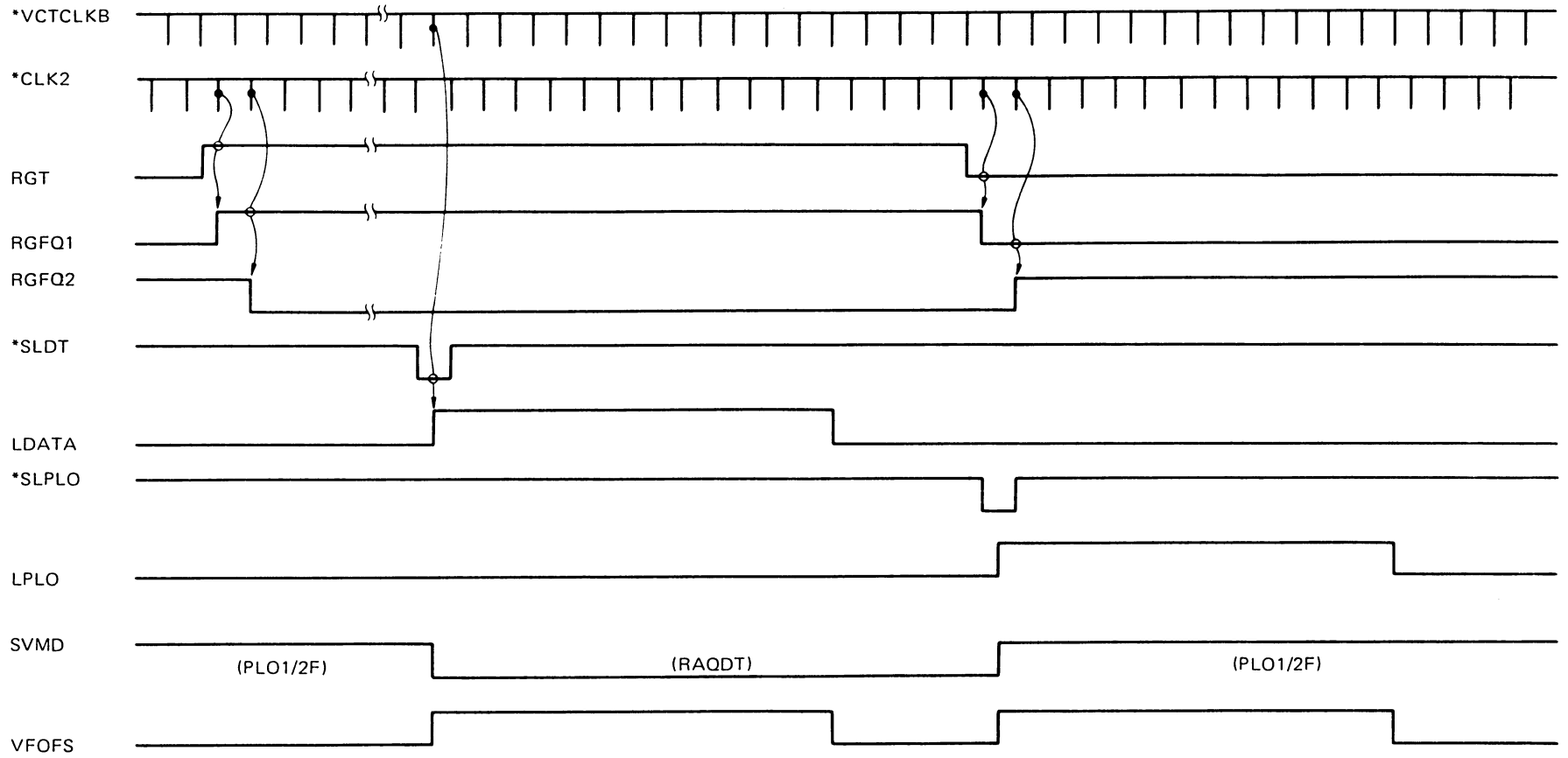


Figure 4.6.49 UFO Control During Read/Write Operation

4.6.8.2 2-7 decoder

The 2-7 decoder converts the 2-7 data into NRZ data.

The 2-7 data synchronized with 2F clock sent from VFO circuit is input to an eight-bit shift register, then sent to a decoder in which the 2-7 data is converted to NRZ data according to the conversion table listed in Table 4.5.2.

A read command starts the decoder detecting all 1 gap data. When this data is detected, the 2F clock is toggled to VFO clock (VFOCLK) to transfer the data. The 2-7 data is converted to NRZ data by gating VFOCLK. The NRZ data synchronized with VFOCLK is sent to the controller.

Figure 4.5.52 shows the abbreviated block diagram of the 2-7 decoder.

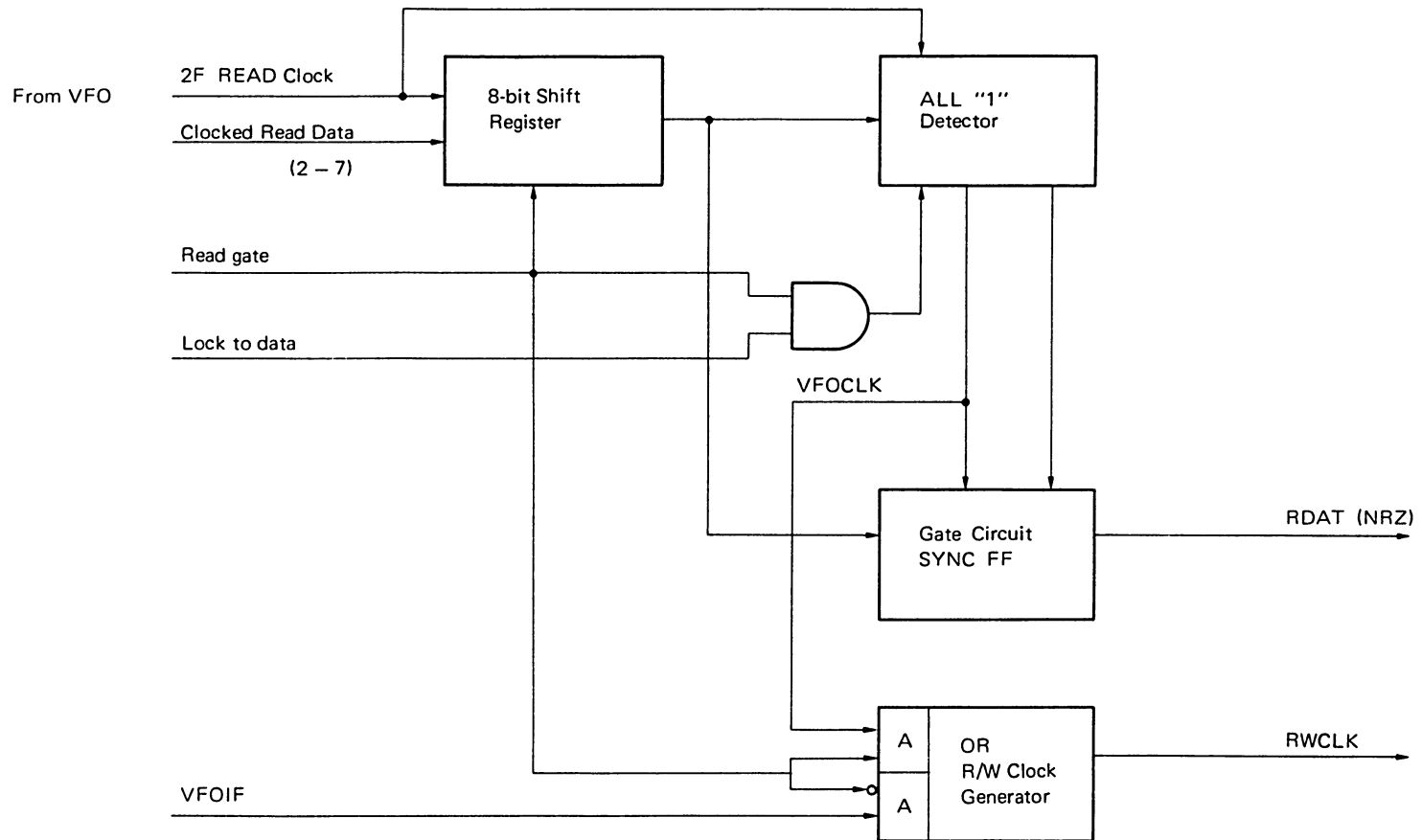


Figure 4.6.50 2-7 Decoder Block Diagram

Section 5

Trouble Shooting Guide

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5. TROUBLE SHOOTING GUIDE

5.1. INTRODUCTION

This section will contain trouble shooting flow charts according to the error status on the disk unit and control unit.

Note: It is recommended that before any operations, maintenance personnel read carefully Section 6 Maintenance and fully understand the details of the procedures and tools required.

Inspect each item in this list before applying power to the unit after installation.

- (1) Ensure that the AC line conditions satisfy the unit requirements.
- (2) If the control unit does not utilize Pick/Hold power sequencing lines, select "Local" mode on the power supply unit.
- (3) Inspect interface cables to ensure pin 1 on the cable goes to pin 1 of the connect both at the unit and control unit.
- (4) If the unit is in daisy chain with another unit, make sure the last unit has a Line Terminator (LTN) installed.
- (5) Ensure that the actuator lock is in the "OFF" position.
- (6) Ensure that the spindle drive motor lock is in the "OFF" position.
- (7) Ensure that the motor pulley and belt tension are correct per the AC line frequency.
- (8) Ensure that the spindle grounding plate (anti-static brush) is properly positioned.
- (9) Ensure that the proper logical unit number (LUN) of the unit is selected on the KGEM PCB and that each LUN is unique to only one unit.
- (10) Ensure that Hard/Soft sector mode is selected per the system configuration.
- (11) In the case of Hard Sector (fixed sector length), ensure that the correct sector count is set on the VOIM PCB.
- (12) Ensure that Tag 4/5 is enabled or disabled as per system configuration.
FOR DUAL PORTED DRIVES.
- (13) Ensure that Disable/Normal keys are correctly set to the Normal position.
- (14) Ensure the Release Timer Key is set to the desired position.
- (15) Ensure that all PCB assemblies are firmly seated.

5.2. ERROR STATUS

The disk unit and/or the control unit will issue the following statuses.

Table 5.2.1 Error Status

NOT READY	NOT READY status results if the disk drive is not ready.
DEVICE CHECK	DEVICE CHECK status indicates a fault condition has occurred in the unit.
SEEK ERROR	SEEK ERROR status results if a seek error has occurred in a seek operation.
READ ERROR	READ ERROR status results if a data error has occurred in a read operation.
DUAL PORT	DUAL PORT malfunction concerns Select/Reserve functions.

Maintenance Personnel can see the unit status on the Maintenance Aid Display at the rear of the PCB chassis in the unit. Each status is defined by decoding status tags (0 to 3) as shown in Table 5.2.2.

Table 5.2.2 Maintenance Aid Display

Tag Decode	Tag Decode 0	Tag Decode 1	Tag Decode 2	Tag Decode 3
Status	Not Ready	Device Check	Unit Normal	Seek Check
Status 0	Power Ready	Control Check 1	Unit Selected	Seek or RTZ Time Out
Status 1	Channel Ready	Control Check 2	Fixed Sector Mode	Seek Guard Band
Status 2	Speed OK	Read/Write Check 1	On Cylinder	Linear Mode Guard Band
Status 3	Start 1	Read/Write Check 2	File Protected	RTZ Outer Guard Band
Status 4	Start 2	Read/Write Check 3	Busy	Over Track Crossing Pulse
Status 5	Initial Seek Time Out	Read/Write Check 4	Access-Head *1 selected	Illegal Cylinder *2 Address
Condition	URDY	URDY-DVCK	URDY, DVCK, SKERR	URDY, DVCK, SKERR

* Notes: (1) Access-Head Selected must be always true (ON).
 (2) Illegal Cylinder Address must be always false (OFF).

The trouble shooting guide is provided with the Error Code which is defined by the Maintenance Aid Display LED's. Each error code is represented in hexadecimal, in which TG2 is MSB (Most Significant Bit) and ST0 is LSB (Least Significant Bit). The error codes are shown in Table 5.2.3.

Table 5.2.3 Error Code

Unit Status	Error Code	TG2	TG1	ST5	ST4	ST3	ST2	ST1	ST0	Error/Fault
Not Ready Status	00/02	0	0	0	0	0	0	(*2) X	0	Not Power Ready
	01/03	0	0	0	0	0	0	X	1	Not Speed OK
	05/07	0	0	0	0	0	1	X	1	Not GBENB
	0D/1F	0	0	0	0	1	1	X	1	Not START
	1D/1F	0	0	0	1	1	1	X	1	Not STARTP
	3D/3F	0	0	1	1	1	1	X	1	Initial Seek Time Out (* 1)
Device Check Status	41	0	1	0	0	0	0	0	1	Control Check 1
	42	0	1	0	0	0	0	1	0	Control Check 2
	44	0	1	0	0	0	1	0	0	Read/Write Check 1
	48	0	1	0	0	1	0	0	0	Read/Write Check 2
	50	0	1	0	1	0	0	0	0	Read Write Check 3
	60	0	1	1	0	0	0	0	0	Read/Write Check 4
Seek Check Status	C1	1	1	0	0	0	0	0	1	Seek or RTZ Time Out
	C2	1	1	0	0	0	0	1	0	Seek Guard Band
	C4	1	1	0	0	0	1	0	0	Linear Mode Guard Band
	C8	1	1	0	0	1	0	0	0	RTZ Outer Guard Band
	D0	1	1	0	1	0	0	0	0	Over Track Crossing Pulse
	E0	1	1	1	0	0	0	0	0	Illegal Cylinder Address

(* 1) Error Code "3F" activates DVCK status, which is issued to the control unit and lights the DVCK LED on the optional front panel.


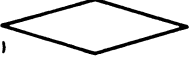



(* 2) "X" is irrelevant.

5.3 TROUBLE SHOOTING SYMBOL

The trouble shooting flow chart contains the procedures to pursue malfunctions starting from an error status.

The following conventions are provided to aid understanding the symbols used in the trouble shooting flow charts as shown in Table 5.3.1.

Table 5.3.1 Symbol of Flow Chart

Symbol	Description
	Terminals. Starting point of the trouble.
	Decision, go ahead according to YES or NO. (Reference test point.)
	Connector, go ahead same-numbered symbol in same sheet.
	Connector, go ahead same-numbered symbol in another sheet.
	Process

5.4 TROUBLE SHOOTING FLOW CHART

In this paragraph, the following flow charts are provided.

Figure 5.4.1 Not Ready

Figure 5.4.2 Device Check

Figure 5.4.3 Seek Error

Figure 5.4.4 Read Error

Figure 5.4.5 Dual Port

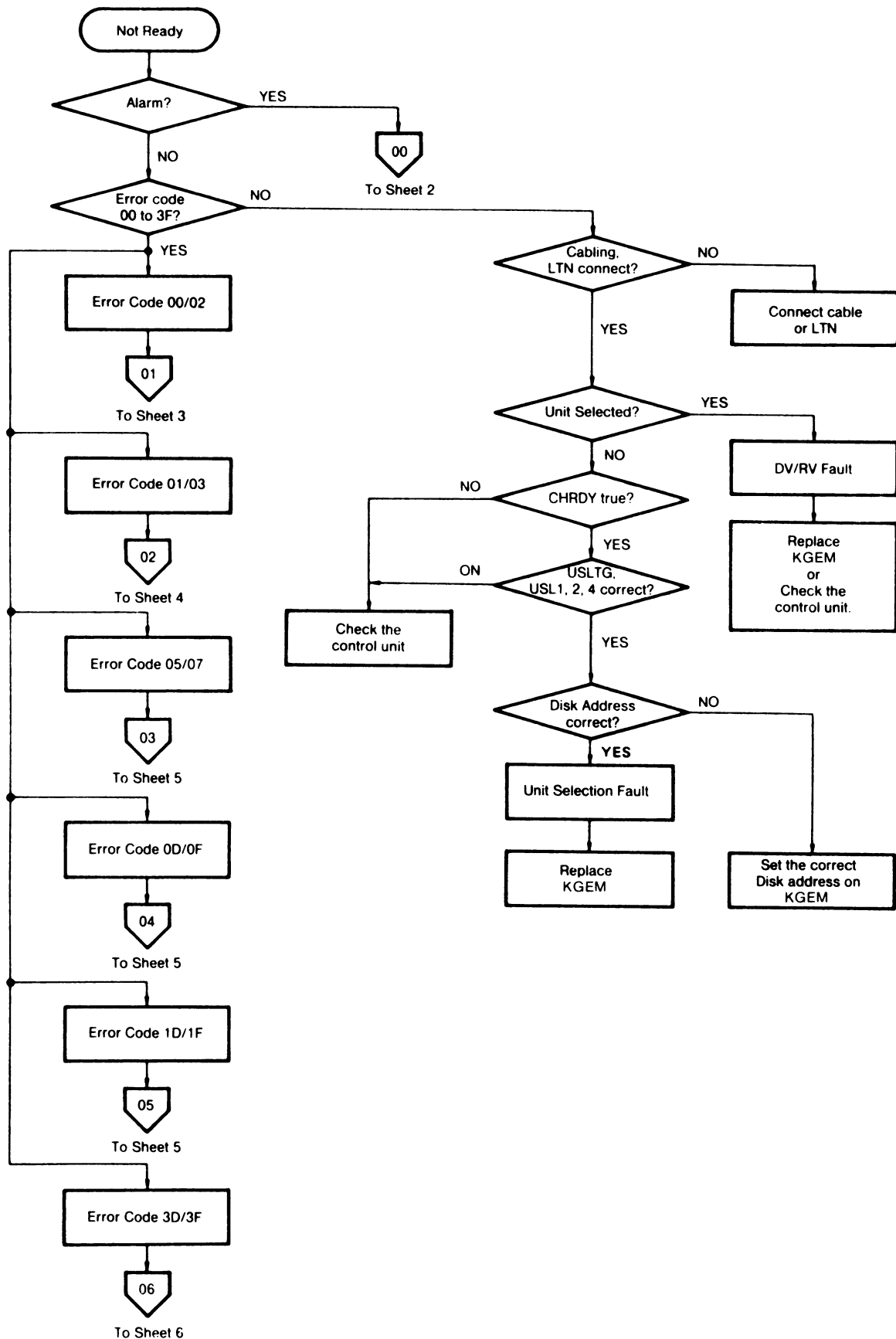


Figure 5.4.1 Not Ready Flow Chart (Sheet 1 of 6)

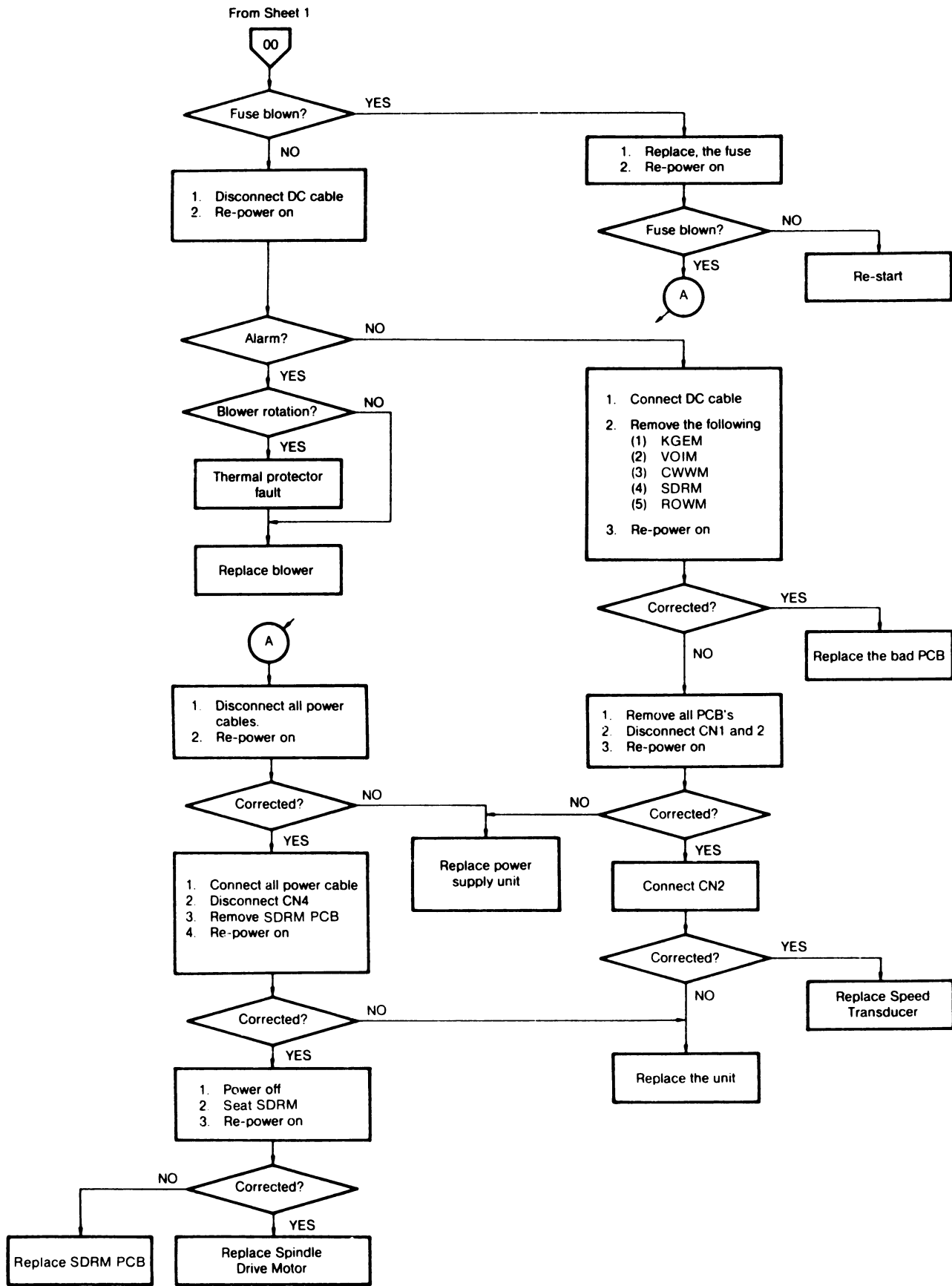


Figure 5.4.1 Not Ready Flow Chart (Sheet 2 of 6)

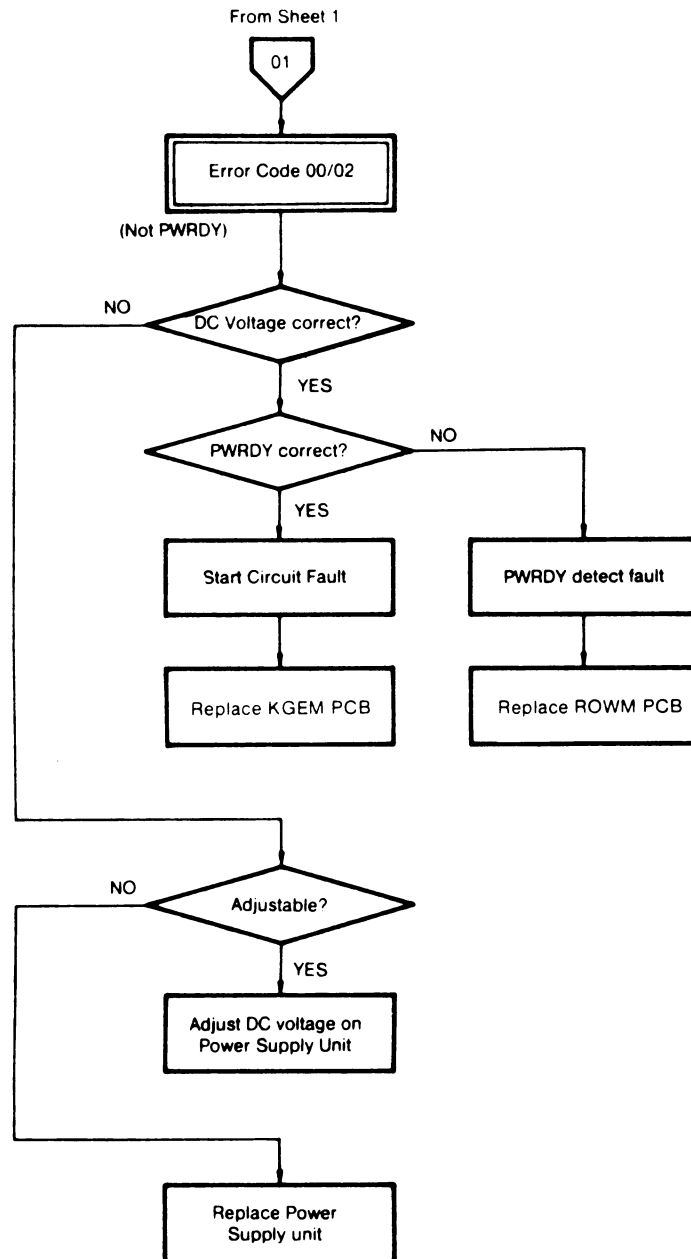


Figure 5.4.1 Not Ready Flow Chart (Sheet 3 of 6)

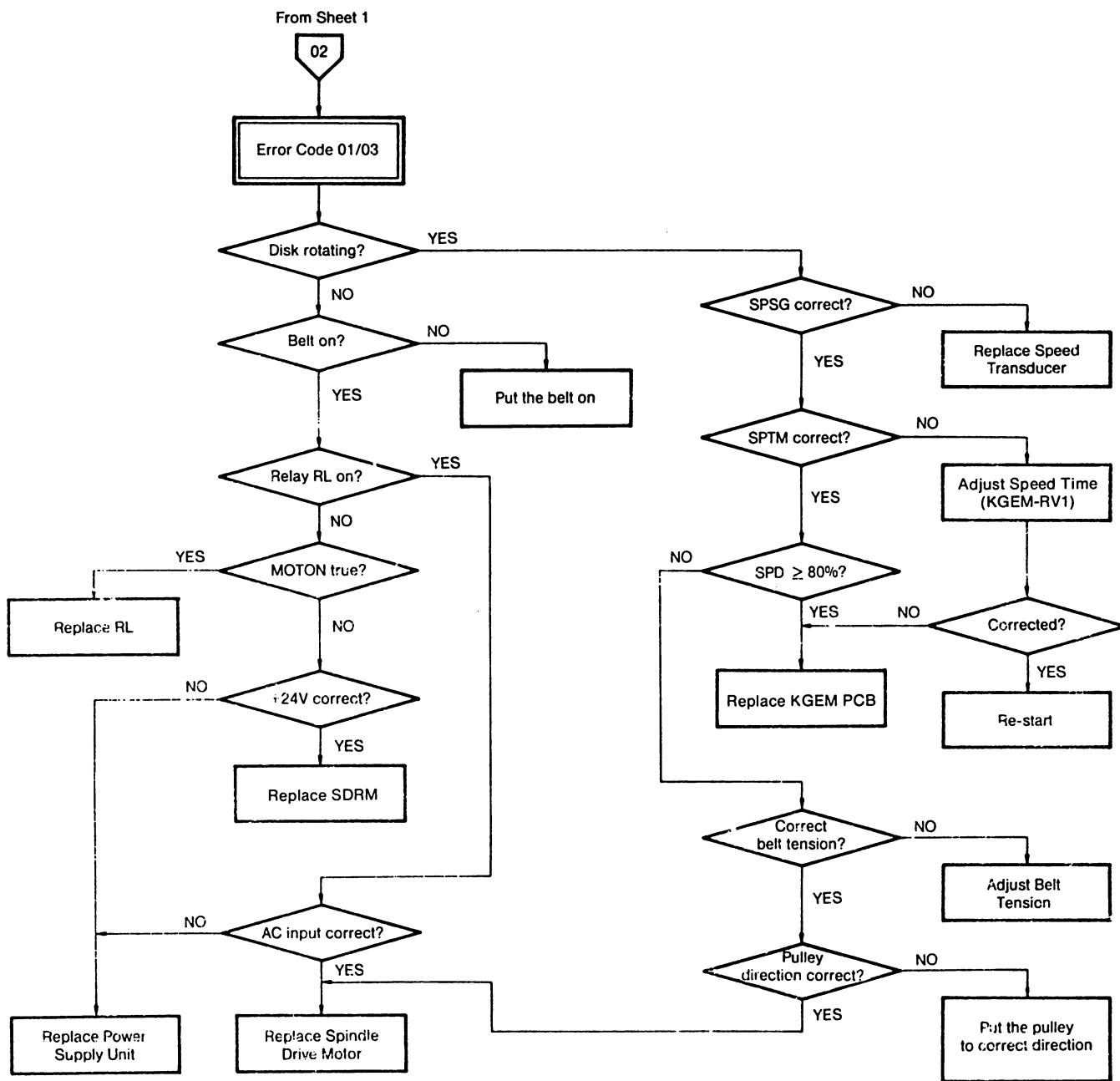


Figure 5.4.1 Not Ready Flow Chart (Sheet 4 of 6)

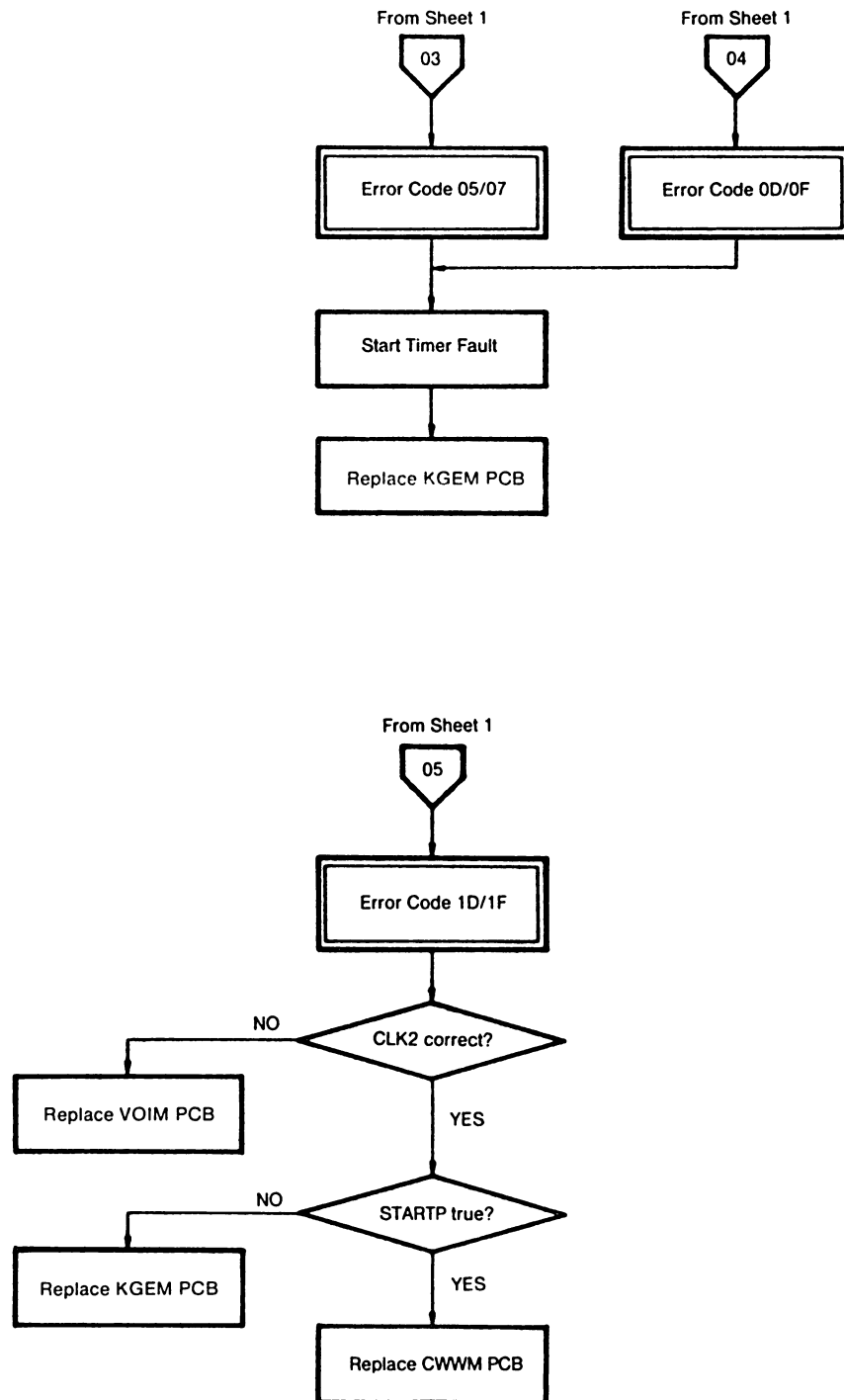


Figure 5.4.1 Not Ready Flow Chart (Sheet 5 of 6)

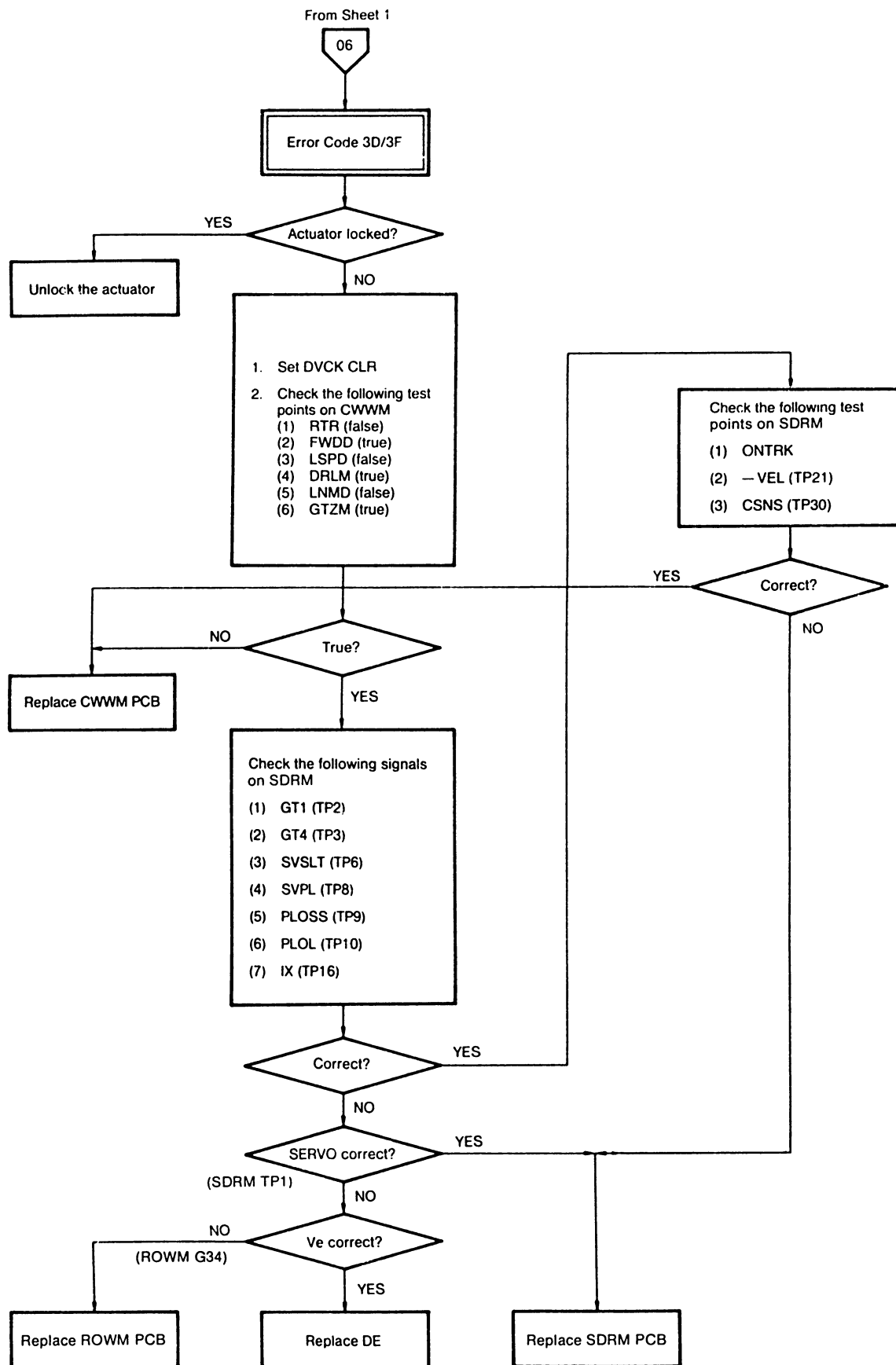


Figure 5.4.1 Not Ready Flow Chart (Sheet 6 of 6)

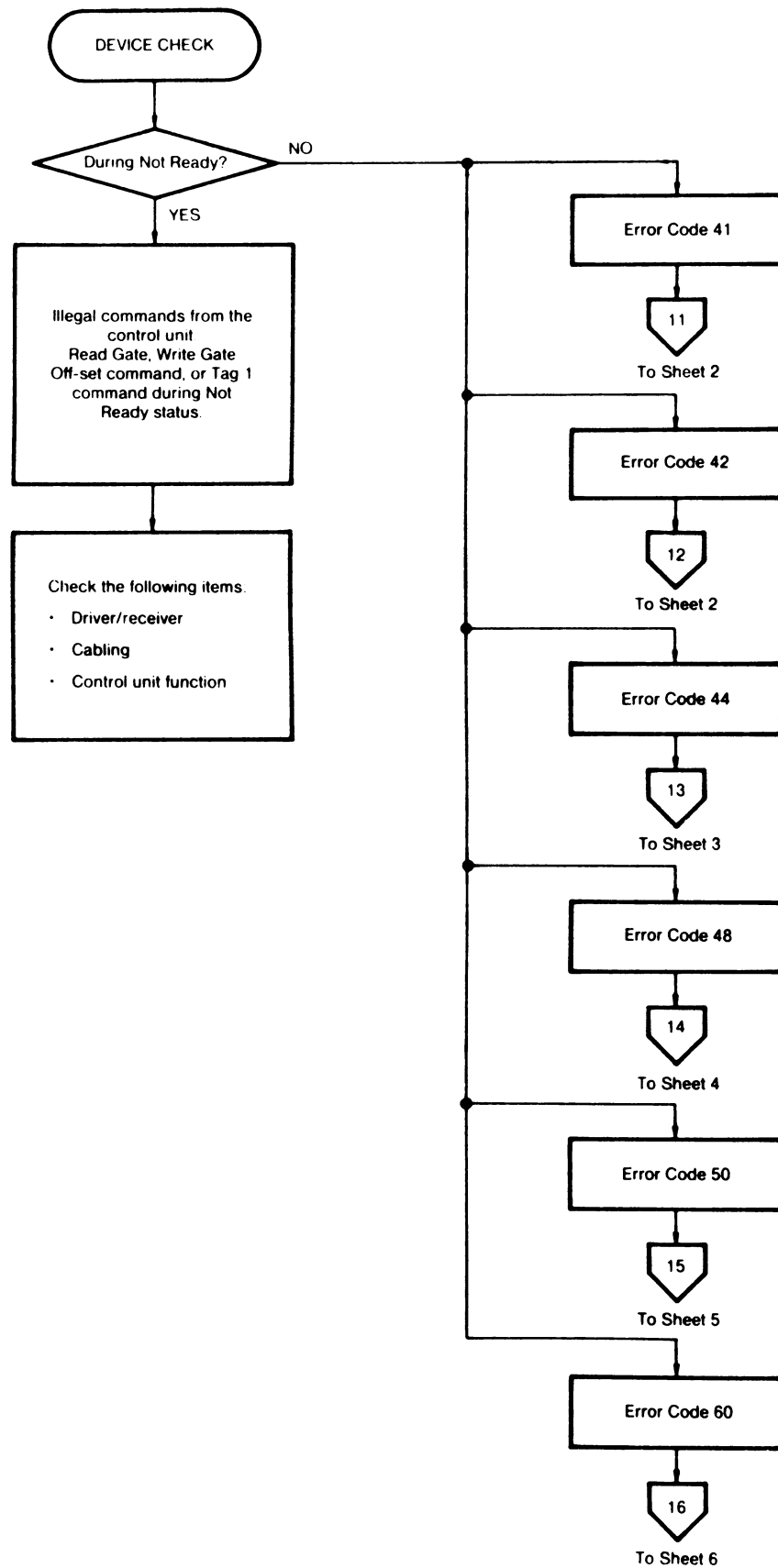


Figure 5.4.2 Device Check Flow Chart (Sheet 1 of 6)

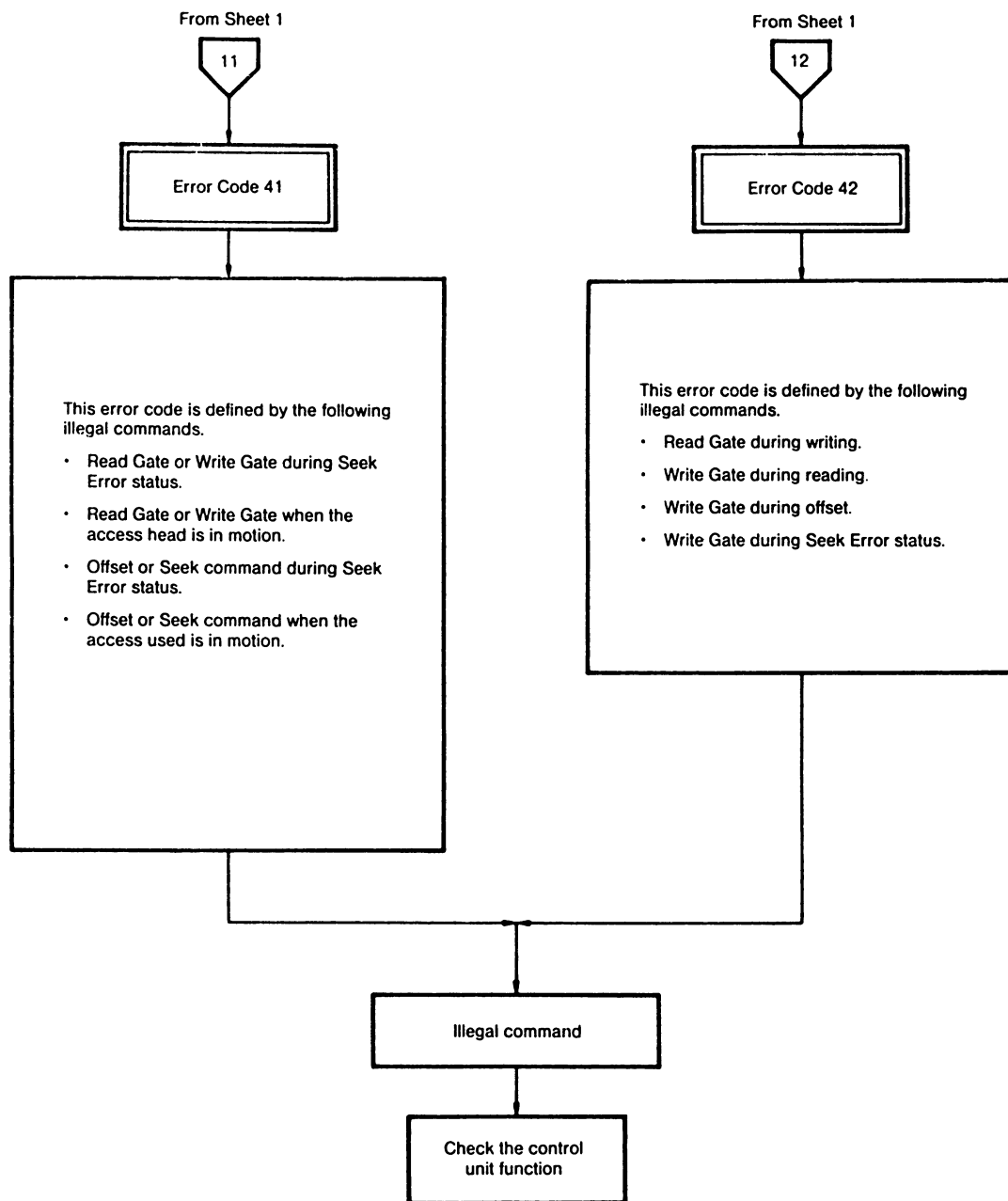


Figure 5.4.2 Device Check Flow Chart (Sheet 2 of 6)

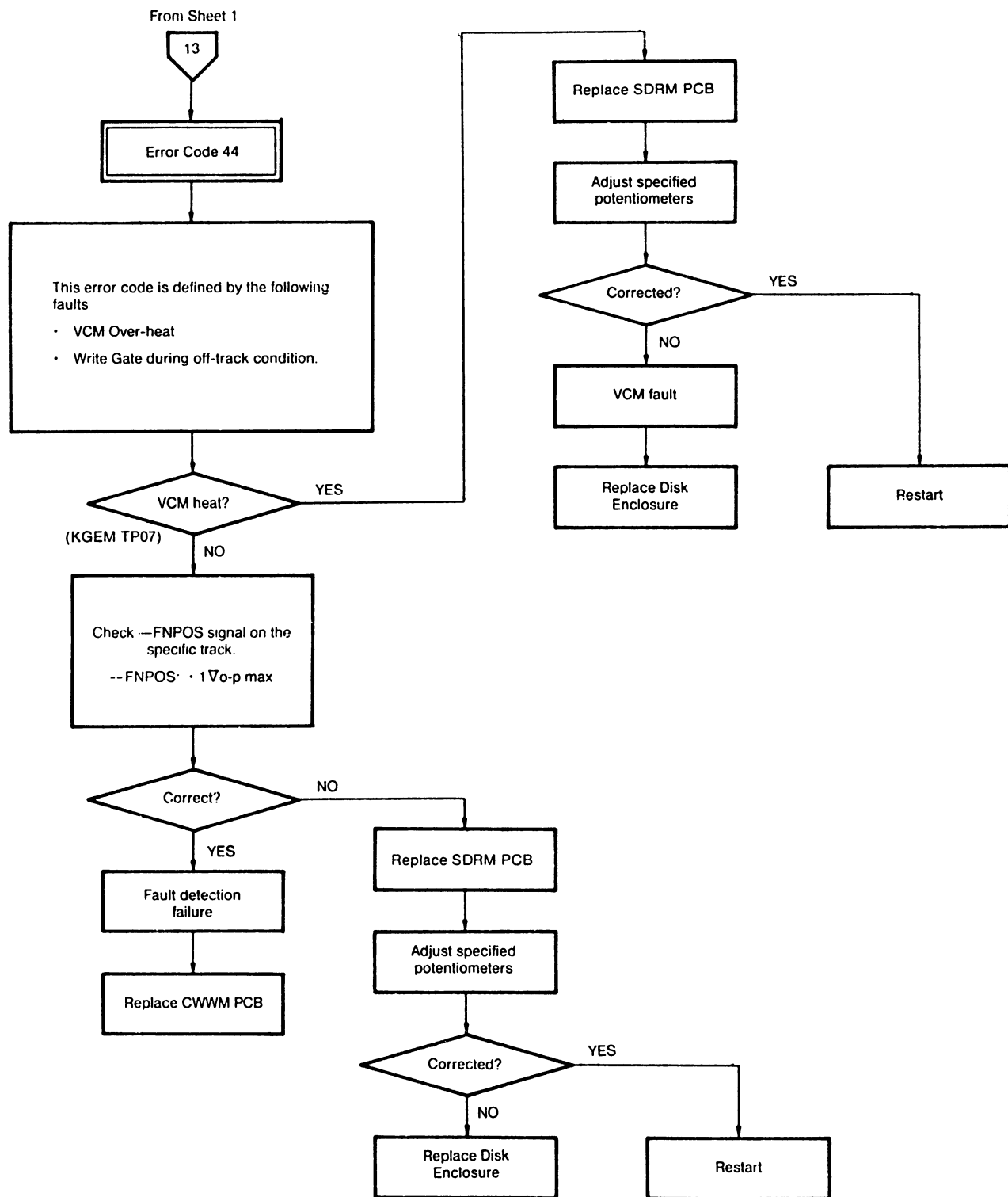


Figure 5.4.2 Device Check Flow Chart (Sheet 3 of 6)

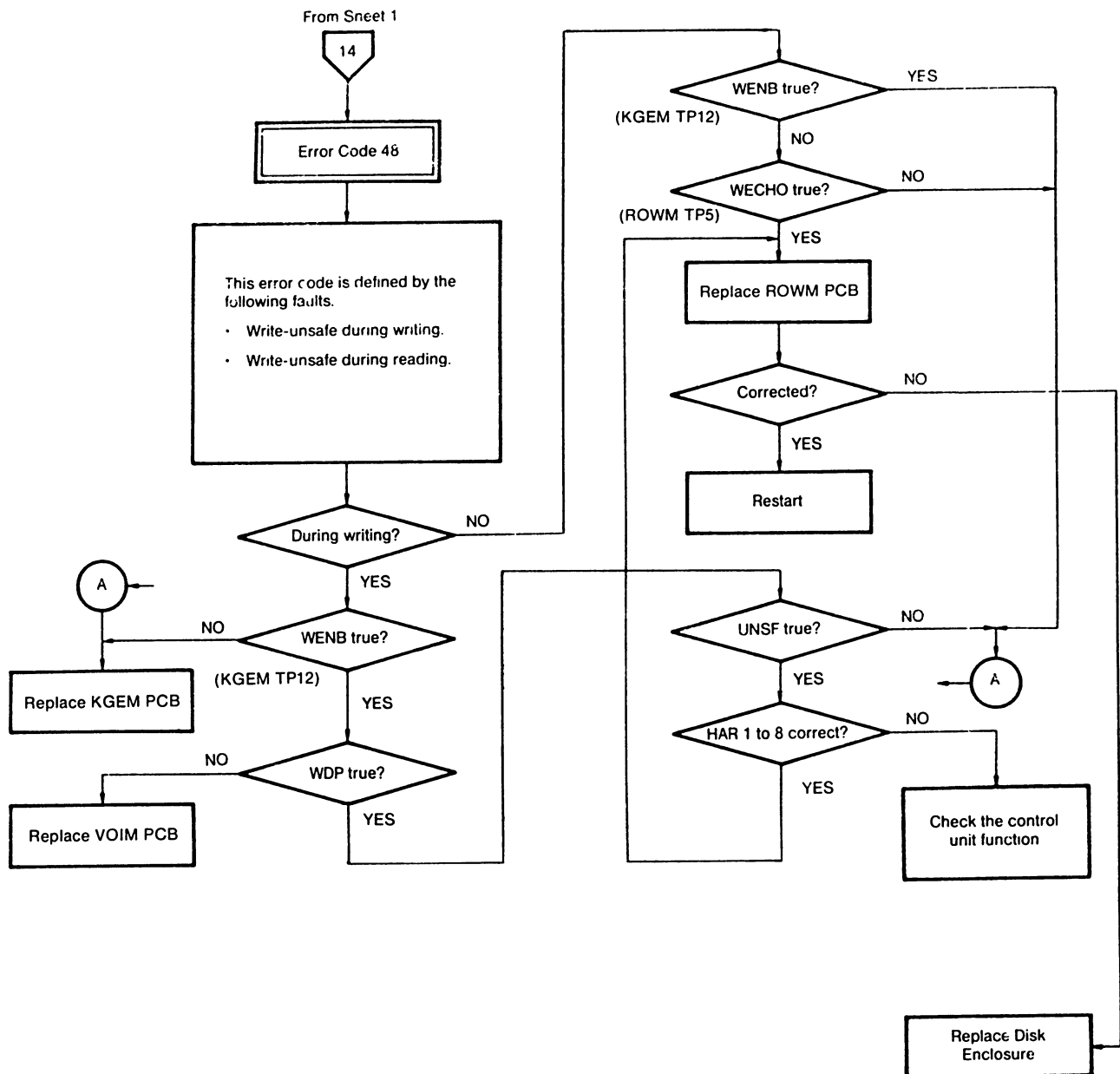
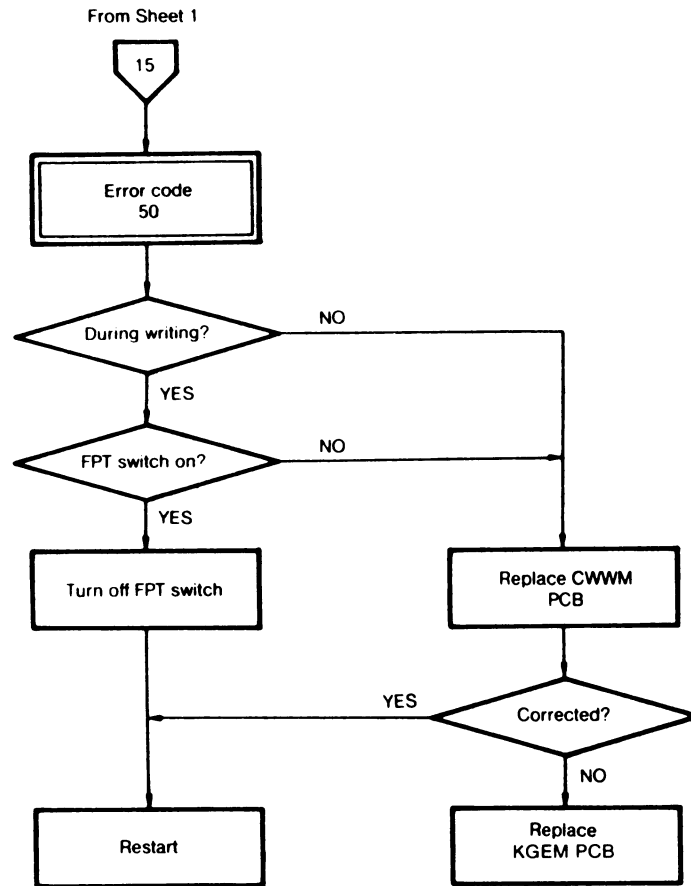


Figure 5.4.2 Device Check Flow Chart (Sheet 4 of 6)



Note: FPT (file-protect) switches are located on the front panel and the PCB chassis.

Figure 5.4.2 Device Check Flow Chart (Sheet 5 of 6)

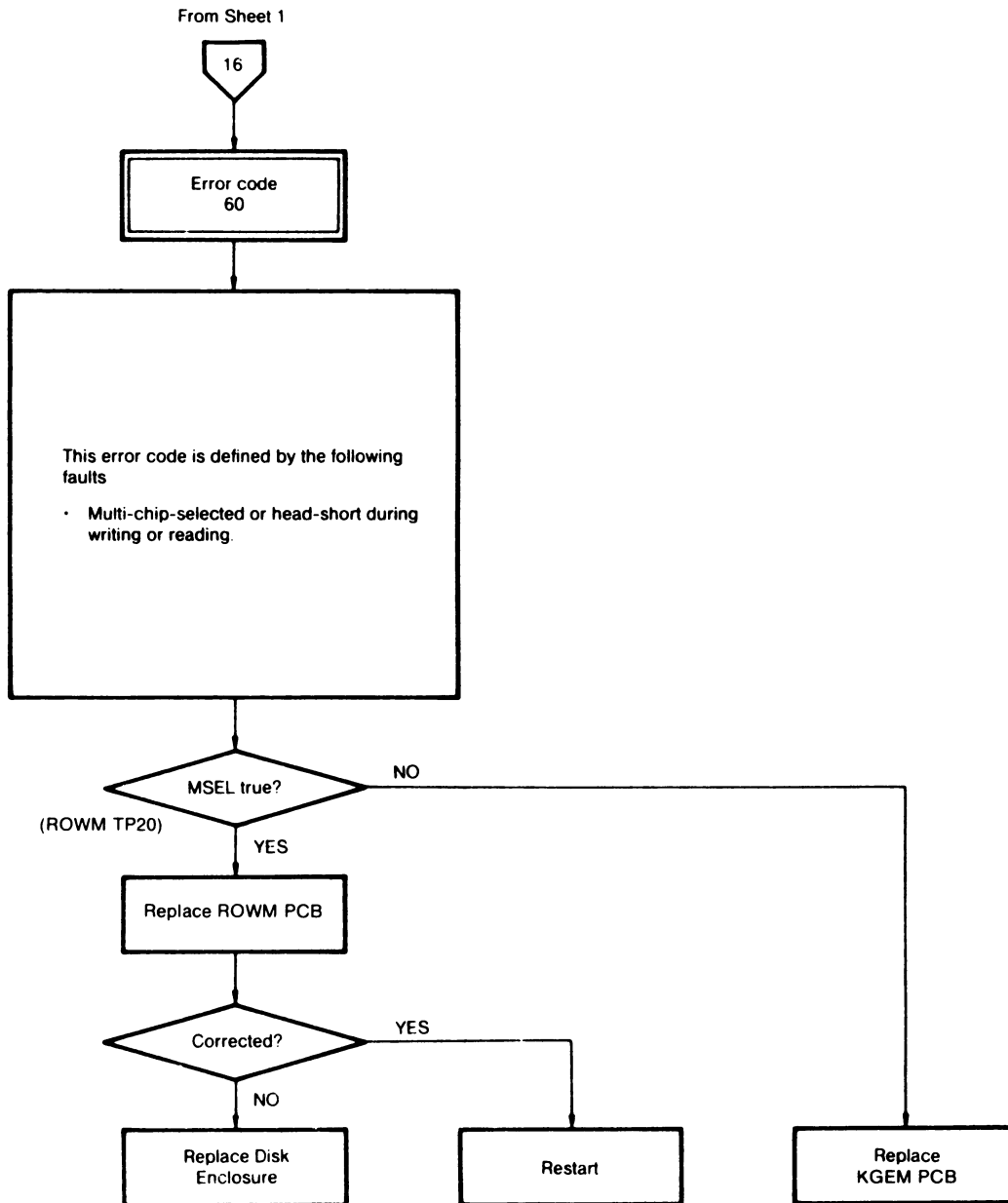


Figure 5.4.2 Device Check Flow Chart (Sheet 6 of 6)

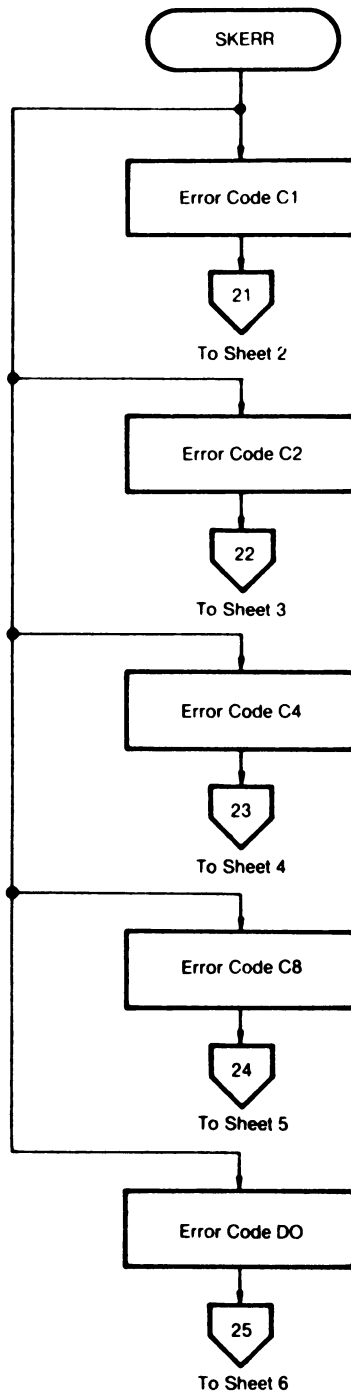


Figure 5.4.3 Seek Error Flow Chart (Sheet 1 of 6)

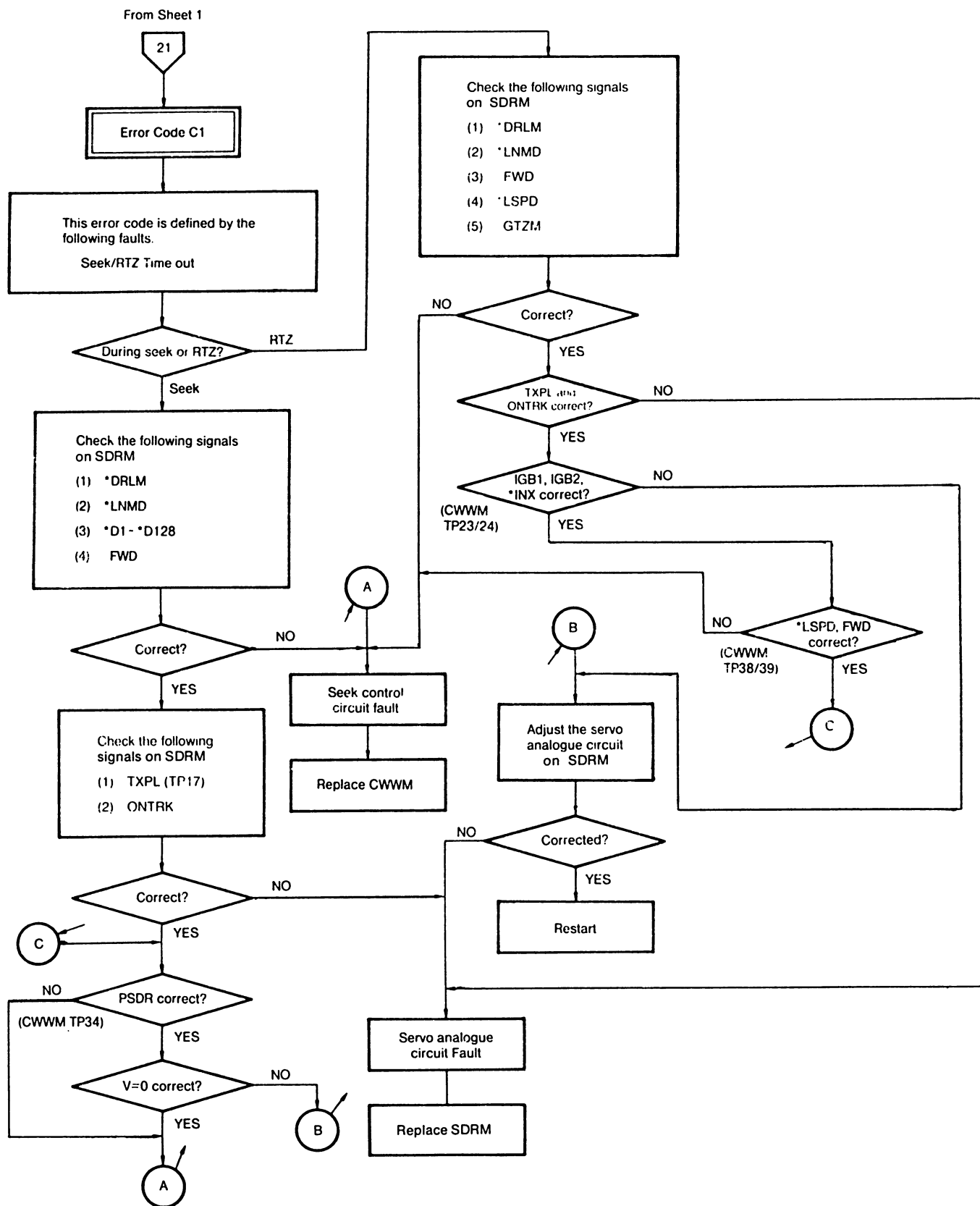


Figure 5.4.3 Seek Error Flow Chart (Sheet 2 of 6)

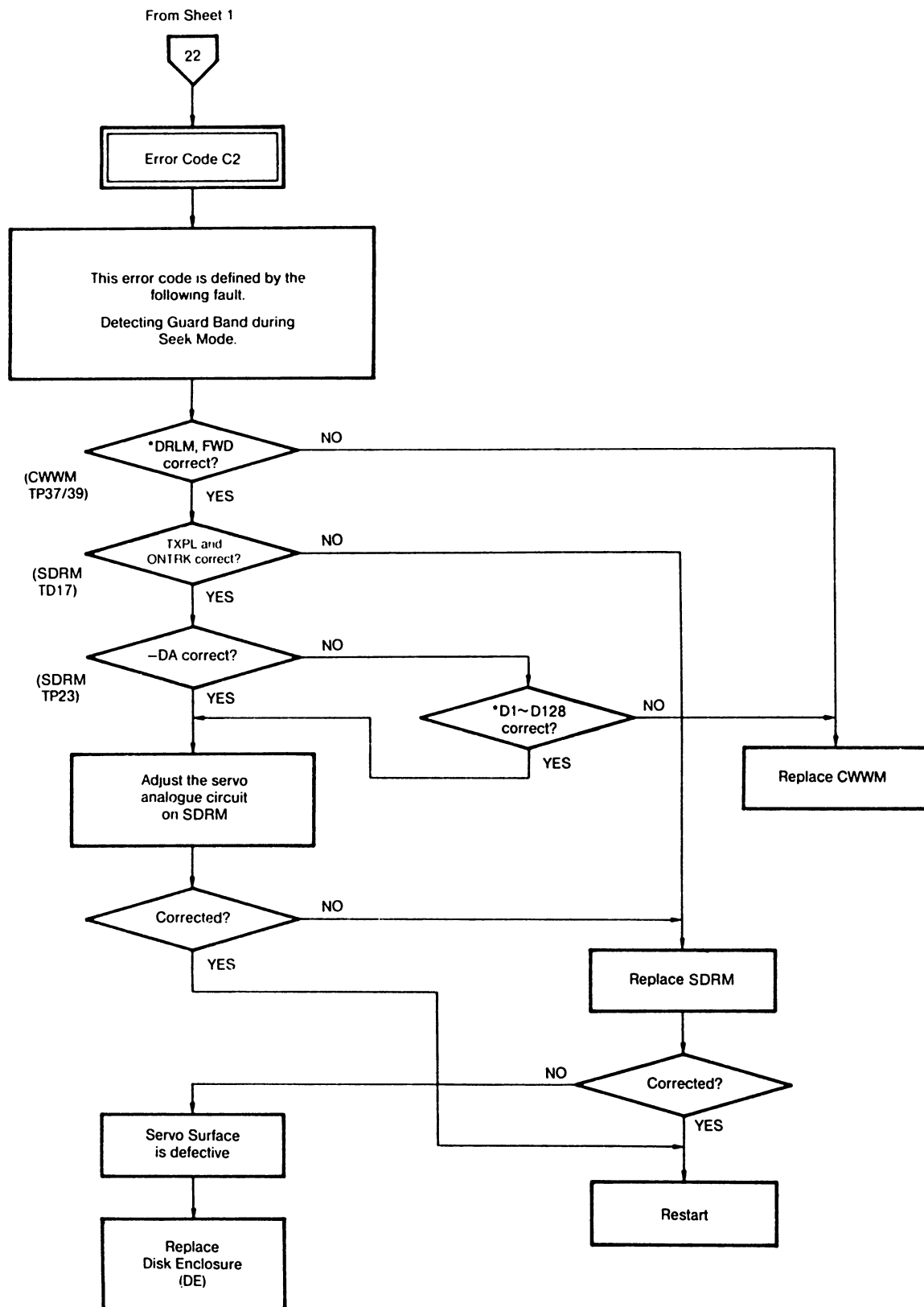


Figure 5.4.3 Seek Error Flow Chart (Sheet 3 of 6)

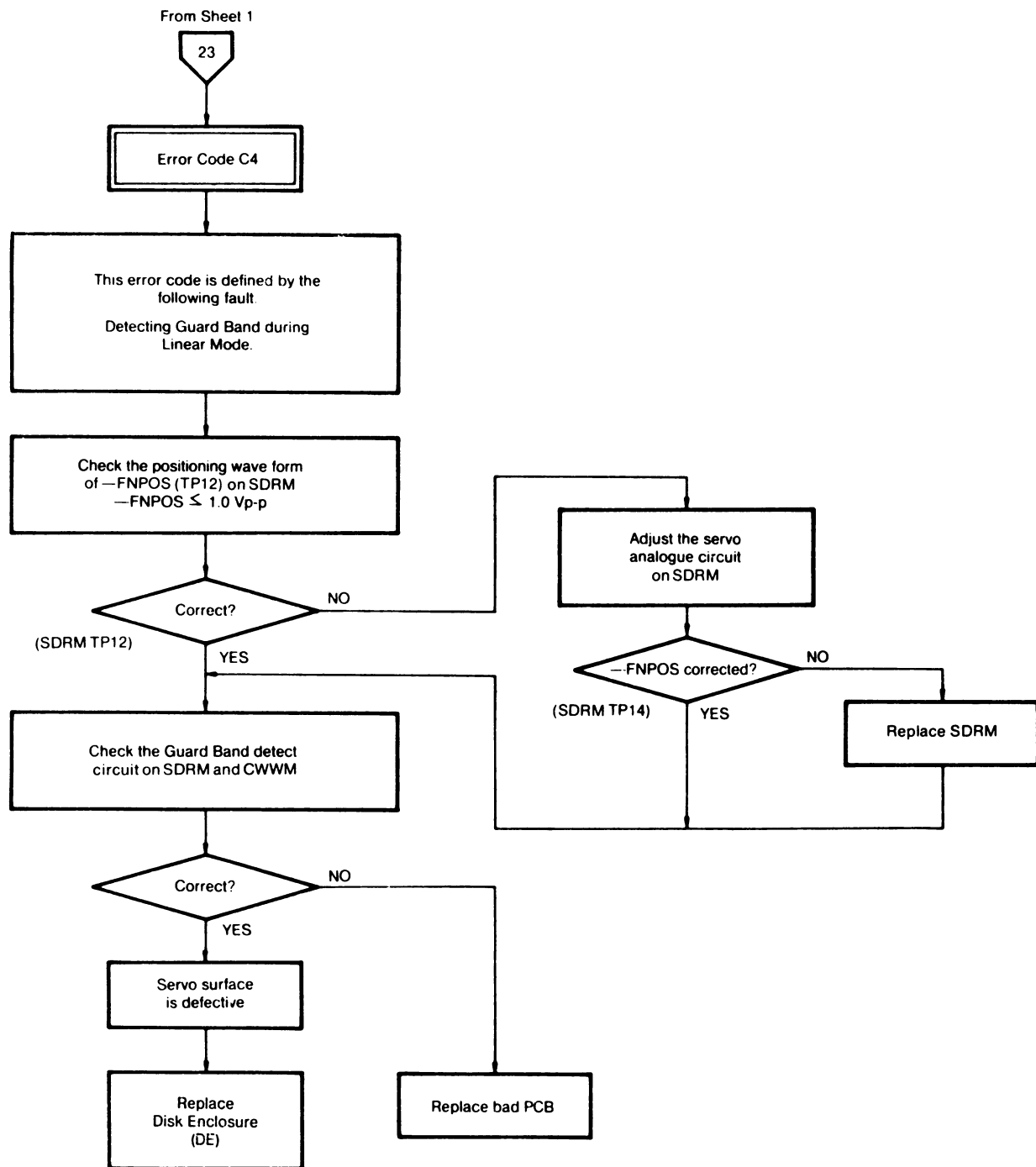


Figure 5.4.3 Seek Error Flow Chart (Sheet 4 of 6)

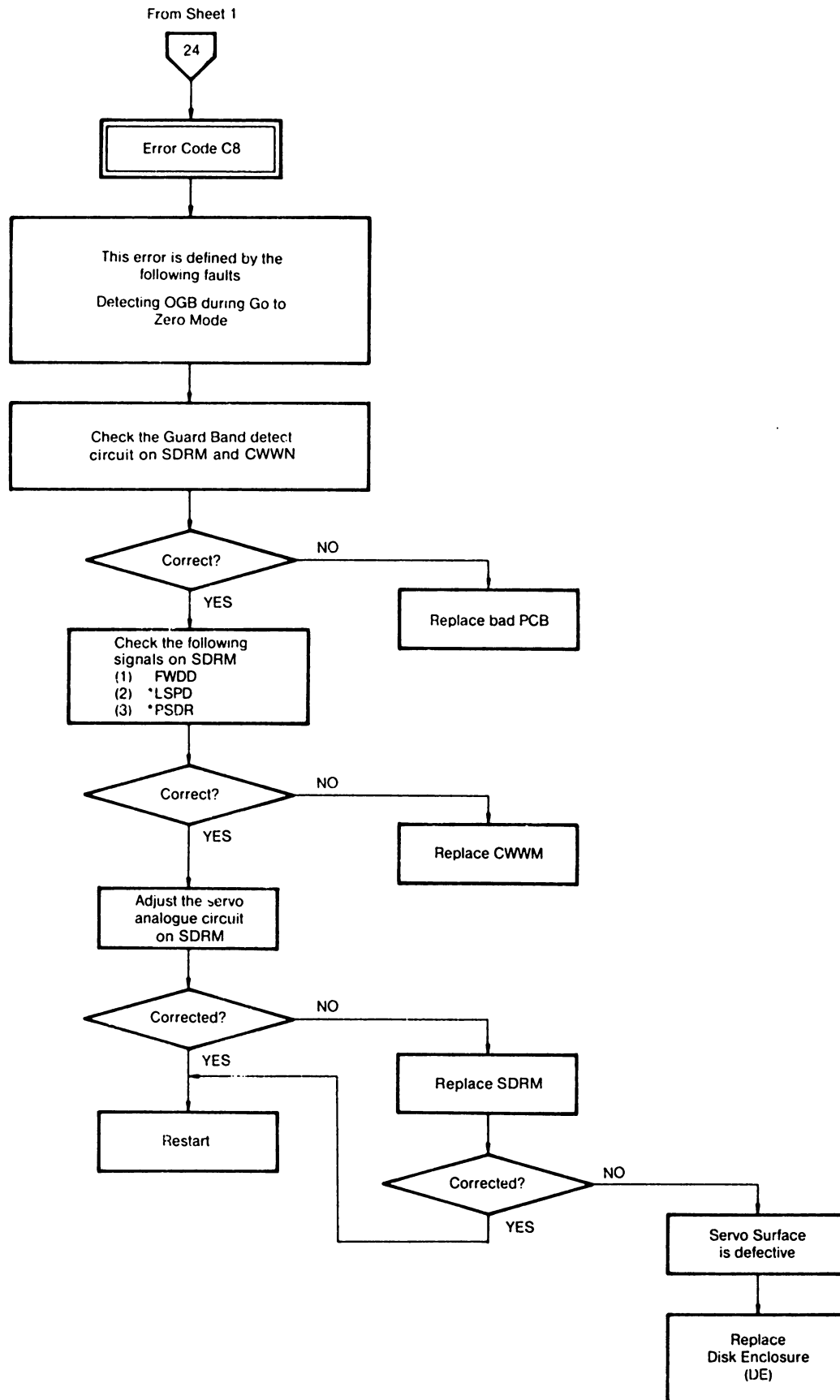


Figure 5.4.3 Seek Error Flow Chart (Sheet 5 of 6)

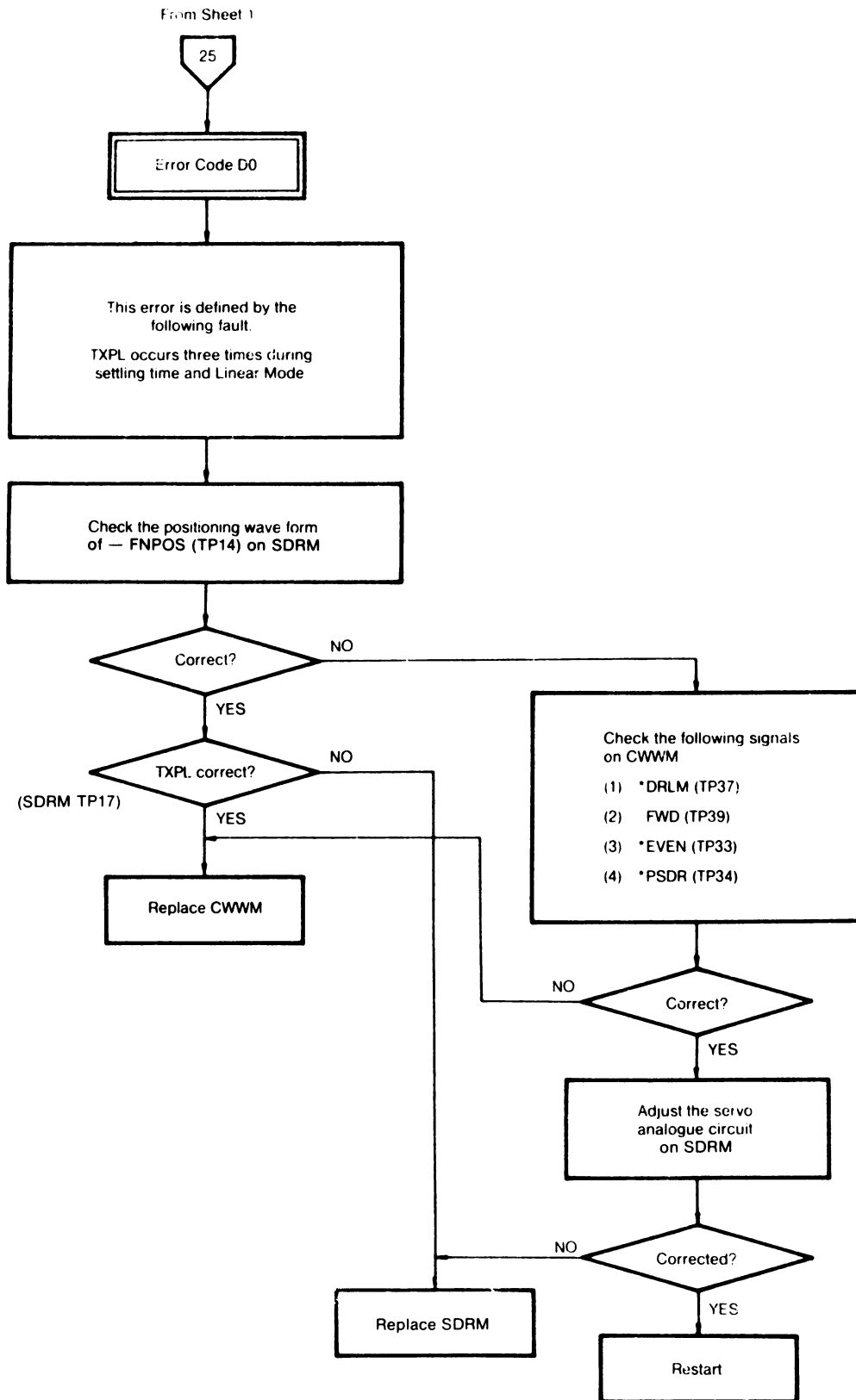
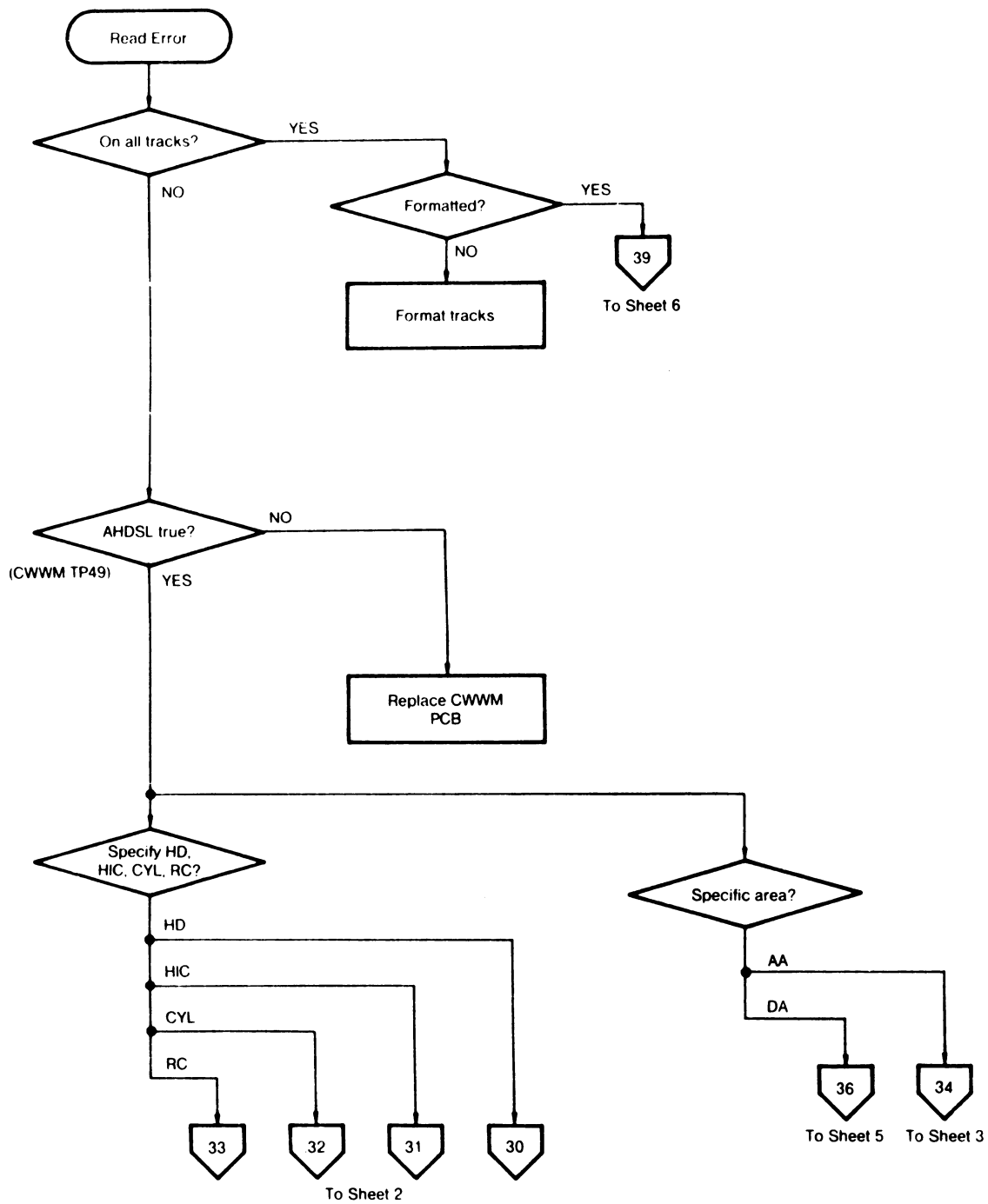
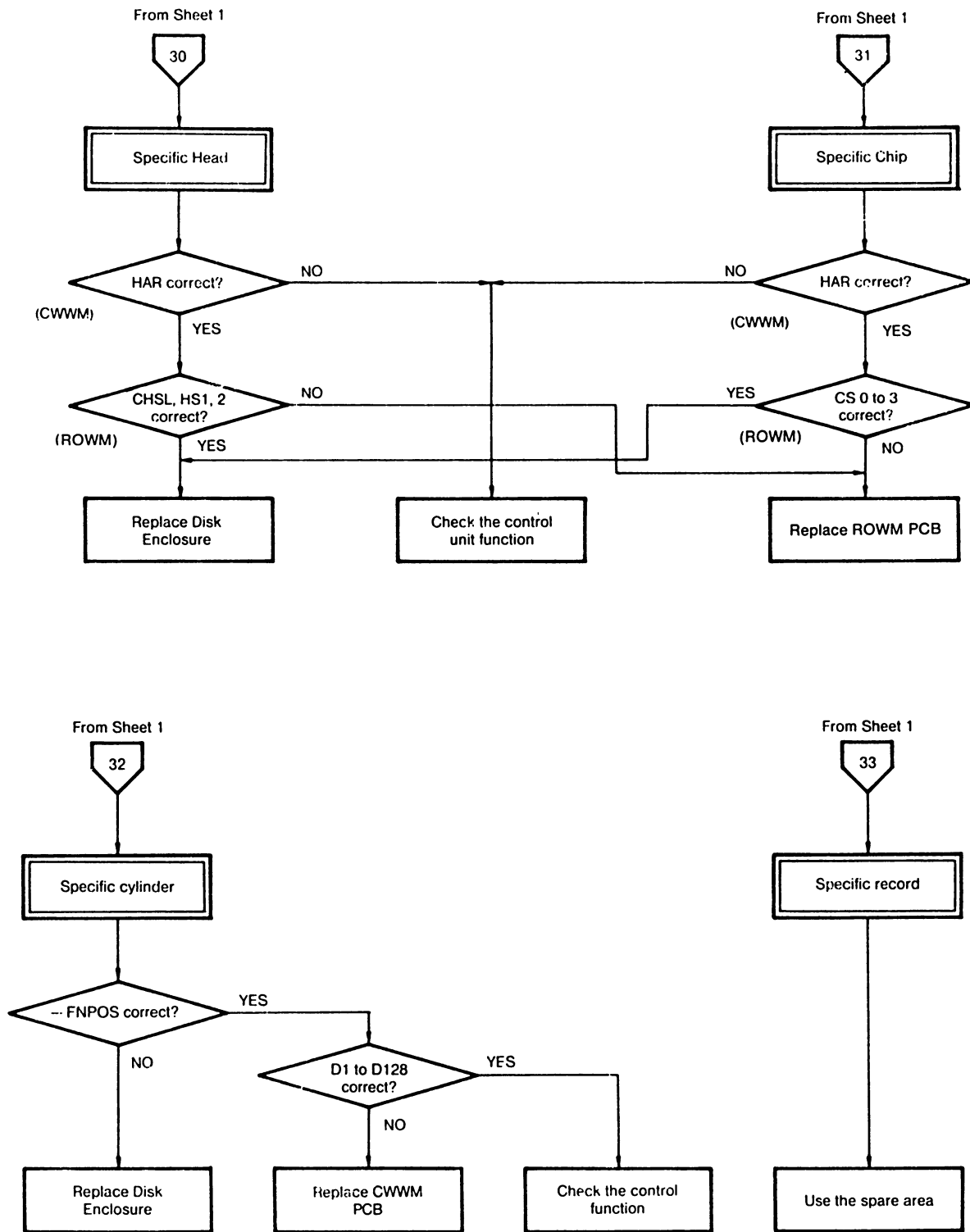


Figure 5.4.3 Seek Error Flow Chart (Sheet 6 of 6)



Note: AA is Address Area.
DA is Data Area.

Figure 5.4.4 Read Error Flow Chart (Sheet 1 of 6)



Note: One chip has four heads.

CS 0: HD0 to 3
 1: HD4 to 7
 2: HD8 to 11
 3: HD12 to 15

Figure 5.4.4 Read Error Flow Chart (Sheet 2 of 6)

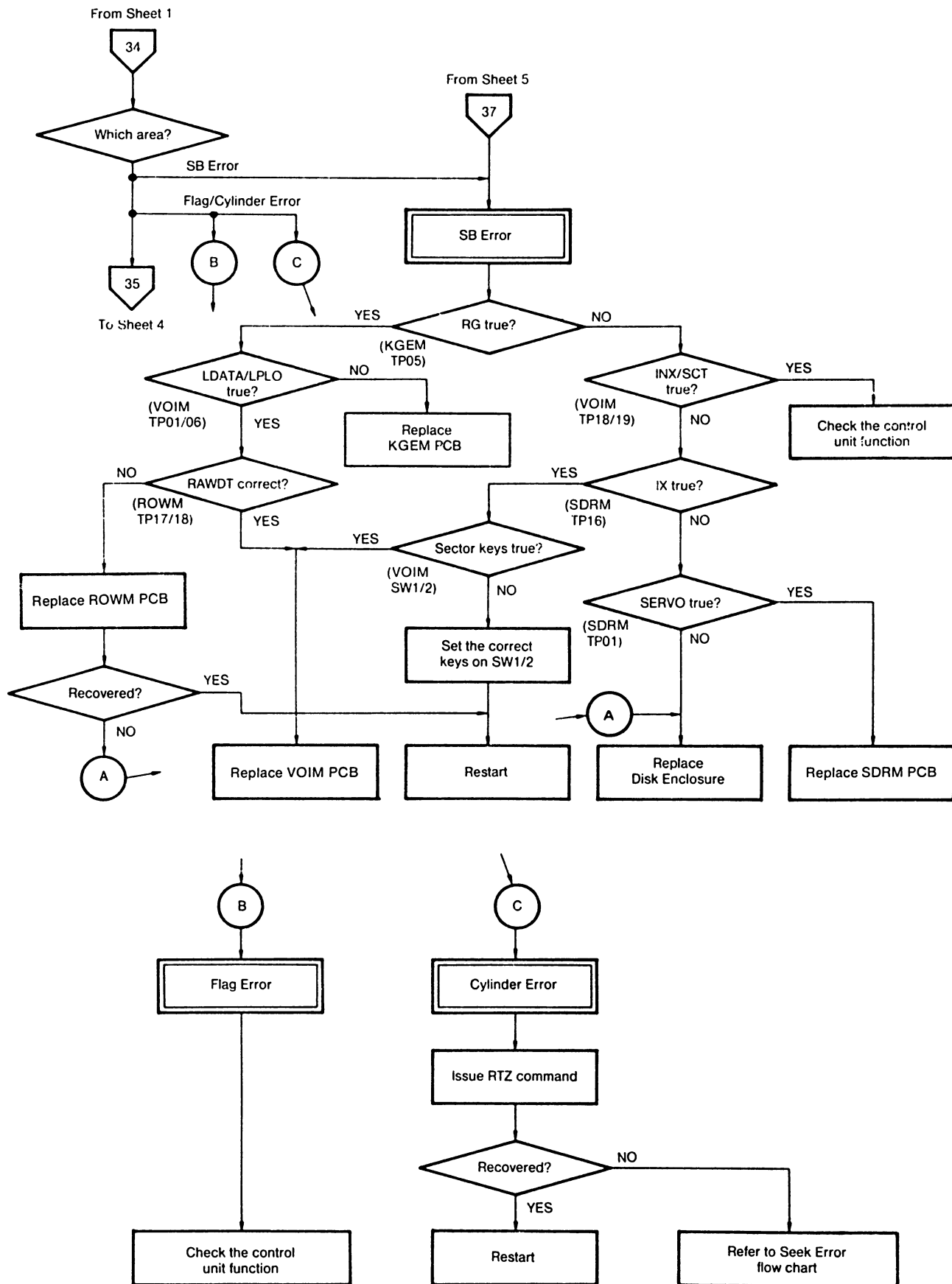


Figure 5.4.4 Read Error Flow Chart (Sheet 3 of 6)

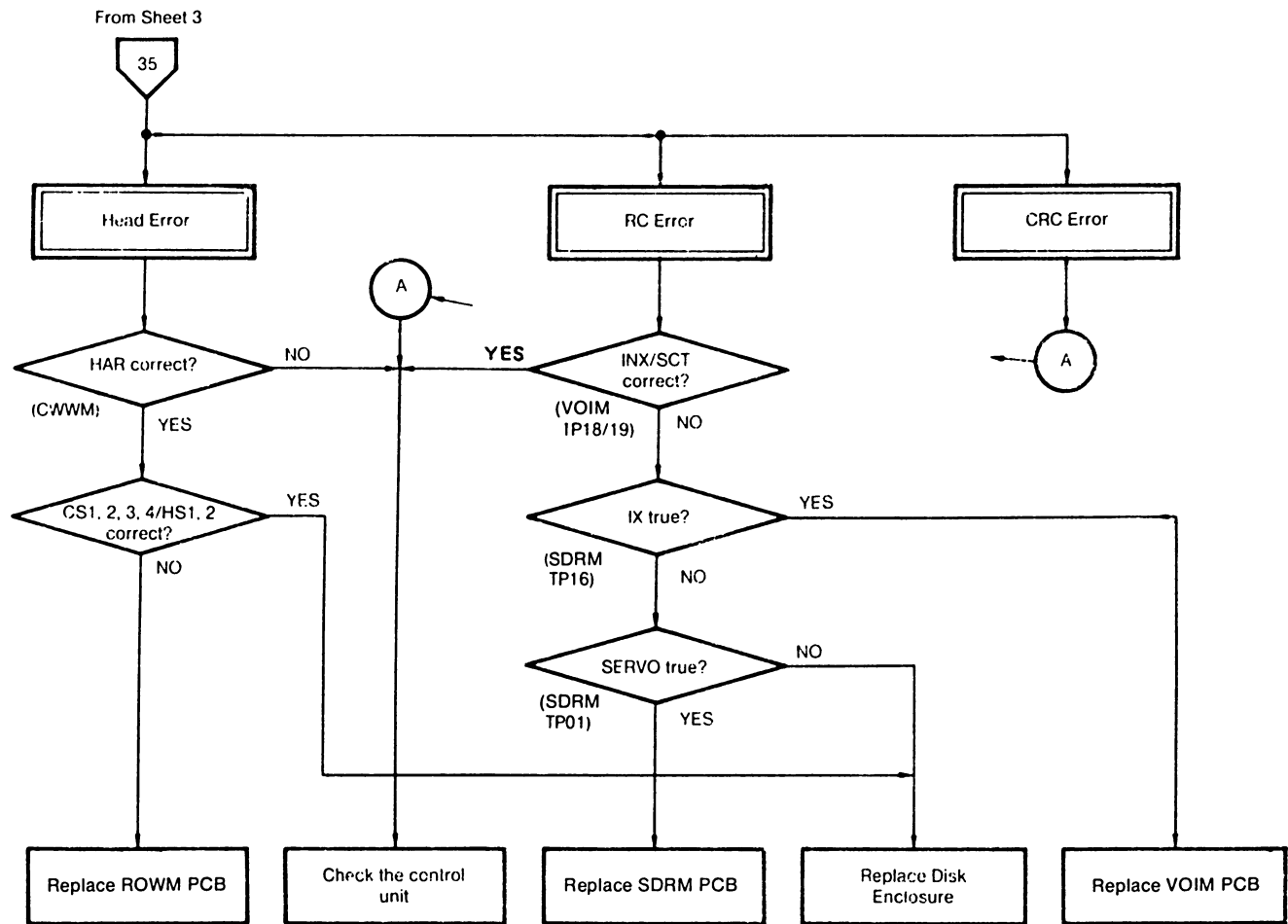


Figure 5.4.4 Read Error Flow Chart (Sheet 4 of 6)

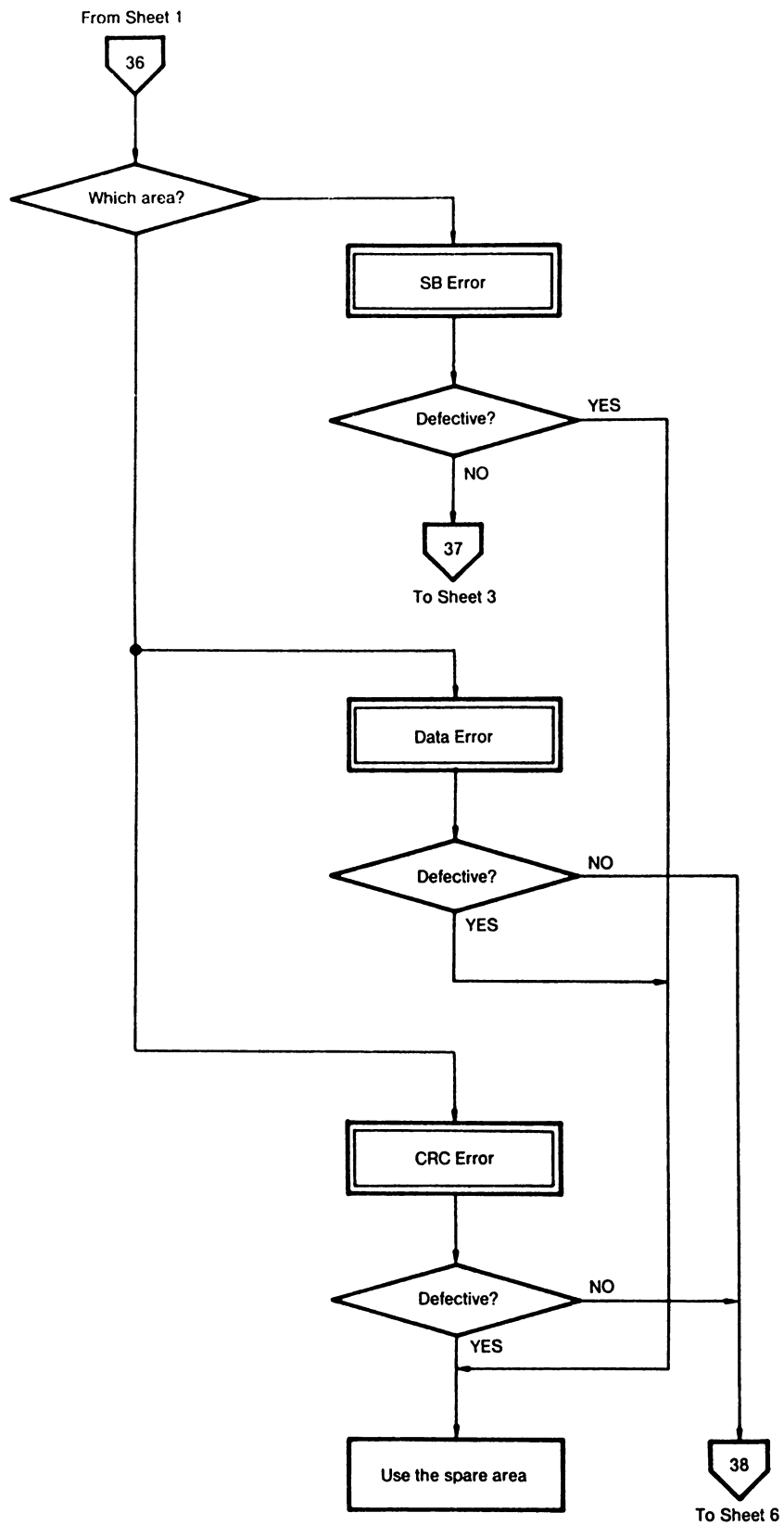


Figure 5.4.4 Read Error Flow Chart (Sheet 5 of 6)

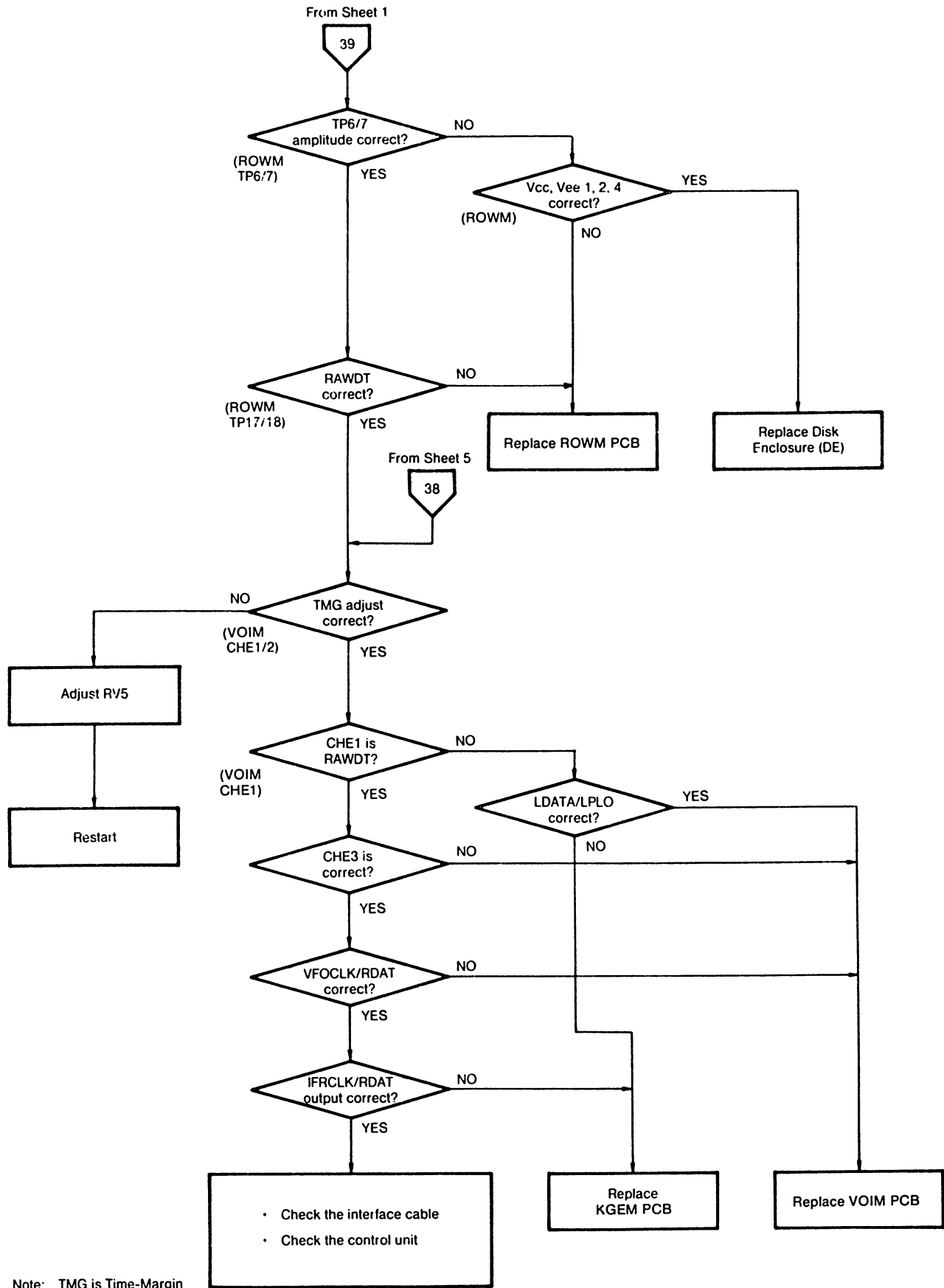


Figure 5.4.4 Read Error Flow Chart (Sheet 6 of 6)

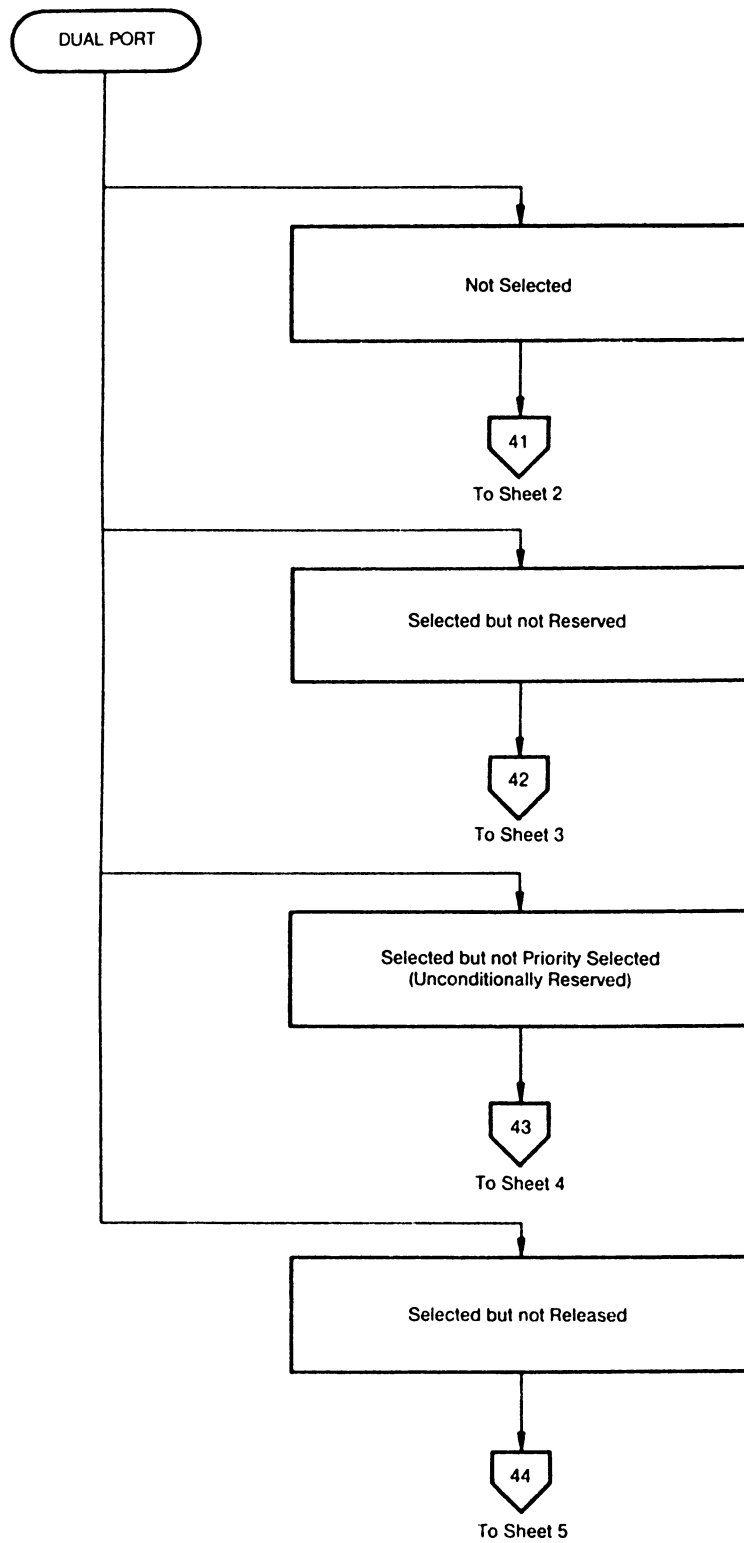


Figure 5.4.5 Dual Port Malfunction Flow Chart (Sheet 1 of 5)

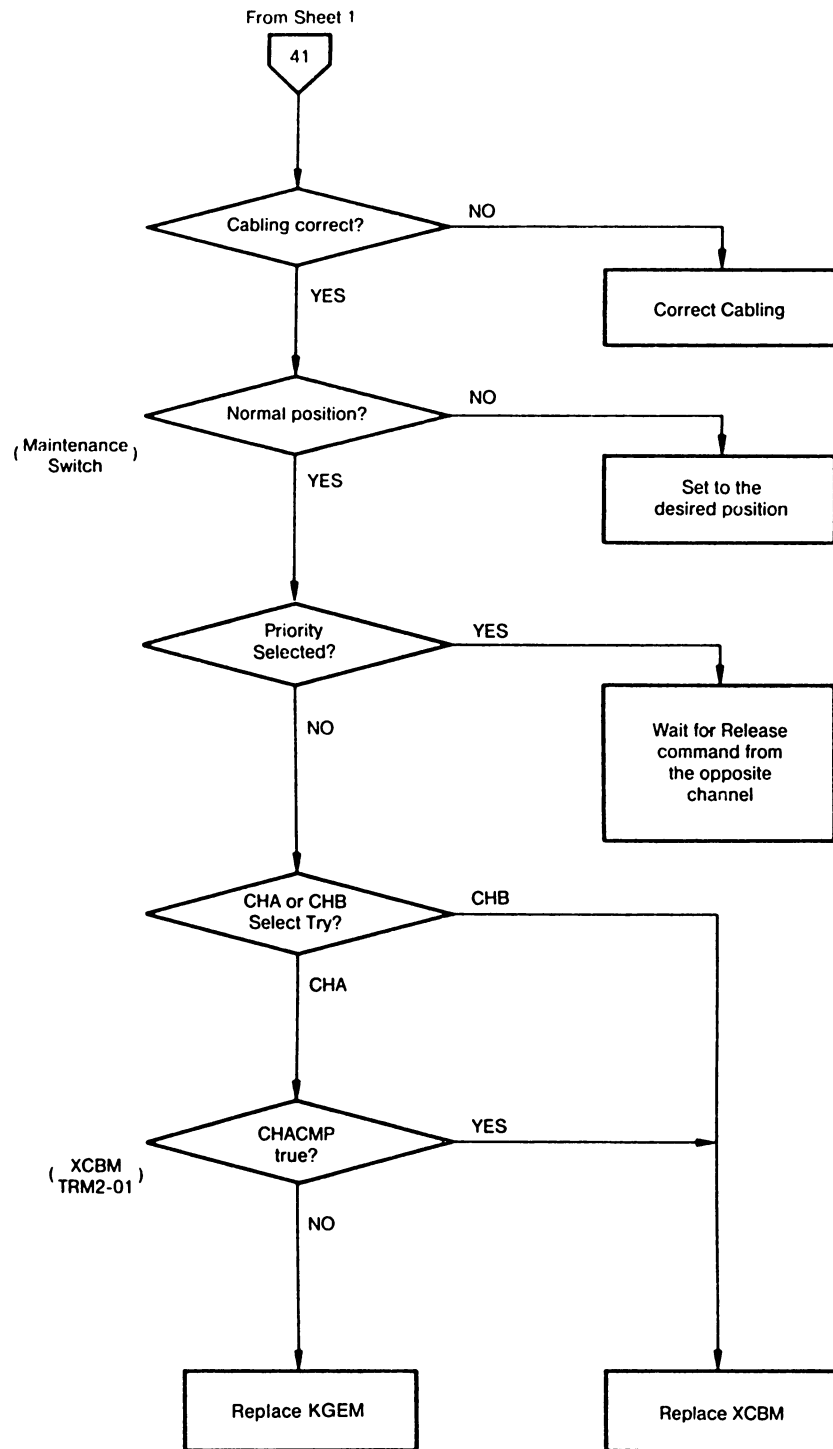


Figure 5.4.5 Dual Port Malfunction Flow Chart (Sheet 2 of 5)

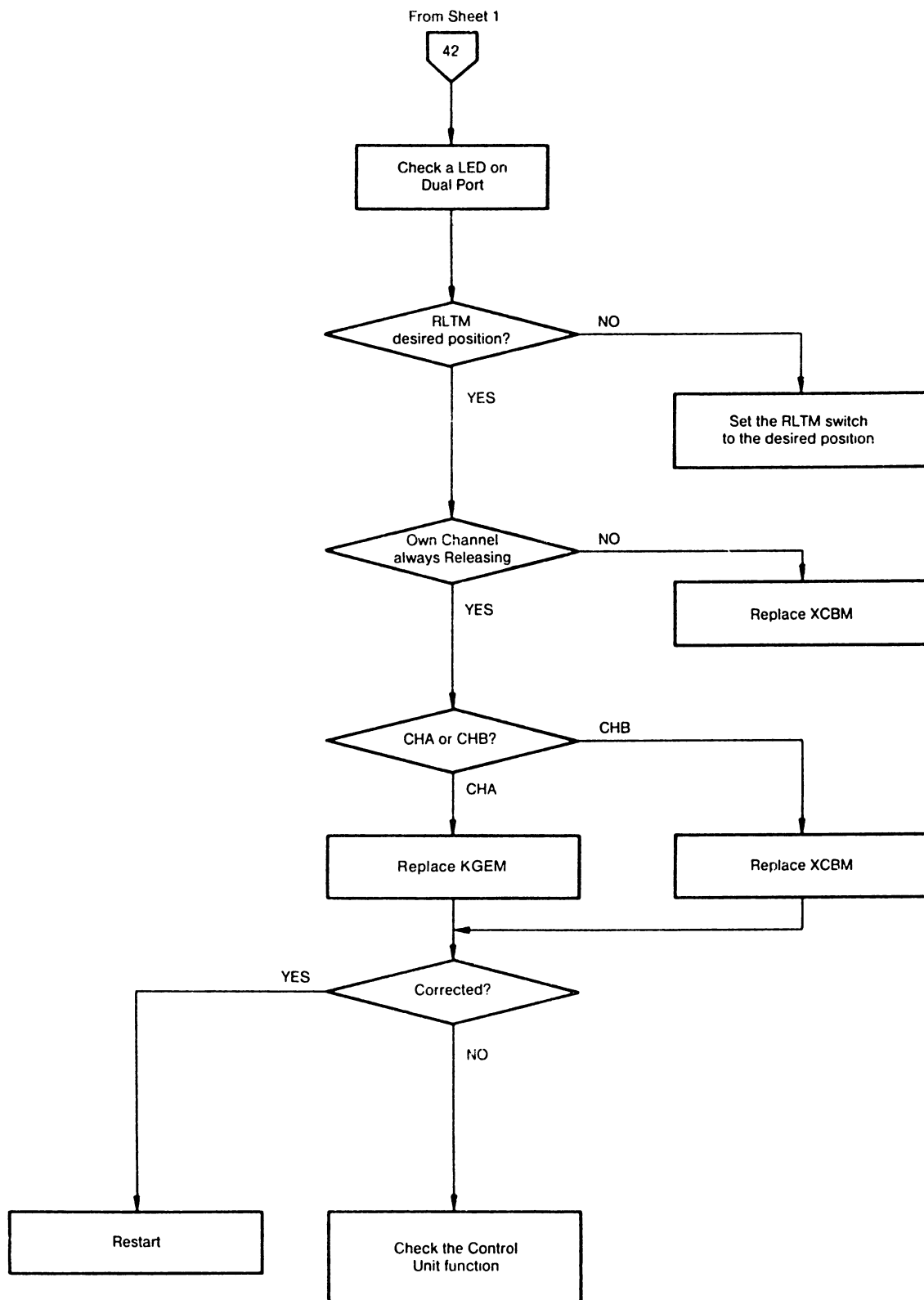


Figure 5.4.5 Dual Port Malfunction Flow Chart (Sheet 3 to 5)

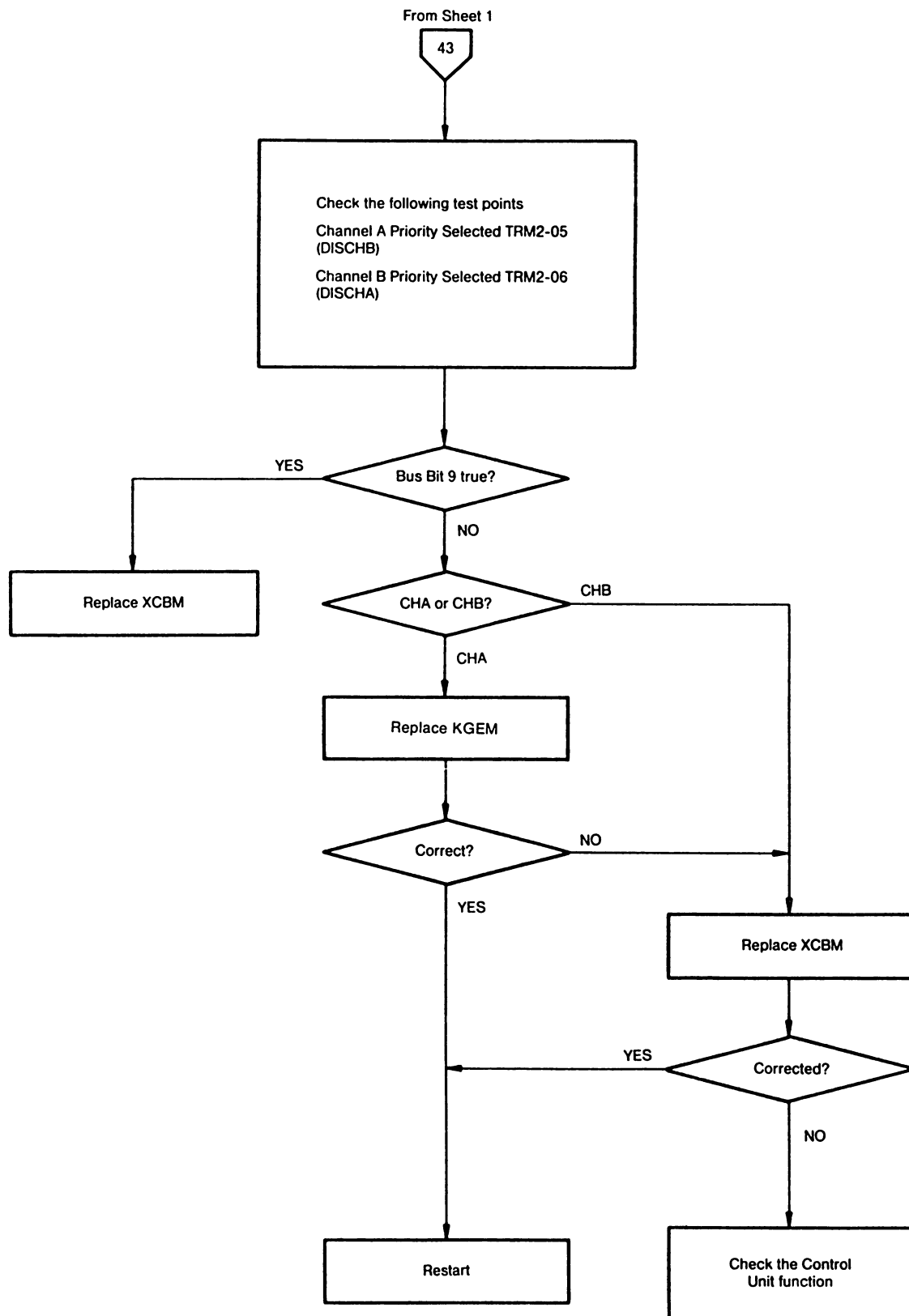


Figure 5.4.5 Dual Port Malfunction Flow Chart (Sheet 4 of 5)

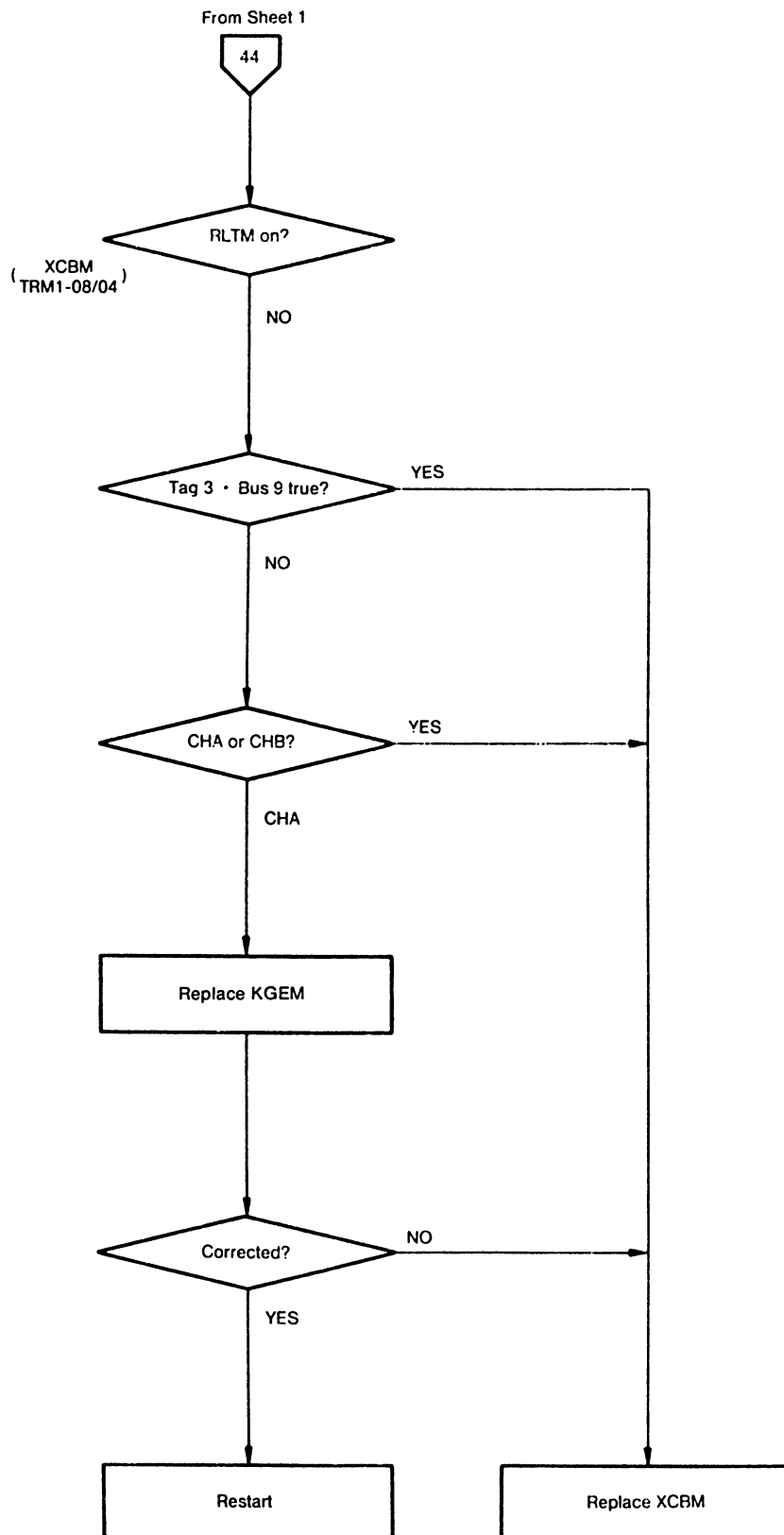


Figure 5.4.5 Dual Port Malfunction Flow Chart (Sheet 5 of 5)

Section 6

Maintenance

BLANK

6. MAINTENANCE

6.1 INTRODUCTION

This section covers maintenance of the unit, and is divided into General Precaution, Preventive Maintenance, Maintenance Equipment, Parts Replacement and Adjustment, and Electrical Checks and Adjustment items.

6.2 GENERAL PRECAUTIONS

6.2.1 Power ON/OFF

- (1) Visually check the condition of the device before turning the power on and off.
- (2) Before turning the power on after maintenance, check that all the printed-circuit boards are mounted in the correct position.

6.2.2 PCB Assembly and Connector Removal

- (1) Always turn the power off before removing and inserting printed-circuit boards and connectors.
- (2) Always insert the printed-circuit boards along the printed-circuit board guide.

6.2.3 Parts Replacement

- (1) Use screwdrivers, wrenches, and other tools matched to the size of the screws and bolts.
- (2) Do not leave removed screws in the device.
- (3) Tighten all the screws securely.

6.2.4 DE Replacement

- (1) A Disk Enclosure (DE) is sensitive to shock. Be careful when handling or replacing the DE. Do not apply a shock.
- (2) Use the specified packing box for a spare DE. When returning the replaced DE, put the DE into the specified packing box used for transporting.

6.2.5 Dual Port Switches

- (1) Turn the switches to the desired position according to system configuration.
- (2) After maintenance, turn the maintenance switch to the Normal A/B (NRA/NRB) position.

6.2.6 Others

- (1) Use test equipment that has been correctly calibrated.
- (2) Always record the data and its processing for later reference when trouble occurs.

6.3 MAINTENANCE TOOLS AND EQUIPMENT

Table 6.3.1 Maintenance Tools and Equipment

Tool and equipment	Model
Oscilloscope	TEKTRONIC 475, or equivalent
Oscilloscope probe (X10)	TEKTRONIX P6053B, or equivalent
Digital multimeter	
Extender	B16B-3190-0010A
Screwdriver	
Hexagon Wrench	
Wrench or crescent wrench	

6.4 PREVENTIVE MAINTENANCE

No special preventive maintenance is necessary.

6.5 MECHANICAL PARTS REPLACEMENT AND ADJUSTMENT

When replacing mechanical parts, always lock the spindle and actuator.

6.5.1 Disk Enclosure

The disk enclosure (DE) is attached to the sub-frame with three nuts. To replace the DE, proceed as follows:

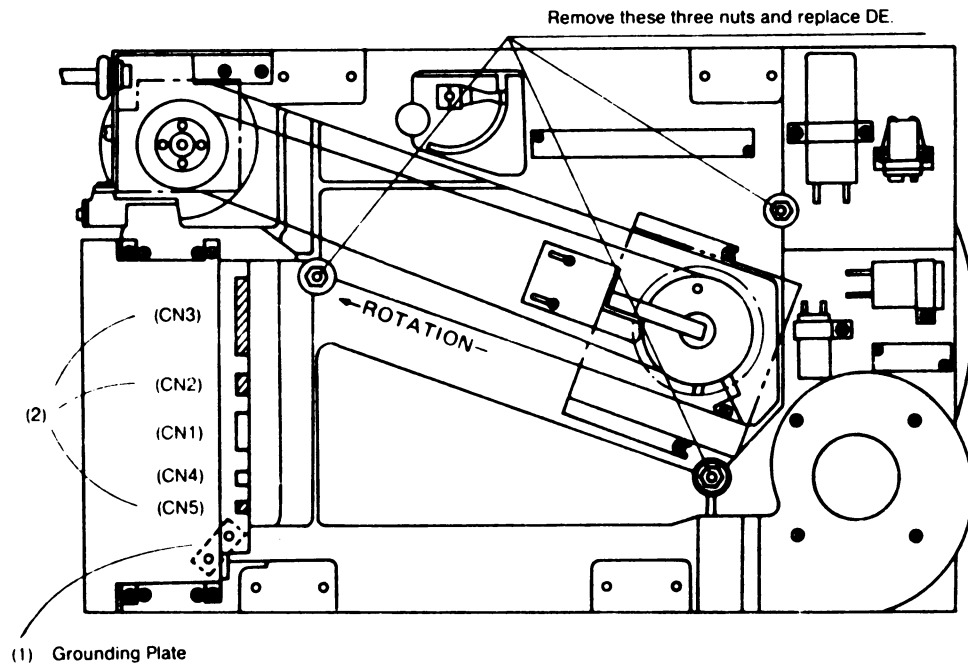


Figure 6.5.1 Disk Enclosure Replacement

(A) Removal

- (1) Remove grounding plate between gate shelf and sub-shelf of unit. (Top side)
- (2) Disconnect wiring (CN2, CN3, and CN5) from the gate shelf.
- (3) Lock actuator. (Refer to 3.4.4)
- (4) Remove belt in accordance with 6.5.4.
- (5) Remove three nuts shown in Figure 6.5.1 from rear of sub-frame.
- (6) Remove DE by lifting it slowly, being careful not to damage any of the wires.

Note: Be careful not to lose disk enclosure isolating bushing (polyacetal: white) and rubber packing when replacing disk enclosure. Refer to Figure 6.5.2.

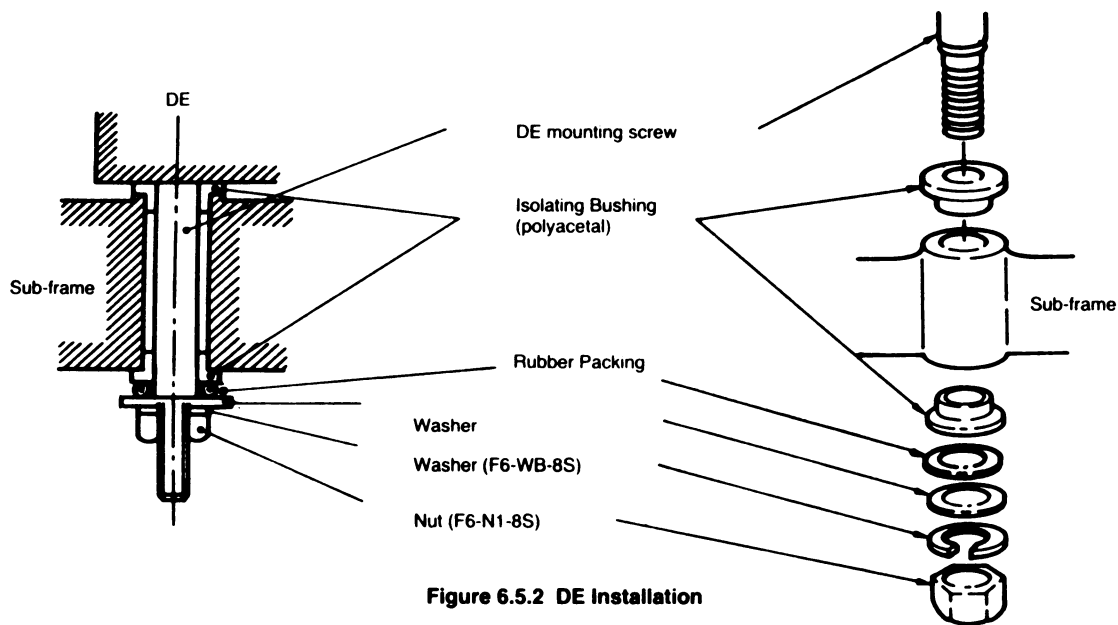


Figure 6.5.2 DE Installation

(B) Installation

- (1) Fasten Disk Enclosure to the sub-frame as illustrated in Figure 6.5.2.
- (2) Install belt in accordance with paragraph 6.5.4.
- (3) Unlock actuator (See paragraph 3.4.4).
- (4) Fasten connectors (CN2, CN3, CN5) coming from disk enclosure.
- (5) Install grounding plate between gate shelf and sub-shelf of the unit.

Note: After DE replacement, the adjustments of SDRM PCB assembly may be required as described in 6.6.3.1 to 6.6.3.3.

6.5.2 Spindle Drive Motor

The spindle drive motor is fastened to the sub-frame.

To replace this motor, proceed as follows:

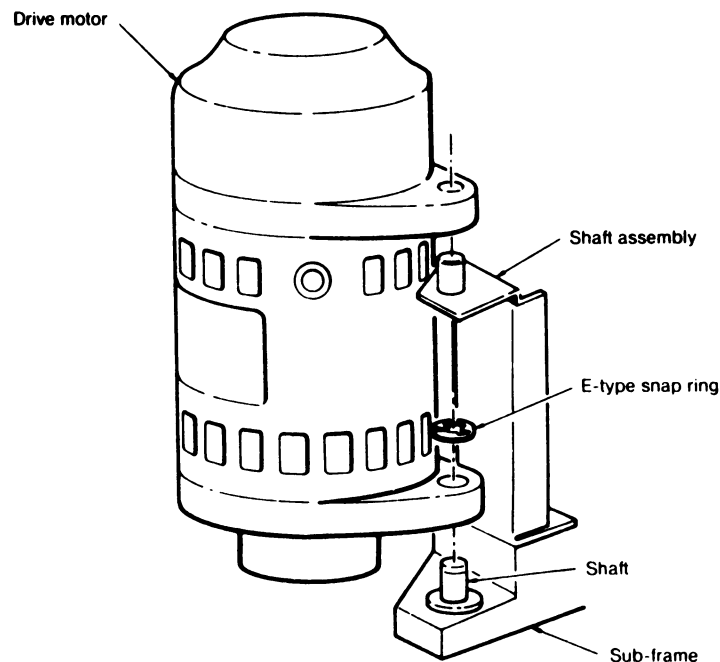


Figure 6.5.3 Disk Drive Motor Replacement

- (A) Removal
 - (1) Disconnect motor cable from TRM2.
 - (2) Remove belt in accordance with paragraph 6.5.4.
 - (3) Remove E-type snap ring shown in Figure 6.5.3, and pull out the motor from shaft.
- (B) Installation
 - (1) Install motor, and fasten it to shaft with E-type snap ring shown in Figure 6.5.3.
 - (2) Install belt in accordance with paragraph 6.5.4.
 - (3) Connect motor cable by terminal numbers of TRM2.

6.5.3 Motor Pulley Replacement

To replace the motor pulley and change from 60Hz to 50Hz, proceed as follows:
Refer to Figure 6.5.4.

- (A) Removing motor pulley
 - (1) Remove belt in accordance with paragraph 6.5.4.
 - (2) Loosen and remove two screws A.
 - (3) Insert removed screws A into screw holes in holder A, and remove the holder A by tightening screws alternately.
 - (4) Loosen and remove two screws A from holder A.
 - (5) Insert removed screws A into screw holes in pulley, and remove the holder B for top-ward by tightening screws alternately.
 - (6) After removing holder A and holder B, remove pulley from motor shaft. See Figure 6.5.4.
- (B) Installing motor pulley
 - (1) Check line frequency. Large diameter of pulley is for 50Hz and small diameter is for 60Hz. Refer to Pulley Label.
 - (2) Insert holder A and holder B into taper of pulley and align holes of pulley with holes of holder A and screw holes of holder B. (Holder A must be inserted into taper of pulley on opposite side of specified frequency.)
 - (3) Pass screws A through holes of holder A and tighten with holder B loosely.
 - (4) Insert the pulley onto motor shaft with specified frequency side on top, and set "B" surface of pulley with "A" surface of motor shaft.
 - (5) Fasten the pulley to motor shaft by tightening screws A alternately.
 - (6) Insert belt in accordance with paragraph 6.5.4. Belt must be at center of pulley when it is rotating.

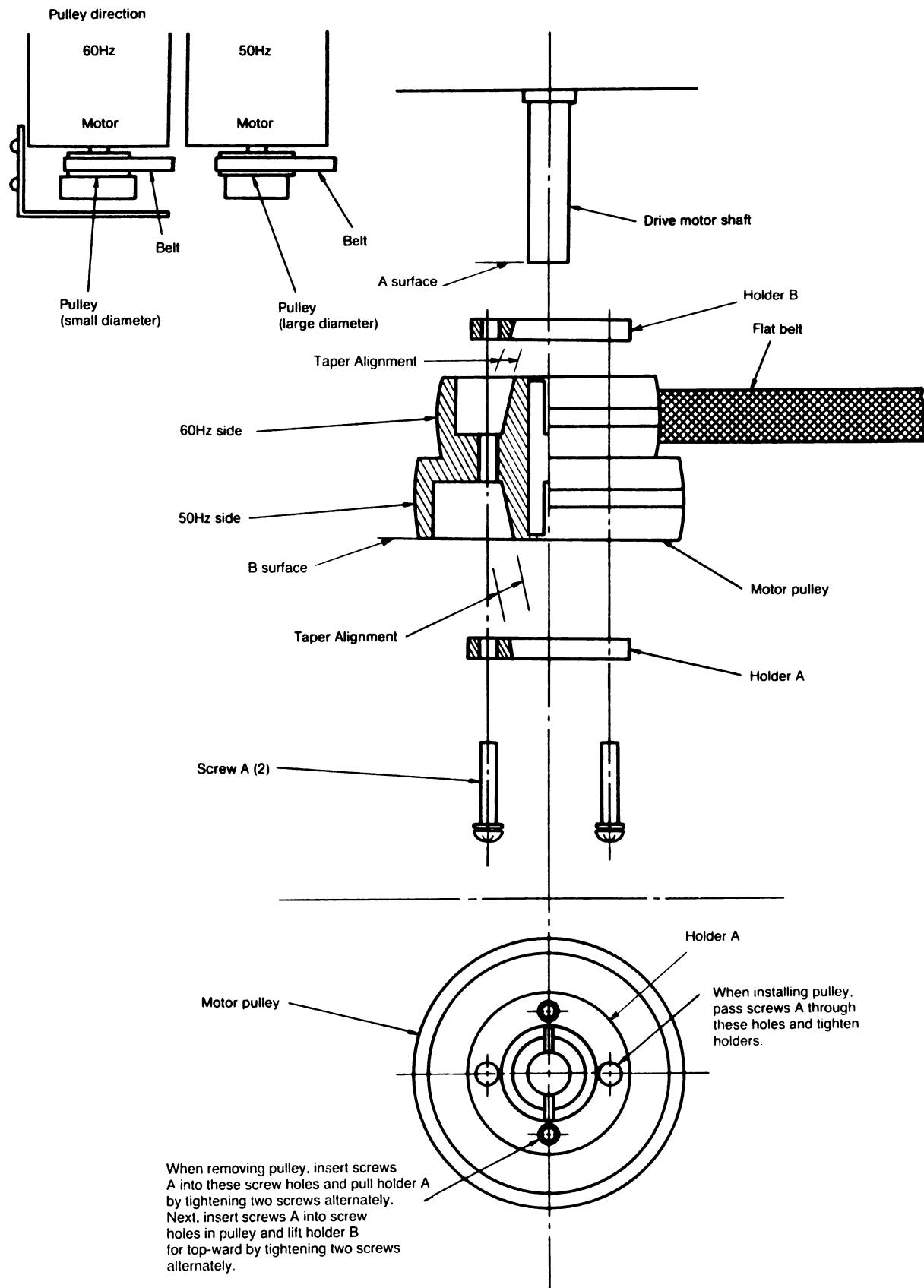


Figure 6.5.4 Motor Pulley Replacement

(C) Readjustment of belt tension

After changing the motor pulley to meet a different power line frequency, make it a rule to readjust belt tension.

Tension adjustment label is located beside the side of the slider (see Figure 6.5.5). Adjust belt tension with screw "D" so that the rear edge of the slider is aligned to proper reference line of tension adjustment label.

According to power line frequency and type of device installation, there are four setting positions (reference lines). The relation between installation position and line frequency is shown on pulley label put on motor cover. Pulley label is shown in Figure 6.5.6.

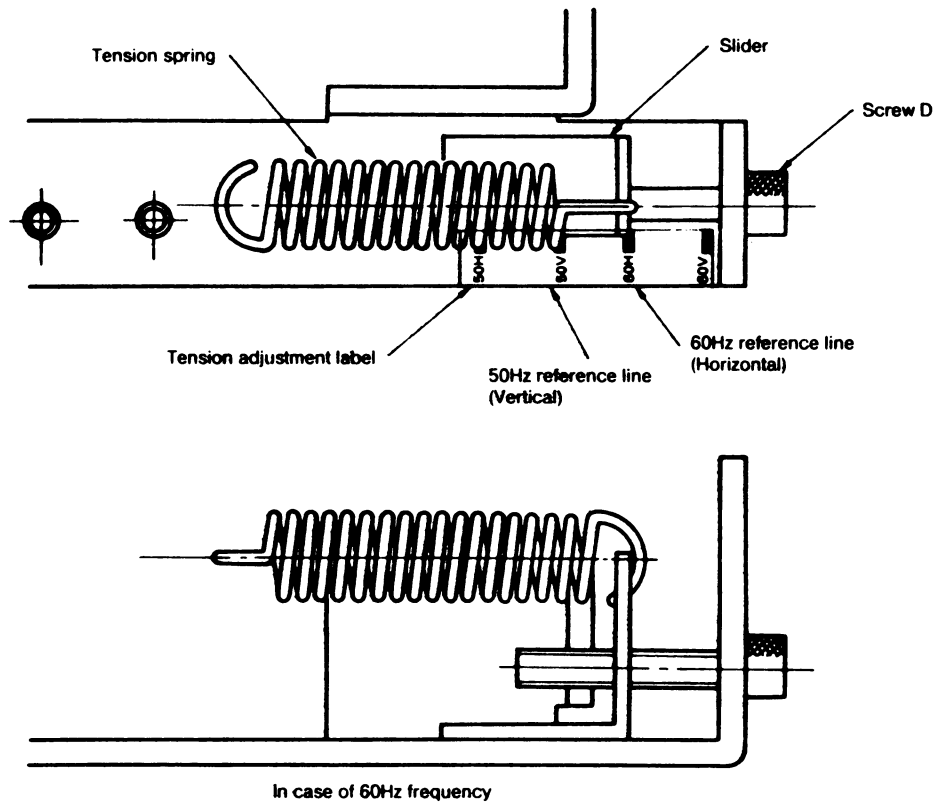


Figure 6.5.5 Belt Tension Adjustment

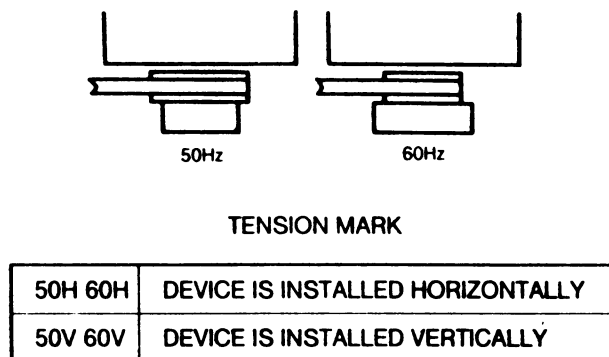


Figure 6.5.6 Pulley Label

6.5.4 Belt Replacement

To replace belt proceed as follows:

(A) Removing belt

- (1) Loosen screws "B" (2) and remove screws "C" (2) shown in Figure 6.5.7, and remove spindle cover and motor cover.
- (2) Lock spindle (see paragraph 3.4.3).
- (3) Loosen belt by loosening screw "D" of Figure 6.5.6 with a hexagon wrench, and remove belt.

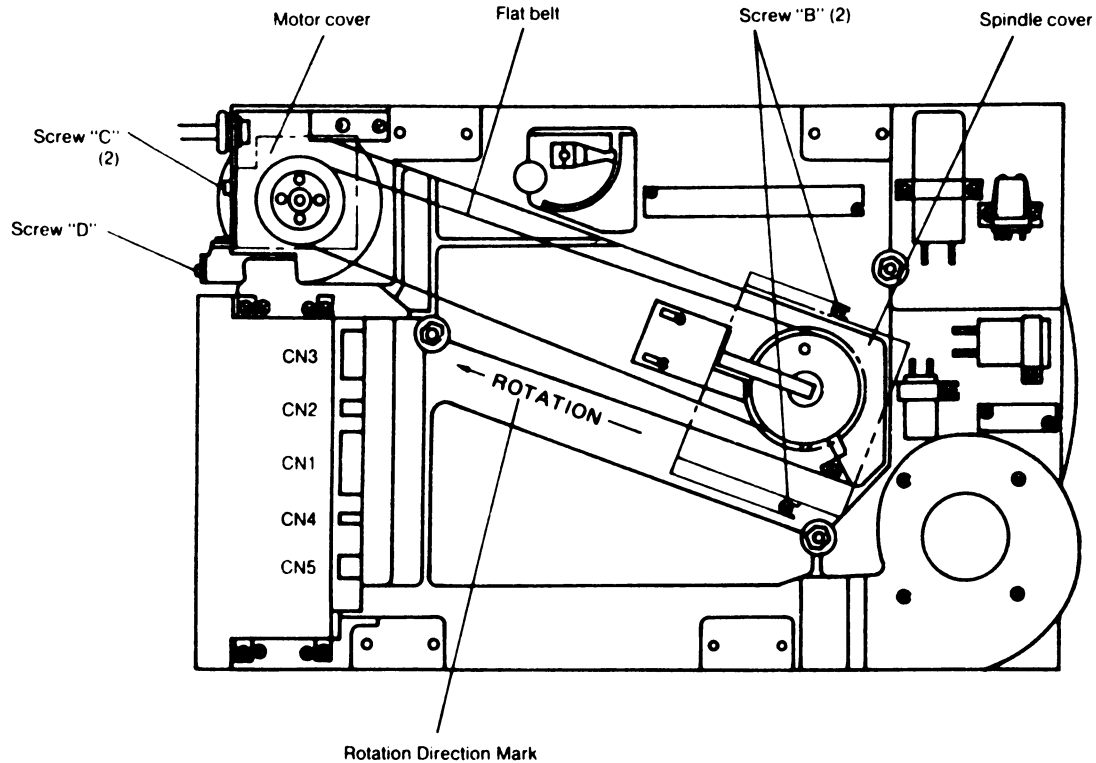


Figure 6.5.7 Belt Replacement

(B) Installing belt

- (1) Position the belt, and adjust belt tension. Adjust belt tension with screw "D" so that the rear of slider is aligned to the correct line on the tension adjustment label as shown in Figure 6.5.5.
- (2) Unlock spindle (see paragraph 3.4.3).
- (3) Adjust spindle grounding in accordance with paragraph 6.5.5.
- (4) Install motor cover and spindle cover.

6.5.5 Spindle Grounding Plate (Anti-static Brush)

To replace and adjust spindle grounding plate proceed as follows (see Figure 6.5.8).

(A) Replacement

Spindle grounding plate is replaced by removing screw "E" (2).

(B) Installation and adjustment

Confirm that the center of the spindle shaft is at the center of the spindle grounding contact, and tighten spindle grounding plate.

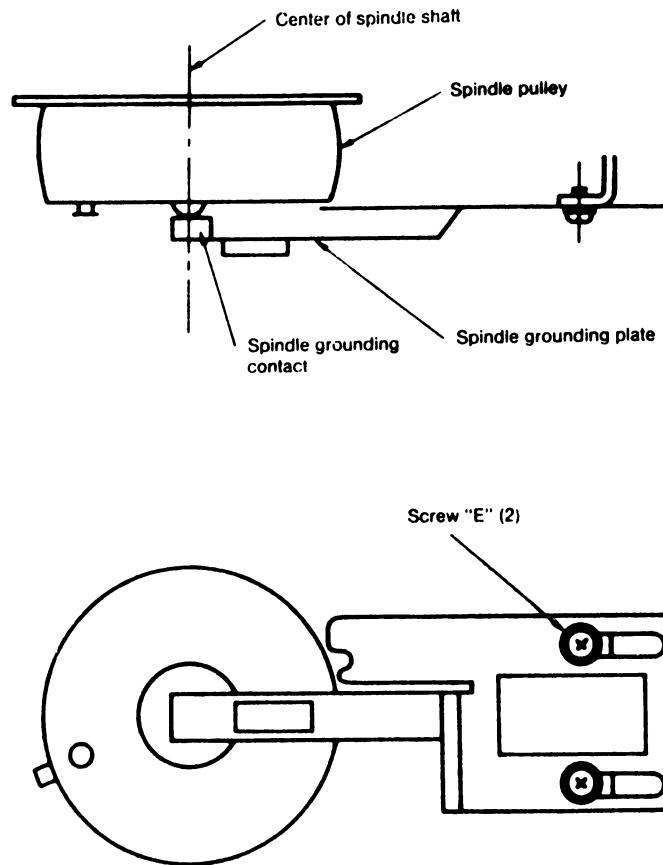


Figure 6.5.8 Spindle Grounding Plate Replacement and Adjustment

6.5.6 Speed Transducer

The speed transducer is used to detect the speed by detecting the projection attached to the spindle pulley.

(A) Removal

- (1) Remove disk enclosure as described in paragraph 6.5.1.
- (2) Loosen screw "F" (2) shown in Figure 6.5.9, and remove holder plate. At this time, also remove the speed transducer assembly.
- (3) Loosen screw "G" (2), and replace the speed transducer assembly.

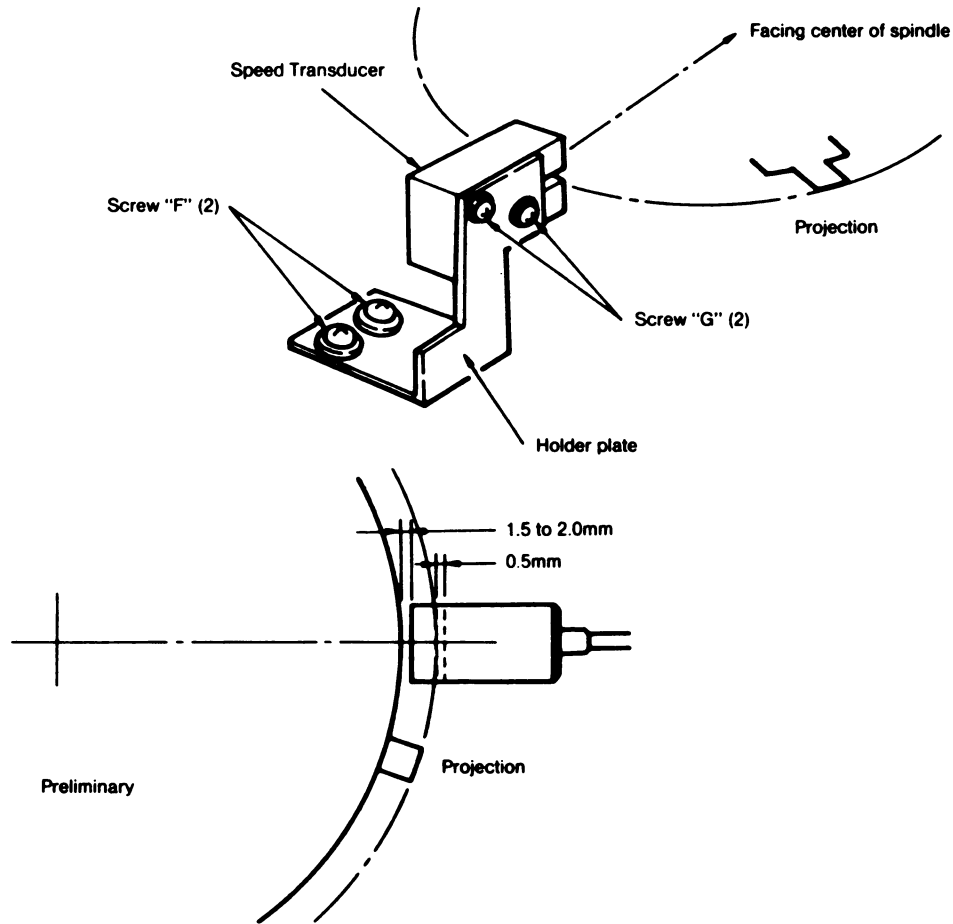


Figure 6.5.9 Speed Transducer

(B) Installation

- (1) When installing the speed transducer, adjust so that it does not touch the pulley and projection. Refer to Figure 6.5.9. Moreover, center of the speed transducer must be facing center of spindle. After adjustment, retighten screws.
- (2) Fasten Disk Enclosure to sub-frame as described in paragraph 6.5.1.
- (3) Rotate the spindle pulley by hand in proper direction and ensure that projection of the pulley does not contact the speed transducer. Also ensure that there is a gap (about 0.5mm) between the speed transducer and belt when the belt is shifted up to the speed transducer.

6.5.7 Blower Replacement

The blower is installed on the bottom, front of the sub-frame, and blows air through a duct in the sub-frame to cool the sub-frame, PCB assemblies and motor.

To replace the blower refer to Figure 6.5.10, proceed as follows:

(A) Removal

- (1) Disconnect blower cable from TRM3.
- (2) Remove screws "H" (4), and remove blower.

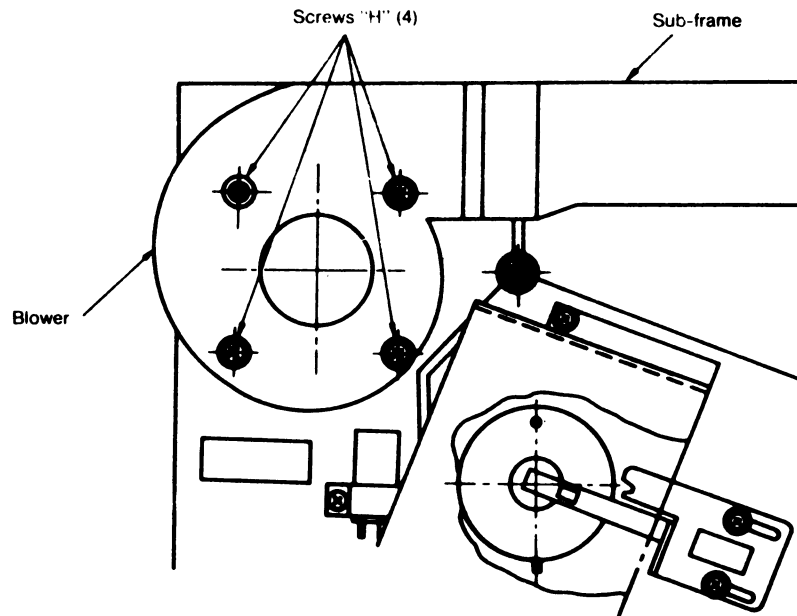


Figure 6.5.10 Blower Replacement

(B) Installation

- (1) When installing blower, be sure that outlet of blower is pushed tightly against duct so that there is no air leakage.
- (2) Connect blower cable by matching numbers on wires to terminal numbers of TRM3.

6.5.8 Brake Relay

Replace relay by removing holder. Remove holder by pulling it in directions of arrows in Figure 6.5.11.

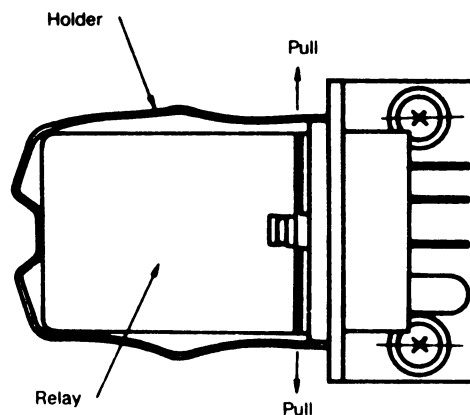


Figure 6.5.11 Relay Replacement

6.5.9 Dual Port Option

When the Dual Port option is replaced, perform the reverse procedure as described in Figure 3.4.9.

When the Cross-Call B (XCBM) PCB assembly is replaced, perform the following procedure:

- (1) Loosen two screws securing the cable holder, and remove the cable holder.
- (2) Disconnect the interface cables (OM1B, OM2B and OM3B) connecting to channel B.
- (3) Disconnect cables on connectors CN32 and CN34 from XCBM PCB assembly.
- (4) Remove the cover by loosening the three screws.
- (5) Disconnect a cable on connector CN31 connecting KGEM PCB assembly.
- (6) Remove XCBM PCB assembly by removing the four screws.
- (7) Reposition the spare XCBM PCB assembly by reverse procedure items (1) to (6). Refer to Figure 6.5.12.

After replacement, fully check the switches for their modes and cables for their connections.

Caution: When connecting the 10-pin cable to CN32, see that this cable does not interfere with FPT (File Protect) switch function.

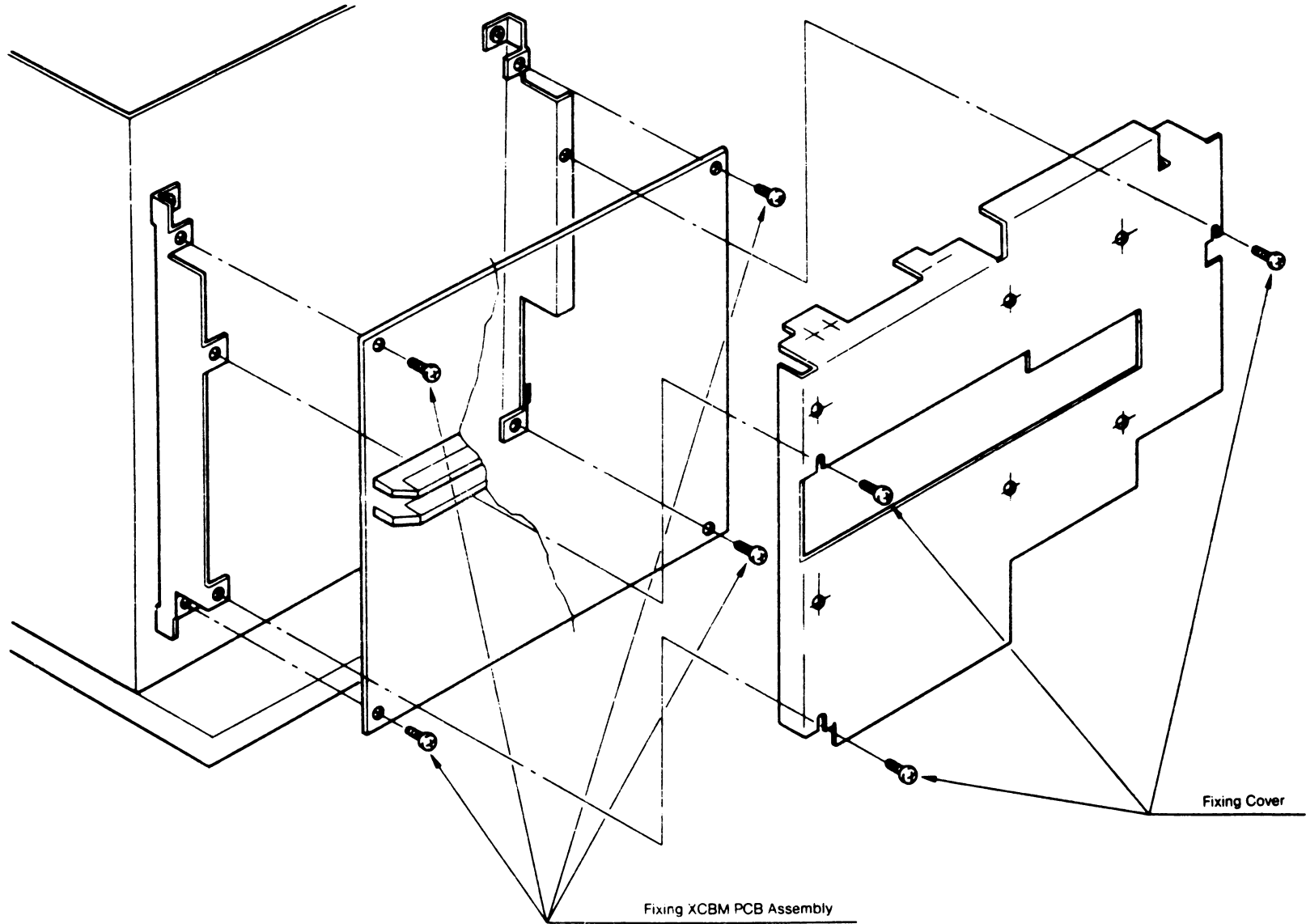


Figure 6.5.12 XCBM PCB Assembly Replacement

6.6 PCB ASSEMBLY REPLACEMENT/ADJUSTMENT

6.6.1 PCB Assembly Arrangement

The following Printed Circuit Board assemblies are mounted in the PCB chassis. To remove these PCB's, remove the top cover of the PCB chassis by loosening to screws, and then pull the levers on the PCB assemblies.

The PCB arrangement of the FDU M2298 is shown in Table 6.6.1.

Table 6.6.1 PCB Arrangement

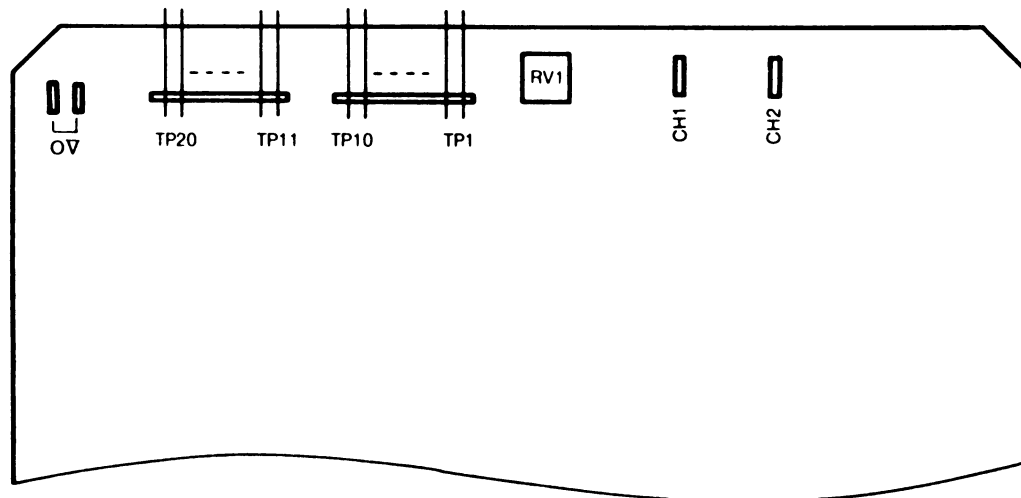
	M2294	Function
PCB Chassis	ROWM	Read/Write Circuit
PCB Chassis	SDRM	Servo Circuit
	CWWM	Seek Control
	VOIM	VFO
	KGEM	Interface Control

6.6.2 Test Point Arrangement on the PCB

Each PCB assembly is provided with test points and potentiometers to check and/or adjust the circuit functions.

(1) ROWM PCB

The test points and potentiometers are located on the ROWM PCB assembly as shown in Figure 6.6.1.



Note: No Adjustments are required when the PCB is replaced

Figure 6.6.1 ROWM PCB Test Points

Table 6.6.2 ROTM PCB Test Points

TP NO.	ABBREVIATION	SIGNAL NAME	SCHEMATIC PAGE CODE
(CH1) 1	WC A	Write Current A	EA1
(CH1) 2	WC B	Write Current B	EA1
3	*DIGLT	Diag Latch	EA1
4	IWS		EA1
5	*WECHO	Write Echo - Unsafe	EA1
6	PROT 1	Pre-Amp Output 1	EA2
7	PROT 2	Pre-Amp Output 2	EA2
8	AGCOT 1	AGC Output 1	EA2
9	AGCOT 2	AGC Output 2	EA2
10	INTLT 1	Integrator 1	EA2
11	INTLT 2	Integrator 2	EA2
12	SMPCK	Sample Clock	EA2
13	PLSH 2	Pulse Shaper 2	EA2
14	PLSH 1	Pulse Shaper 1	EA2
15	DFROT 2	Diff. Output 2	EA2
16	DFROT 1	Diff. Output 1	EA2
17	RAWDT	Raw Data 1	EA2
18	*RAWDT	Raw Data 2	EA2
19	TEST	Power Ready	EA3
20	MSEL	Multi-Selected	EA3

The ROWM PCB assembly is provided with one potentiometers, however, no adjustments are required when the PCB is replaced. The potentiometer function is shown in Table 6.6.3.

Table 6.6.3 ROTM Potentiometer Function

Pot No.	Function/Adjustment	Reference TP
RV1	Data Head Write Current	TP1/TP2

(2) SDRM PCB

The test points, potentiometers, and switches are located on SDRM PCB assembly as shown in Figure 6.6.2.

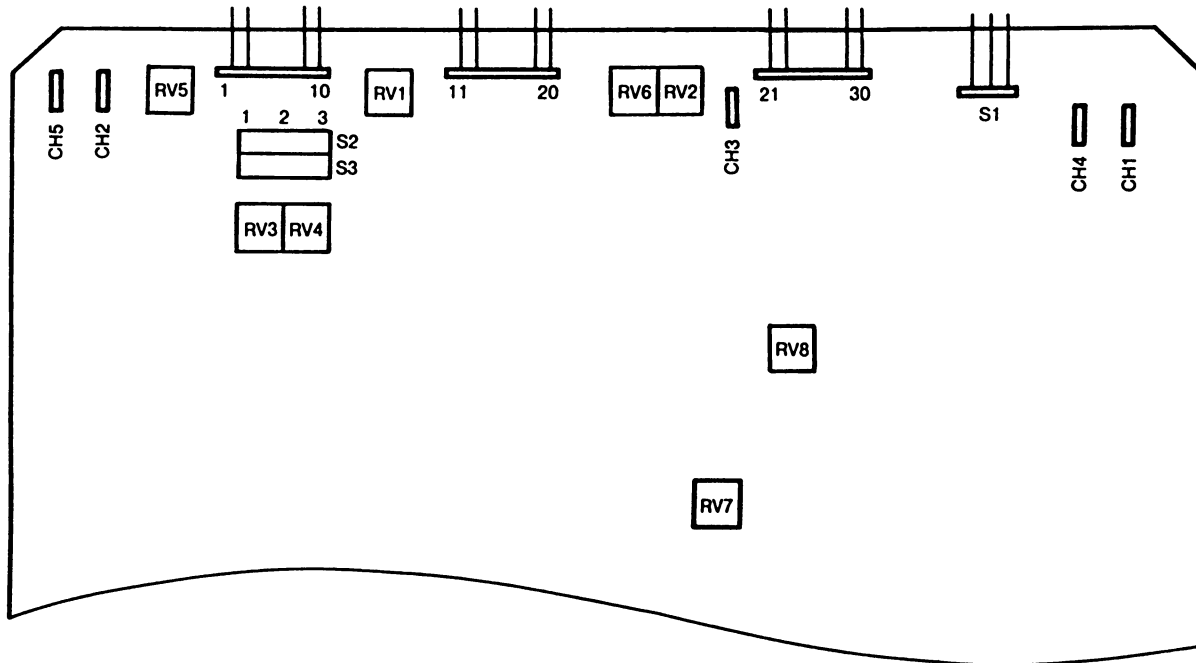


Figure 6.6.2 SDRM PCB Test Points

Each test point function is shown in Table 6.6.4.

Table 6.6.4 SDRM PCB Test Points and Check Terminals

TP NO.	ABBREVIATION	SIGNAL NAME	SCHEMATIC PAGE CODE
1	SERVO	Servo Signal	CA1
2	*GT1	Gate 1	CA2
3	*GT4	Gate 4	CA2
4	AGC	AGC Control	CA3
5	PLOVC	PLO Control Voltage	CA2
6	SVSLT	Servo Slice Out	CA1
7	SVPWD	Servo Pulse Window	CA1
8	SVPL	Servo Pulse	CA1
9	PLOSS	PLO Single Shot	CA1
10	PLOL	PLO Latch	CA1
11	2 BYTCL	2 Byte Clock	CA2
12	POSN	Position Normal	CA3
13	POSQ	Position Quadrature	CA3
14	-FNPOS	Fine Position	CB1
15	*OFTRK	Off Track	CA3
16	IX	Index	CA2
17	TXPL	Track Crossing Pulse	CB3
18	DRLM	Drive Linear Motor	CB3
19	FWD	Forward Drive	CB3
20	V=0	Velocity=0	CB1
21	-VEL	Velocity	CB1

Table 6.6.4 SDRM PCB Test Points and Check Terminals (Continued)

TP No.	Abbreviation	Signal Name	Schematic Page Code
22	–ABSVL	Absolute Velocity	CB1
23	DA	DA Convertor	CB2
24	FUNC	Function	CB2
25	VER	Velocity Error	CB2
26	PER	Position Error	CB2
27	PADR	Power AMP Drive	CB4
28	CLDOS	Clamp Position	CB2
29	TVEL	Tach Velocity	CB4
30	CSNS	Current Sense	CC1
CH1	CLPOS	Clamp Position	CB2
CH2	N > Q	Normal > Quadrature	CA3
CH3	N + Q > 0	Normal + Quad > 0	CA3
CH4	FVEL	Fine Velocity	CB1
CH5	GBENB	Guard Band Enable	CA1

The SDRM PCB is provided with eight potentiometers and five selecting switches, however, only the three potentiometers (RV2, RV5 and RV6) must be adjusted when the PCB is replaced.

The potentiometer and switch functions are shown in Table 6.6.5 and 6.6.6.

Table 6.6.5 SDRM Potentiometer function

Pot No.	Function/Adjustment	Reference TP/S
RV1	VCO Control Voltage	TP5
RV2	Position Time*	(CWWM) CH7
RV3	Servo Pulse Window	TP7
RV4	PLO Single Shot	TP9
RV5	Position Signal Gain*	TP12
RV6	Over-shoot	TP14
RV7	DA Output	TP23
RV8	Fine Velocity	CH4

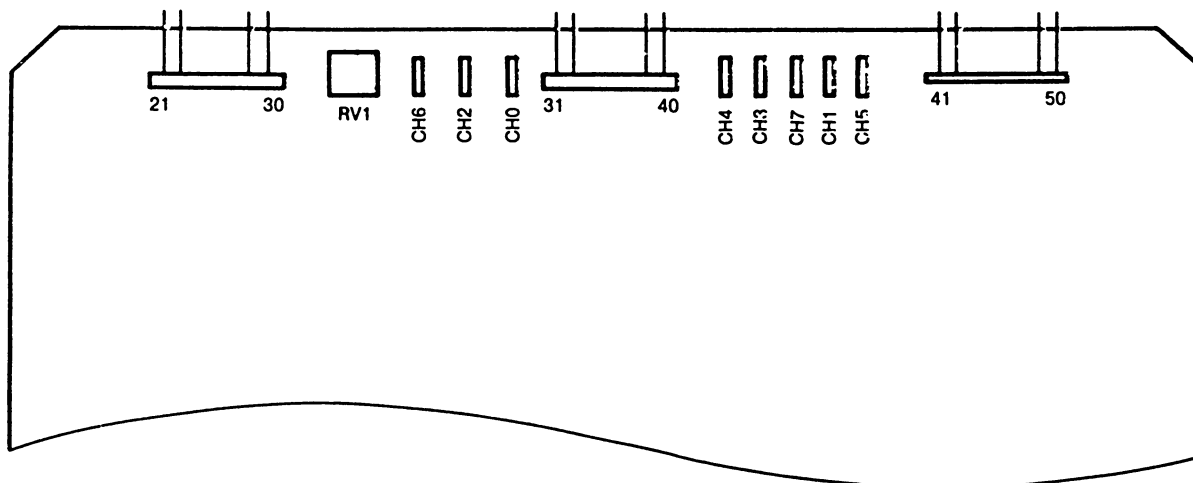
* The potentiometer RV2 and RV5 require adjustment when the SDRM PCB is replaced.

Table 6.6.6 SDRM Switch Function

Switch No.	Function	Reference TP
S1	Power Amp. Drive Cut	NONE
S2, S3	VCO Select	TP11

(3) CWWM PCB

The test points, check terminals and a potentiometer are located on CWWM PCB assembly as shown in Figure 6.6.3.



Note: No adjustments are required when the CWWM PCB assembly is replaced.

Figure 6.6.3 CWWM PCB Test Points

Each test point function is shown in Table 6.6.7 and 6.6.8.

Table 6.6.7 CWWM Check Terminals

CH No.	Abbreviation	Signal Name	Schematic Page Code
0	GND	Ground	—
1	*VFOFS	VFO Fast Sync	BC1
2	STL1	Settline 1	BE1
3	STL2	Settling 2	BE1
4	STL3	Settling 3	BE1
5	OVCYTM	Over Cylinder Timer	BE2
6	GBTM	Guard Band Timer	BE2
7	POSTM	Positioning Timer	BA1

Table 6.6.8 CWWM Test Points

TP No.	Abbreviation	Signal Name	Schematic Page Code
21	GND	—	—
22	OGB	Outer Guard Band	BG1
23	IGB 1	Inner Guard Band 1	BG1
24	IGB 2	Inner Guard Band 2	BG1
25	—	—	—
26	SKEND	Seek End	BE2
27	ONCYL	On Cylinder	BE2
28	URDY	Unit Ready	BE2
29	SKERR	Seek Error	BE2
30	SKC	Seek Complete	BE1
31	GND	—	—
32	SUBEN	Sub Enable	BD4
33	EVEN	Even	BD4
34	PSDR	Position Drive	BD4
35	LNMD	Linear Mode	BD4
36	—	—	—

Table 6.6.8 CWWM Test Points (Continued)

TP No.	Abbreviation	Signal Name	Schematic Page Code
37	DRLM	Drive Linear Motor	BD4
38	LSPD	Low Speed	BD4
39	FWDD	Forward Drive	BD3
40	*OVTXPL	Over Track Crossing	BD2
41	GND	—	—
42	TMOTP	Time Out Pulse	BD2
43	RTRM	Retract Mode	BD1
44	SEKM	Seek Mode	BD1
45	GTZM	Go To Zero Mode	BD1
46	*PLO 1B	PLO 1 Byte Clock	BC1
47	—	—	—
48	*OFACT	Offset Active	BB1
49	*FHDSL	Fixed Head Select	BB1
50	USLD	Unit Selected	BB1

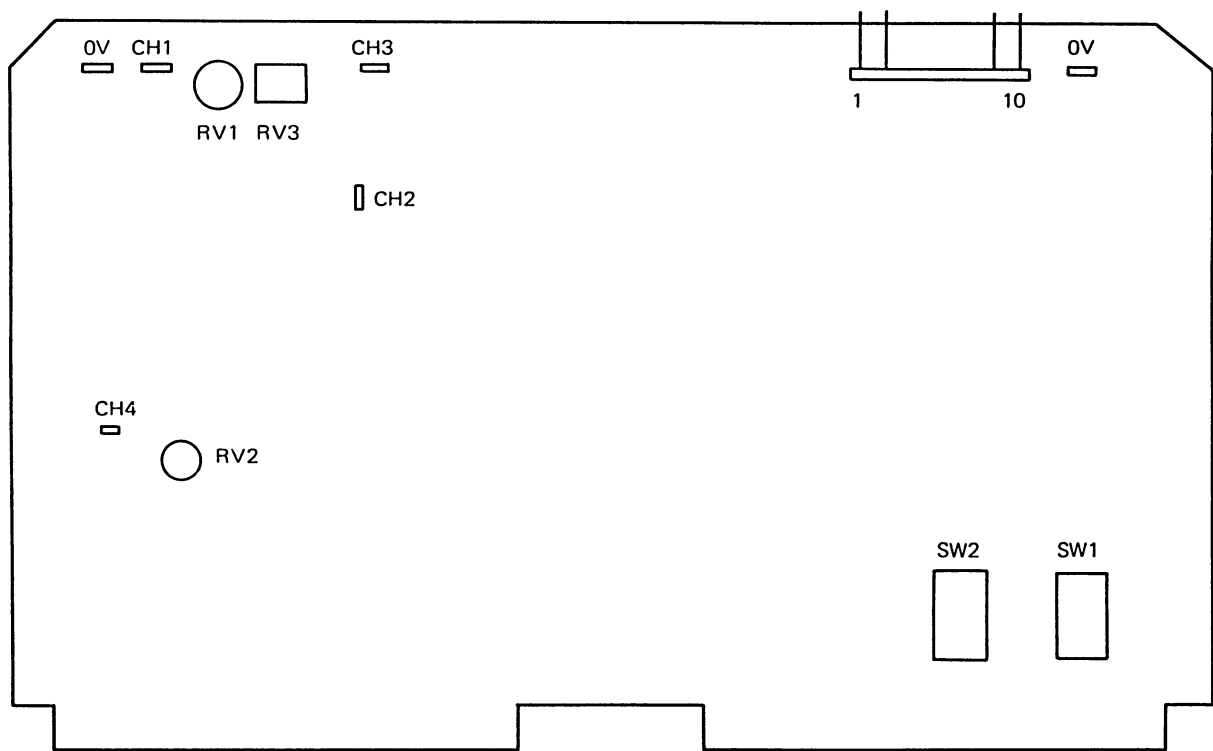
The CWWM PCB is provided with a potentiometer (RV1), however, no adjustment is required when the PCB is replaced. The potentiometer function is shown in Table 6.6.9.

Table 6.6.9 CWWM Potentiometer Function

Pot No.	Function/Adjustment	Reference CH
RV1	Settling Time 1	CH2

(4) **VOIM PCB**

The check terminals, switches, and potentiometers are located on the VOIM PCB assembly as shown in Figure 6.6.4



Note: SW1 and SW2 must be selected when the PCB is replaced.

Figure 6.6.4 VOIM PCB Test Points

Each test point function is shown in Table 6.6.10.

Table 6.6.10 VOIM Check Terminals

TP No.	Abbreviation	Signal Name	Schematic Page Code
1	*LDATA	Lock-To-DATA	DB1
2	RDAT	Read DATA	DD1
3	—	—	—
4	VFOCLK	VFO Clock	DD1
5	SET-ALL1	SET ALL 1	DD1
6	*LPLO	Lock-to-PLO	DB1
7	—	—	--
8	*SCT	Sector	DA1
9	—	—	—
10	*INX	Index	DA1

Table 6.6.10 VOIM Check Terminals (continued)

No.	Abbreviation	Signal Name	Schematic Page Code
CH1	DLDI	Delay Data	DE1
CH2	REFP	Reference Pulse	DE1
CH3	WND	Data Window	DE2
CH4	Vc	Control Voltage	DE3

The VOIM PCB assembly is provided with potentiometers and switches, however, no adjustments except SW1 and SW2 are required when the PCB is replaced. These functions are shown in Table 6.6.11.

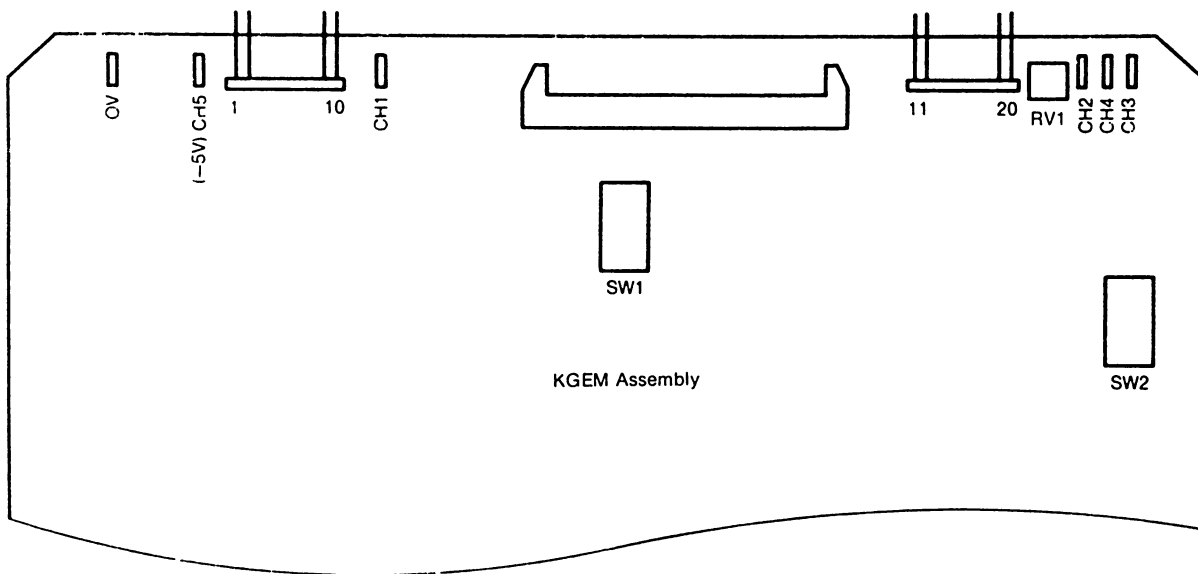
Table 6.6.11 VOIM Potentiometer/Switch Function

No.	Function/Adjustment	Reference TP
RV1	Reference Pulse Adjustment	CH2
RV2	VCO Adjustment	CH4
RV3	Delay Data One shot	CH1/CH3
S1	Sector Counting 1	TP8/TP10
S2	Sector Counting 2	TP8/TP10

(5) **KGEM PCB**

KGEM PCB assembly is for an interface control logic to support dual port or single port function.

The test points and potentiometers are located on the KGEM PCB assembly are shown in Figure 6.6.5. Each test point function is shown in Table 6.6.12.



Note No potentiometer adjustment is required when the PCB is replaced, however, the switch selecting should be performed to meet the customer's configuration

Figure 6.6.5 KGEM PCB Test Points

Table 6.6.12 KGEM Test Points

No.	Abbreviation	Signal Name	Schematic Page Code
TP1	GND	—	AA3
TP2	—	—	—
TP3	—	—	—
TP4	GND	—	—
TP5	RG	Read Gate	AF1
TP6	PWRCNF	Power Conflict	AD2
TP7	VCMHT	VCM Heat	AD2
TP8	—	—	—
TP9	INTMOT	Initial Time Out	AD2
TP10	DVCK	Device Check	AD2
TP11	GND	—	AA3
TP12	WENB	Write Enable	AD2
TP13	AHDSL	Access Head Select	AD1
TP14	INX	Index	AC1
TP15	SCT	Sector	AC1
TP16	START	Start	AB1
TP17	GBENB	Guard Band Enable	AB1
TP18	SPOK	Speed OK	AB1
TP19	—	—	—
TP20	CHAENB/ CHENB 2	Channel A Enable/ Channel Enable 2	AB1
CH1	*SPSG	Speed Signal	AB1
CH2	SPTM	Speed Timer	AB1
CH3	INHECH	Inhibit Echo	AD2
CH4	DLWG	Delayed Write Gate	AD2
CH5	—5V	—5V	AA3/AA2

The KGEM PCB is provided with a potentiometer (RV1) and switches. These functions are shown in Table 6.6.13.

Table 6.6.13 KGEM Potentiometer/Switch Function

No.	Function	Reference CH
RV1	Speed Timer	CH2
SW1	Disk Address	
SW2	Device Type/Sector Mode/TAG 4/5	

(6) XCBM PCB

XCBM PCB assembly is for the dual port function, the test points are located as shown in Figure 6.6.6, and each test point function is shown in Table 6.6.14.

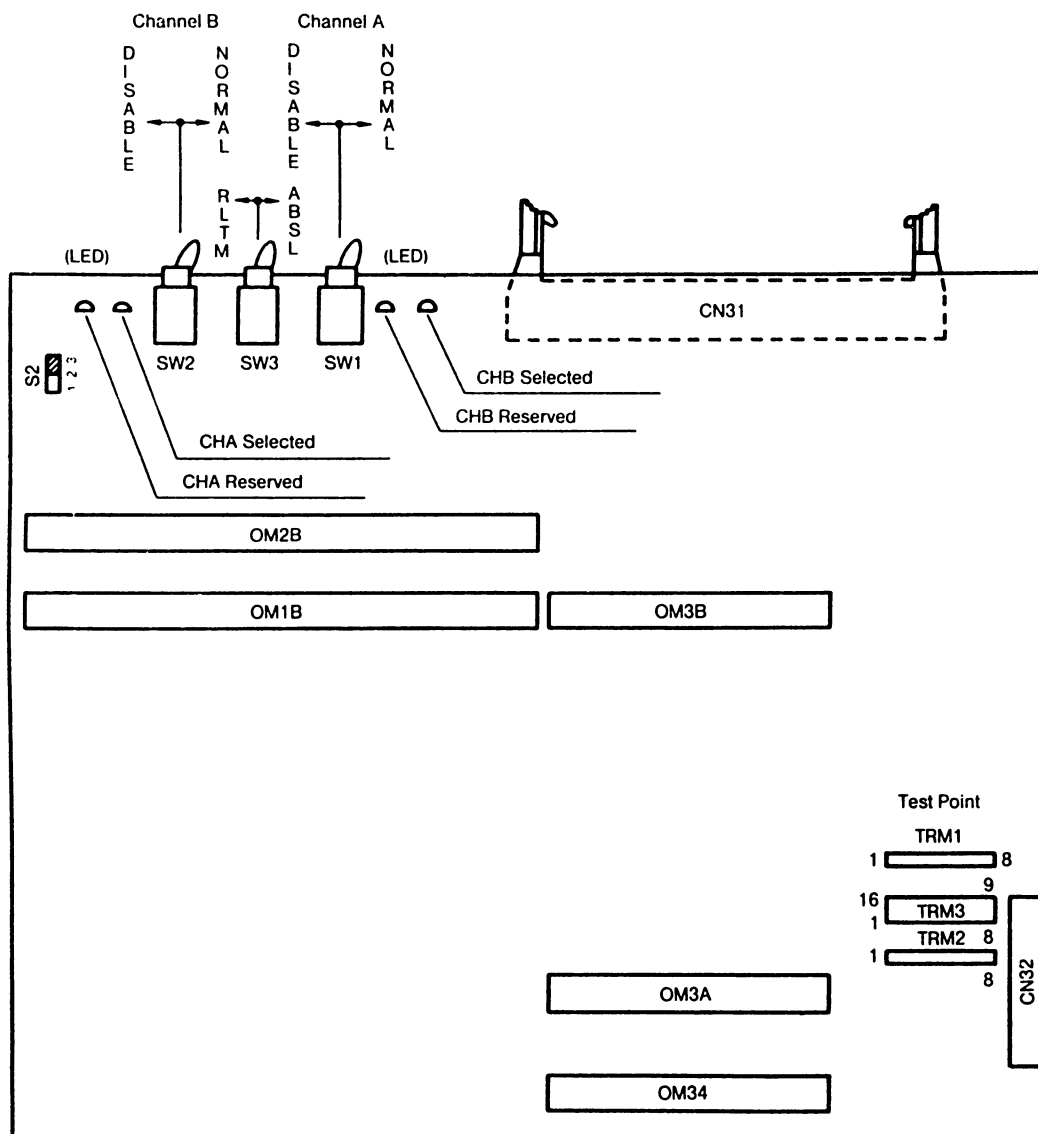


Figure 6.6.6 XCBM Test Points

S2 MODE SELECT

JUMPER	ENABLE MODE	FUNCTION
1-2	MODE A	ANSI
2-3	MODE B	SMD.

Table 6.6.14 XCBM Test Points

TRM	No.	Abbreviation	Signal Name	Schematic code
TRM1	01	CHAENB	Channel A Enable	XC2
	02	DISAK	Disable Channel A Key	XC2
	03	DISBK	Disable Channel B Key	XC2
	04	*RLTMP	Release Timer Pulse	XC2
	05	CHBENB	Channel B Enable	XC2
	06	*CHBSLD	Channel B Selected	XC1
	07	*DISCHA2	Disable Channel A 2	XC1
	08	RLTMK	Release Timer Key	XC2
TRM2	01	CHACMP	Channel A Compare	XB1
	02	*DISCHB2	Disable Channel B 2	XC1
	03	BUSYB	Busy B	XC1
	04	PWRDY	Power Ready	XB1
	05	DISCHB	Disable Channel B	XC2
	06	DISCHA	Disable Channel A	XC3
	07	SKENDA	Seek End A	XC3
	08	0V		
TRM3	01	*INTR	Interrupt (30 μ s)	XC3
	02	SKENDB	Seek End B	XC3
	03	CHBCMP	Channel B Compare	XB1
	04			
	05	-5V		XB1
	06	CHARSV	Channel A Reserved	XC1
	07			
	08	*CHASLD	Channel A Selected	XC1
	09	0V		
	10			
	11			
	12			
	13	CLK1	Clock (200ns)	XB1
	14	BUSYA	Busy A	XC1
	15	*STRSV	Set Reserve (300ns)	XC1
	16	CHBRSV	Channel B Reserved	XC1

6.6.3 PCB Replacement and Adjustment

After PCB or DE replacement, the specified adjustments or settings are required as shown in Table 6.6.15.

Table 6.6.15 PCB Replacement and Adjustment

Item	Replaced Part	Adjustment/Setting
1	Disk Enclosure (DE)	(1) POSN Gain Adjustment (2) Positioning Time Adjustment (Refer to Item 3) (3) Over-shoot Adjustment
2	ROWM PCB Assy	None
3	SDRM PCB Assy	(1) POSN Gain Adjustment (RV5) (2) Positioning Time Adjustment (RV2) (3) Over-shoot Adjustment (RV6)
4	CWWM PCB Assy	None
5	VOIM PCB Assy	(1) Sector Count Selection (SW1 SW2)
6	KGEM PCB Assy	(1) Disk Address (SW1) (2) Optional Device Type (SW2) (3) Sector Mode (SW2) (4) Optional Tag 4 5 Enable (SW2)

Notes: (1) Setting procedures except Device Type on KGEM PCB assembly are described in Section 3 (3.3.5).

(2) The adjustment order on SDRM is from item (1) to item (3).

6.6.3.1 **Optional Device Type**

The customer can select the optional device type on status lines conjunction with optional Tag 4/5 function enabled. The device type of M2298 is specified by keys 1 to 6 of SW2 on KGEM PCB assembly.

Table 6.6.16 Device Type (Optional)

Device Type	Decimal Number	Key 1	Key 2	Key 3	Key 4	Key 5	Key 6
		2 ⁰	2 ¹	2 ²	3 ³	2 ⁴	2 ⁵
M2298	20	OFF	OFF	OFF	OFF	OFF	ON

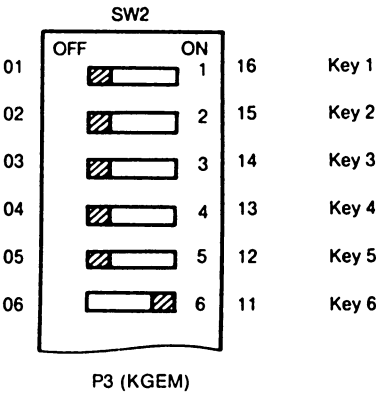


Figure 6.6.7 Device Type

6.6.3.2 **Position Signal N (POSN) Gain Adjustment (SDRM-RV5)**

- (1) Confirm that the unit has normal status.
- (2) Issue RTZ command repeatedly from the control unit.
- (3) Connect the test point TP18 (DRLM) to an oscilloscope and trigger with the positive going edge of the signal (DC coupled).
- (4) Connect the test point TP12 (POSN) to the other channel at the oscilloscope (DC coupled).
- (5) Adjust a potentiometer RV5 so that the signal amplitude is 8V ± 0.2V (peak-to-peak).

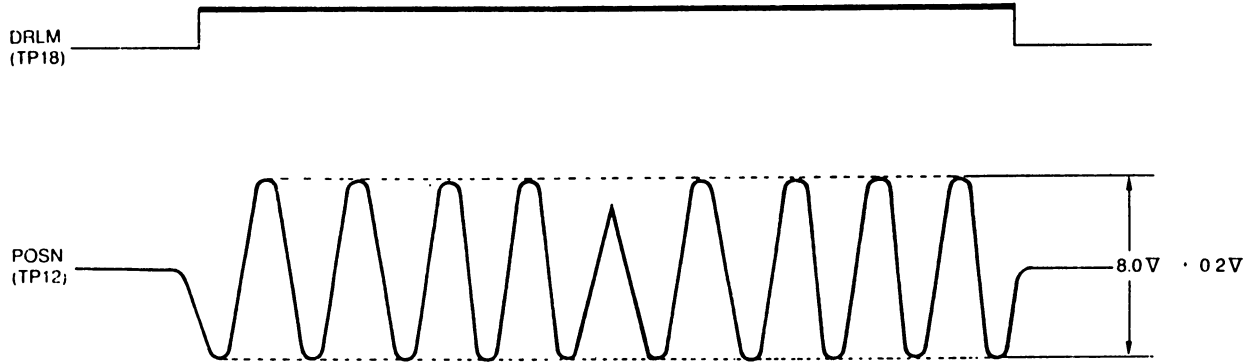


Figure 6.6.8 POSN Gain Adjustment

6.6.3.3 Positioning Time Adjustment (SDRM-RV2)

- (1) Confirm that the unit has normal status.
- (2) Issue the alternate seek command between Cylinder 0 and 512 repeatedly.
- (3) Connect the test point CH7 (POSTM) on CWWM PCB to an oscilloscope and trigger with the positive going edge of the signal.
- (4) Adjust the decelerate time (Tdc) with potentiometer RV2 to the nominal value of $13ms \pm 1ms$ as shown in Figure 6.6.9.

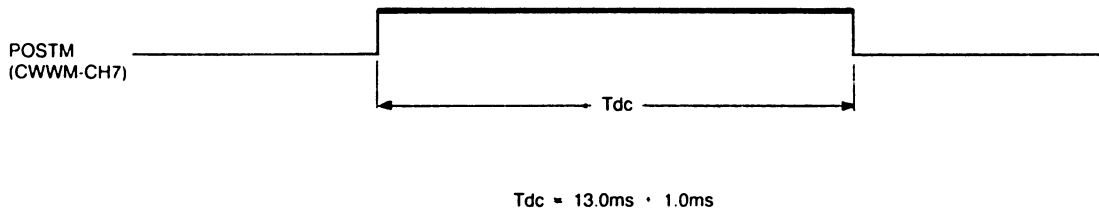


Figure 6.6.9 Positioning Time Adjustment

6.6.3.4 Over-shoot Adjustment (SDRM-RV6)

- (1) Repeat same procedure as 6.6.3.3 item (1) and (2).
- (2) Connect the test point TP34 (PSDR) on CWWM PCB to an oscilloscope and trigger with the positive going edge of the signal.
- (3) Connect the test point TP14 (—FNPOS) on SDRM PCB to the other channel. (DC coupled)
- (4) Adjust the over-shoot voltage (V_{os}) with potentiometer RV6 to nominal value of $0V + 1.0V / - 1.0V$ as shown in Figure 6.6.10.

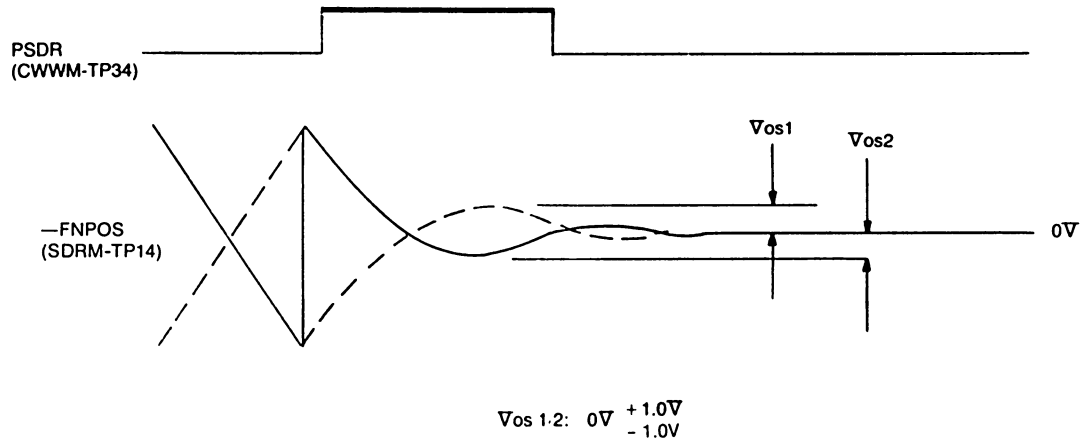


Figure 6.6.10 Over-shoot Adjustment

6.6.4 Electrical Check and Adjustment

The following description is for electrical checks and adjustments when the repair has been performed.

Caution: Do not perform the following adjustments when the PCB is replaced.

6.6.4.1 ROWM PCB Access Head Write Current Adjustment (EA1)

- (1) Confirm that the unit has normal status.
- (2) Connect the test point CH1 (AHWCA) to an oscilloscope and connect the test point CH2 (AHWCB) to the other channel of the oscilloscope with INV mode.
- (3) Issue the seek command to Cylinder 0 and Head 0.
- (4) Issue the write command to proper number of records.
- (5) Add the two channel (differential mode) and adjust the potentiometer RV1 so that the difference is $392\text{mV} \pm 20\text{mV}$.

6.6.4.2 SDRM PCB

- (a) Servo Pulse Window (CA1)
 - (1) Connect the test point TP7 (SVPWD) to a channel of the oscilloscope.
 - (2) Adjust the potentiometer RV3 so that following Tss is $450\text{ns} \pm 10\text{ns}$.

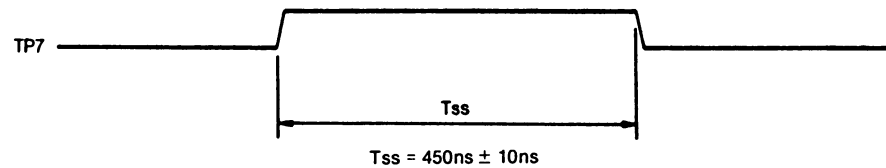


Figure 6.6.11 Servo Pulse Window

- (b) PLOI Free Running Frequency (CA2)
- (1) Turn the power off.
 - (2) Set the switch S1 to the OFF position.
 - (3) Clamp the KGEM-TP17 (GBENB) to 0V.
 - (4) Turn the power on, and wait 40 seconds.
 - (5) Connect the TP5 (PLOVC) to an oscilloscope (DC coupled).
 - (6) Adjust the potentiometer RV1 so that TP5 signal is $+2.5V \pm 0.1V$.
 - (7) Connect the test point TP11 (2 BYTCL) to the Frequency Counter.
 - (8) Select the proper capacitance as shown in Table 6.6.16 so that the frequency of TP11 is closest to 929.5 kHz.
 - (9) Finally adjust the potentiometer RV1 so that the frequency of TP-11 is 929.5 kHz. $\pm 2\%$.

Table 6.6.17 PLOI Adjustment

Plug		Capacitance
S2	S3	
2-3	2-3	30PF
1-2	2-3	45PF
2-3	1-2	37PF
1-2	1-2	52PF

- (c) PLOI Phase (CA1)
- (1) Turn the power off.
 - (2) Set the switch S1 to the OFF position.
 - (3) Turn the power on, and wait 40 seconds.
 - (4) Connect the test point TP9 (PLOSS) to a channel of the oscilloscope.
 - (5) Adjust the potentiometer RV4 so that the following Tss is $2.1 \mu s \pm 0.1 \mu s$.

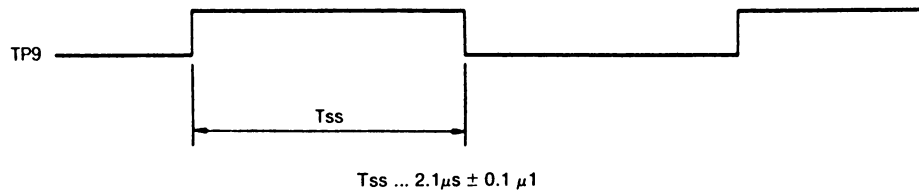


Figure 6.6.12 PLOSS Adjustment

- (d) DAC Output (CB2)
- (1) Confirm that the unit has normal status.
 - (2) Issue the alternate seek command between cylinder 0 and 512 repeatedly.
 - (3) Connect the test point TP23 (—DA) to an oscilloscope and trigger with the negative-going edge of TP23 signal.
 - (4) Adjust the potentiometer RV7 so that VDA is $-5.6V \pm 0.3V$. Refer to Figure 6.6.13.

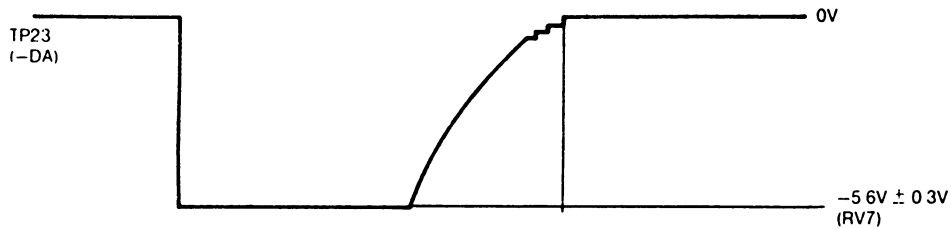


Figure 6.6.13 DAC Output Adjustment

- (e) Fine Velocity (FVEL) Offset Adjustment
 - (1) Locate the head onto Cylinder 0 by issuing RTZ command.
 - (2) Connect the test point CH4 (FVEL) on SDRM PCB to an oscilloscope. (DC coupled)
 - (3) Adjust the potentiometer RV8 so that FVEL signal is $0V \pm 30mV$.

6.6.4.3 CWWM PCB

- (a) Settling Time 1 (BE1)
 - (1) Confirm that the unit has normal status.
 - (2) Connect the check terminal CH2 to an oscilloscope.
 - (3) Issue the alternate seek command between Cylinder 0 and 1 repeatedly.
 - (4) Trigger with the positive-going edge of CH2 signal, and then adjust the potentiometer RV1 so that the pulse width of CH2 signal is $1.5ms \pm 0.1ms$. Refer to Figure 6.6.14.

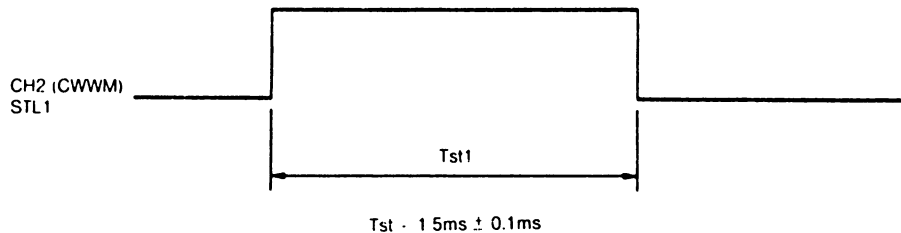


Figure 6.6.14 Settling Time 1 Adjustment

6.6.4.4 VOIM PCB

The adjustment (a) to (d) require a PCB extender.

(a) Reference Pulse Adjustment (RV1)

1. Confirm that unit has a normal status.
2. Connect test point CH2 (REFP) signal to one channel of the oscilloscope (DC coupled).
3. Trigger the oscilloscope with the positive-going edge of the test point signal.
4. Adjust potentiometer RV1 so that the following T_{REF} is $17\text{ns} \pm 0.5\text{ns}$.

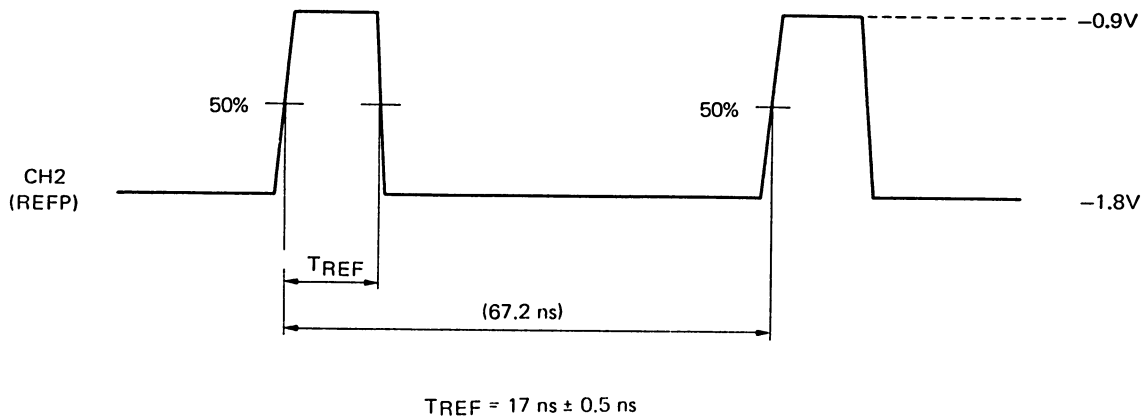


Figure 6.6.15 Reference Pulse Adjustment

(b) VFO Free-run Frequency Adjustment (RV2)

1. Turn the power off.
2. Set S1 (SDRM PCB) to the off position.
3. Clamp Card Pin A22 (VFOLK) on VOIM PCB to 0V firmly.
4. Turn the power on, and wait 60 seconds.
5. Connect the test point CH3 (DTWD) to a frequency counter.
6. Adjust the potentiometer RV2 so that the frequency of CH3 (DTWD) signal is $14.872\text{MHz} \pm 300\text{KHz}$.

(c) Delayed Data One-shot (RV3)

1. Confirm that unit has normal status.
2. Connect test point CH3 (DTWD) on VOIM PCB to one vertical input of an oscilloscope (DC coupled).
3. Connect test point CH1 (DLDT) on VOIM PCB to the other vertical input.
4. Trigger with the positive-going edge of TP (DTWD).
5. Issue a read command to the drive.
6. Adjust the potentiometer RV3 so that the following T is $15\text{ns} \pm 1\text{ns}$.

Caution

Use the same length of probe for measurement of T. Read error caused by measurement error may occur if this precaution is not followed.

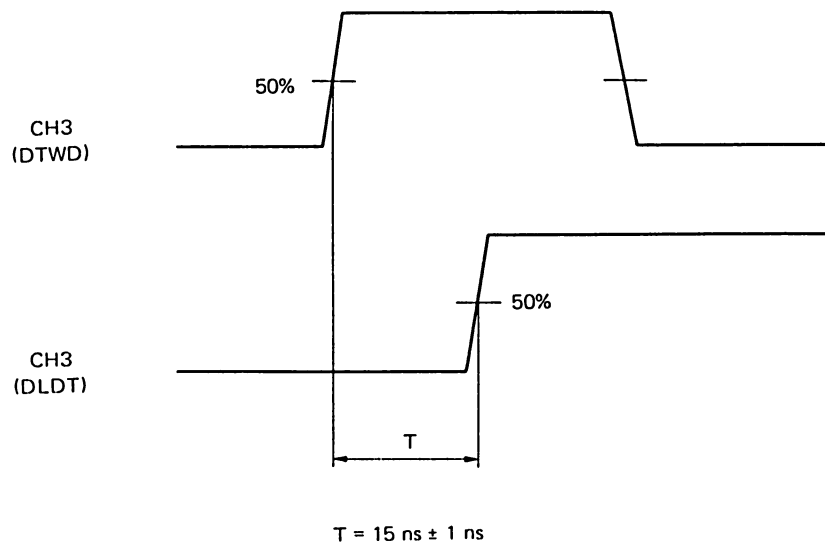


Figure 6.6.16 Delayed Data One-shot Adjustment

6.6.4.5 KGEM

(a) Speed Timer

- (1) Turn the power off.
- (2) Set the switch S1 of SDRM PCB to the OFF position.
- (3) Turn the power on.
- (4) Connect the check terminal CH2 to an oscilloscope (DC coupled).
- (5) Trigger with the positive-going edge of CH2 signal and adjust the potentiometer RV1 so that the positive pulse is $27.5\text{ms} \pm 0.5\text{ms}$.

6.6.5 Electrical Measurement

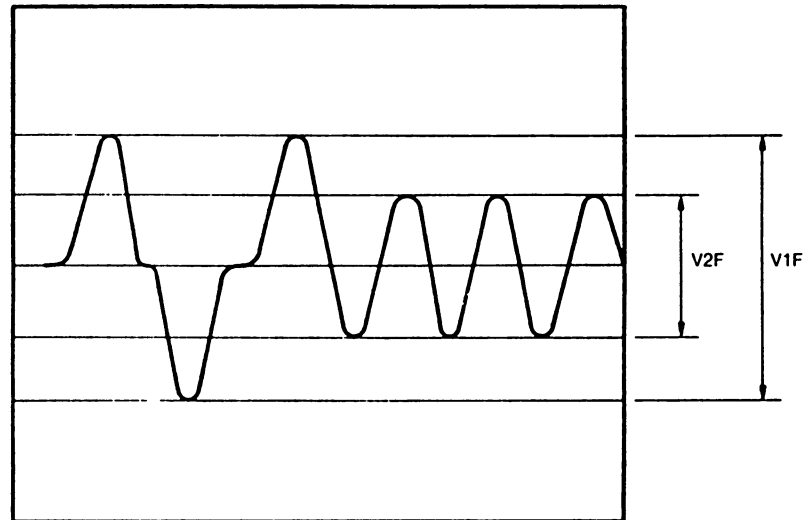
This description will give the maintenance aid to maintenance personnel for electrical measurement.

6.6.5.1 Read Output Measurement

Caution: Use the 0V terminals near the test points TP6 and TP7 on ROWM PCB, and also use the 200MHz wide band oscilloscope. Otherwise some measurement error may occur.

- (1) Write a repetitive "CCCCCCCC B6DB6DB6₁₆" pattern to all records on the desired track.
- (2) Connect the test point TP6 and TP7 on ROWM PCB with the differential mode (inverted channel 2 and add with channel 1).
- (3) After writing, measure the peak-to-peak level of V_{2F} and V_{1F} as shown in Figure 6.6.22.

Note: Measurement may be performed on Cylinder 0 and even Head address.



$$V2F \geq 80\text{mVp-p}$$

$$\text{Resolution Ratio} = \frac{V2F}{V1F} \times 100(\%) \geq 60\%$$

Figure 6.6.17 Read Output Measurement

6.6.5.2 Timing Margin Measurement

The write data pattern may be "CCCCCF6DB4CCCC₁₆". After writing on all records of Cylinder 0 - even Hed address, this measurement should be performed. Caution: Use the 0V terminals near the check terminals CHE1 to 3 for the measurement, also use 200MHz wide band oscilloscope. Otherwise some measurement error may occur.

- (1) Connect the check terminals CHE1 and CHE3 on VOIM PCB. Refer to 6.6.4.4 item (e).
- (2) Adjust CHE1 signal by the potentiometer RV3 to minimum width of critical state that no errors occur for five minutes. $\xrightarrow{\text{TW1}}$
- (3) Similarly, adjust the maximum width as mentioned above. $\xrightarrow{\text{TW2}}$
- (4) Perform the procedures 2 and 3 to all even Head on Cylinder 0 respectively.
- (5) The timing margin will be specified as follows:

$$\text{TTMG} = \text{TW2 (min)} - \text{TW1 (max)} \quad 5\text{ns}$$

- (6) Finally adjust the CHE1 signal as follows:

$$T_{\text{ADJ}} = \frac{\text{TW2 (min)} + \text{TW1 (max)}}{2} \approx 15\text{ns}$$

Refer to Figure 6.6.23.

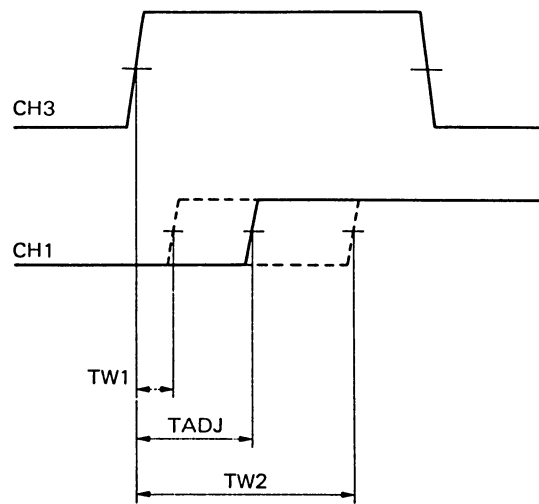


Figure 6.6.18 Timing Margin Measurement

Section 7

Spare Parts List

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7. SPARE PARTS LIST

7.1 SPARE PARTS LIST

Table 7.1 Spare Parts List

Part Designation	Specification	Remarks
Disk Enclosure	B030-4540-T012A	
Spindle Drive Motor	B90L-0980-0002A	AC100V/115V *2
Spindle Drive Motor	B90L-0980-0004A	AC220V/240V *2
Belt	B30L-1000-0108A# L1026	
Anti-static Brush	B030-4420-W006A	*1
Speed Transducer	B030-4420-W030A	*1
Blower	B90L-1190-0001A	*1
Brake Relay	B58L-0170-0001A	*1
VOIM PCB Assembly VFO/PLO	B16B-9820-0010A	
CWWM PCB Assembly Logic	B16B-6150-0010A	
KGEM PCB Assembly INT	B16B-6160-0060A	*2
SDRM PCB Assembly Servo	B16B-8990-0060A	
ROWM PCB Assembly R/W	B16B-9000-0060A	

- Notes:
- (1) The spare parts marked by “*1” are commonly used with M228X and M2294 Disk Drive.
 - (2) The spare parts marked by “*2” are commonly used with M2294 Disk Drive.
 - (3) The spare parts without “*” are exclusively used for M2298 Disk Drive.

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Section 8

IC Details

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8. IC DETAILS

8.1 INTRODUCTION

This section describes functions of TTL, ECL, Linear and FUJITSU Analog Master Slice IC's.

8.2 LOGIC CONVENTIONS AND SYMBOLOGY

8.2.1 TTL Logic

M2298 Fixed Disk Unit uses +5V Transistor-Transistor-Logic. TTL logic is defined in terms of standard POSITIVE LOGIC using the following definitions:

High Voltage = Logical "1"

Low Voltage = Logical "0"

The input/output logic of TTL are defined as follows:

(A) TTL Medium Speed IC

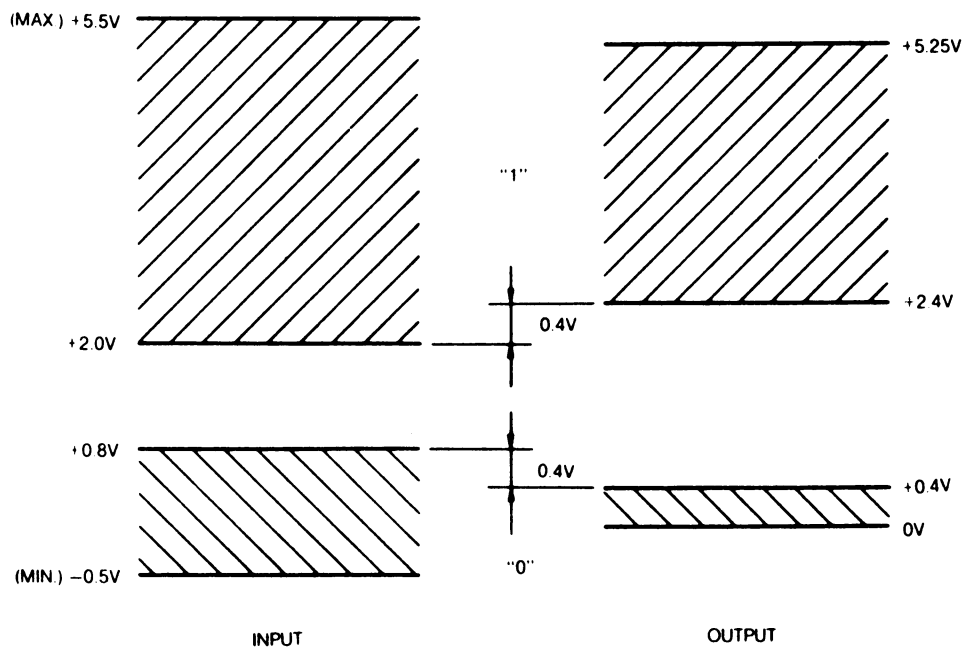


Figure 8.2.1 TTL Medium Speed IC Level

(B) TTL Super High Speed IC Level

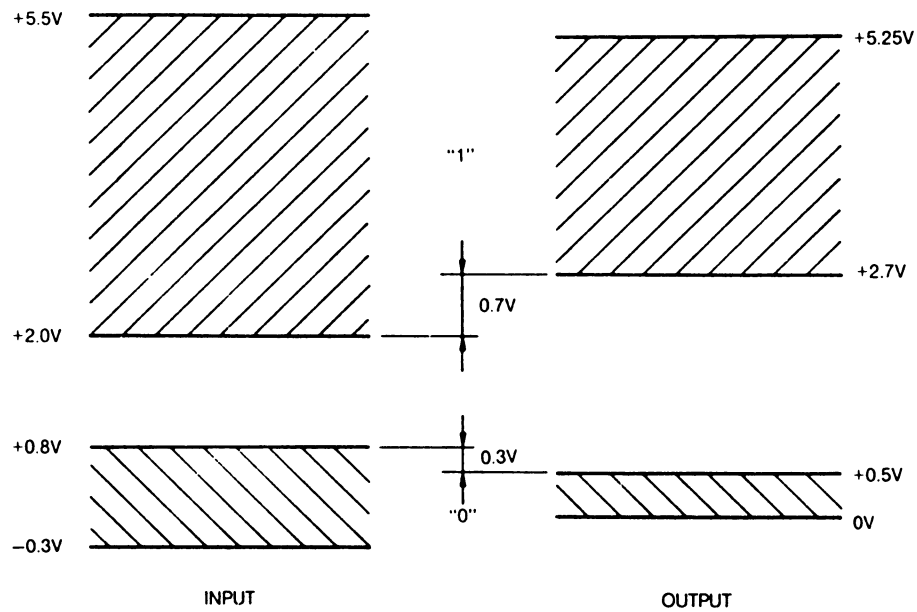


Figure 8.2.2 TTL Super High Speed IC Level

(C) TTL Medium Speed Low Power Consumption IC

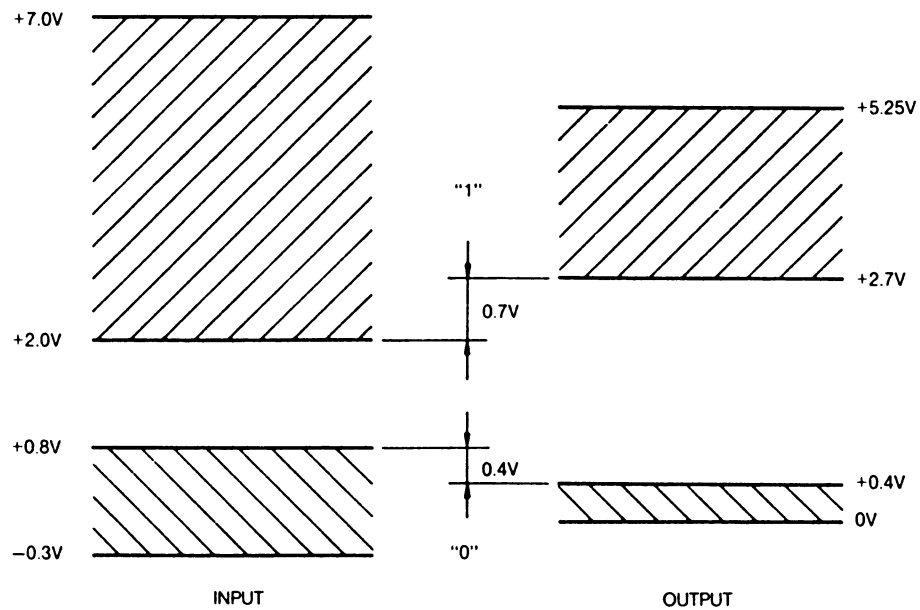


Figure 8.2.3 TTL Medium Speed Low Power Consumption IC Level

8.2.2 ECL Logic

M2298 Fixed Disk Unit uses -5.2V ECL (Emitter-Coupled-Logic). The high impedance of the logic (input to differential amplifier) coupled with the low impedance of the driving source (emitter-follower output) allows high DC fan-out.

High-speed operation and high AC fan-out are possible because all circuits are designed to operate in a 50 ohms system. Complementary outputs cause a function and its complement to appear simultaneously at the device output, without the use of external inverters. In M2298 each output is terminated to resistors. ECL logic is defined in terms of standard POSITIVE LOGIC using the following definitions:

High Voltage = Logical "1"

Low Voltage = Logical "0"

The input/output logic levels of ECL are defined as follows:

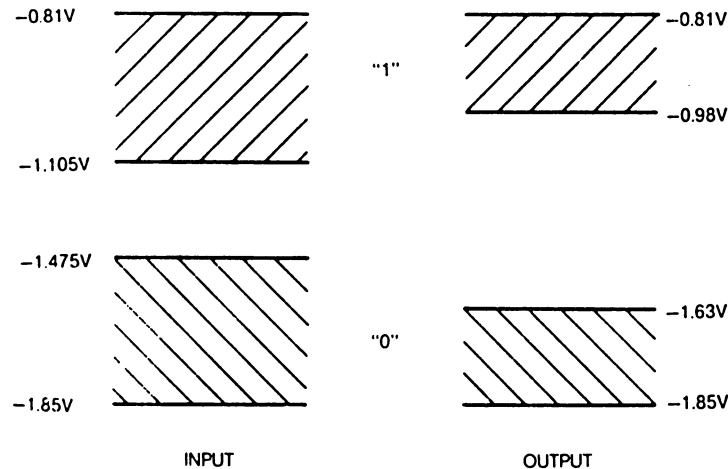
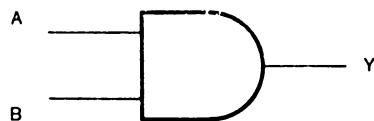


Figure 8.2.4 ECL Logic Level

8.2.3 Logic Symbology

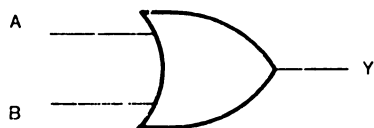
The following conventions are provided to aid in understanding the symbology used in this manual.

(1) TTL



This indicates AND gate.

$$Y = A \cdot B$$



This indicates OR gate.

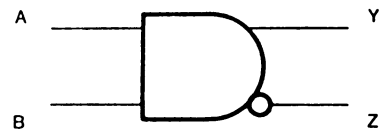
$$Y = A + B$$

A circle placed on any input line or on the output line indicates that logical "0" is the significant state.

The absence of a circle, "1" is the significant state.

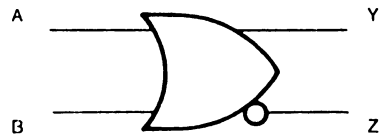
O

(2) ECL



This indicates AND/NAND gate.

$$Y = A \cdot B = \bar{Z}$$



This indicates OR/NOR gate.

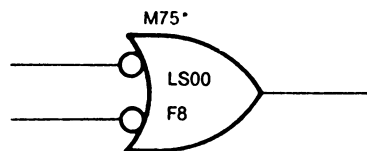
$$Y = A + B = \bar{Z}$$

This symbol has the same meaning as in TTL.

○

(3) All logic symbols on each logic diagram are identified by a sequential numbering and element type code.

For example:



M75*: Sequential part number of each parts list.

LS00: Abbreviation (marking) of the element code.

F8: Physical location of element on P.C.B assembly.

8.3 IC INTERCHANGEABILITY GUIDE

8.3.1 TTL IC Interchangeability

Table 8.3.1 TTL Interchangeability

FUJITSU		Direct	Functions
Type No.	Marking	Replacement	
MB400M	LA01	SN7400N	Quad 2-input NAND
MB418M	LA18	SN7404N	Hex Inverter
MB433M	433	SN7438N	Quad 2-input NAND Buffer
MB434M	434	SN75451P	Dual 2-input OR Buffer
MB435M	435	SN7437N	Quad 2-input NAND Buffer
MB436M	436	SN75453P	Dual 2-input OR Buffer

Table 8.3.1 TTL Interchangeability (Continued)

FUJITSU		Direct	Functions
Type No.	Marking	Replacement	
None	LX16	SN75452P	Dual 2-input NAND Buffer
None	LS18	SN7408N	Quad 2-input AND
None	LX20	SN7414N	Hex Schmitt-Trigger Inverter
None	LX27	SN74221N	Dual Monostable
None	LX32	SN7406N	Hex Inverter with Open Collector
None	LX33	SN7407N	Hex Buffer with Open Collector
MB74S00M	S00 (LH01)	SN74S00N	Quad 2-input NAND
MB74S04M	S04 (LH04)	SN74S04N	Hex Inverter
MB74S08M	S08	SN74S08N	Quadruple 2-input AND Gates
MB74S10M	S10 (LH02)	SN74S10N	Triple 3-input NAND
MB74S11M	S11 (LH08)	SN74S11N	Triple 3-input AND Gate
None	S133 (LH07)	SN74S133N	13-input NAND
None	S112 (LH10)	SN74S112N	Dual J-K Flip-Flop
None	S124 (LH24)	SN74S124N	Dual VCO
MB74S37M	S37	SN74S37N	Quadruple 2-input NAND Buffer
MB74S51M	S51 (LH06)	SN74S51N	Dual AND-OR-NOT
None	S64	SN74S64N	4-2-3-2 input AND-OR-Invert Gates
None	S74	SN74S74N	Dual D-Type Flip-Flop
MB74S174M	S174 (LH28)	SN74S174N	Flex D-Type Flip-Flop
MB74LS00M	LS00	SN74LS00N	Quad 2-input NAND
MB74LS02M	LS02	SN74LS02N	Quad 2-input NOR
MB74LS04M	LS04	SN74LS04N	Hex Inverter
MB74LS08M	LS08	SN74LS08N	Quad 2-input AND
MB74LS10M	LS10	SN74LS10N	Trip 3-input NAND
MB74LS11M	LS11	SN74LS11N	Trip 3-input AND
MB74LS20M	LS20	SN74LS20N	Dual 4-input NAND
MB74LS30M	LS30	SN74LS30N	8-input NAND
MB74LS32M	LS32	SN74LS32N	Quad 2-input OR
MB74LS37M	LS37	SN74LS37N	Quad 2-input NAND Buffer
MB74LS32M	LS42	SN74LS42N	BCD to Decimal Decoder
MB74LS51M	LS51	SN74LS51N	Dual 2-wide 2-input ND-OR-INV
MB74LS74M	LS74	SN74LS74N	Dual D-Type Flip-Flop
MB74LS85M	LS85	SN74LS85N	4-Bit Magnitude Comparator
MB74LS86M	LS86	SN74LS85N	Quad 2-input EOR
MB74LS107M	LS107	SN74LS107N	Dual J-K Flip-Flop
None	LS123	SN74LS123N	Dual Retriggerable Monstable
MB74LS139M	LS139	SN74LS139N	Dual 2 to 4 Decoder
MB74LS153M	LS153	SN74LS153N	Dual 4-to-1 Data Selector/Multiplexer
MB84LS161M	LS161	SN74LS161N	4-bit Binary counter
MB74LS164M	LS164	SN74LS164N	8-bit Shift Register
MB74LS174M	LS174	SN74LS174N	Hex D-Type Flip-Flop

Table 8.3.1 TTL Interchangeability (Continued)

FUJITSU		Direct	Functions
Type No.	Marking	Replacement	
MB74LS175M	LS175	SN74LS175N	Quad D-Type Flip-Flop
MB74LS191M	LS191	SN74LS191N	4-bit Up/Down Counter
None	LS221	SN74LS221N	Dual Monostable
None	LS279	SN74LS279N	Quad S-R Latch
MB74LS283M	LS283	SN74LS283N	4-bit Full Adder Fast Carry
MB14601C	14601	None	Linear Motor Control

Note: Direct replacement is a device of Texas Instruments Inc.

8.3.2 ECL IC Interchangeability

Table 8.3.2 ECL Interchangeability

FUJITSU	Direct	Functions
Type No.	Replacement	
MB10101C	MC10101L	Quadruple OR/NOR Gates
MB10102C	MC10102L	Quad 2-input NOR
MB10105C	MC10105L	Triple 2-3-2-input OR/NOR Gates
MB10106C	MC10106L	Triple 4-3-3 NOR
MB10109C	MC10109L	Dual 4-5 OR/NOR
MB10115C	MC10115L	Quad Line Receiver
MB10116C	MC10116L	Triple Line Receiver
MB10124C	MC10124L	Quad TTL to ECL Translator
MB10125C	MC10125L	Quad ECL to TTL Translator
MB10131C	MC10131L	Dual D Flip-Flop
MB10174C	MC10174L	Dual 4-to-1 Multiplexers

8.3.3 Linear IC Interchangeability

Table 8.3.3 Linear IC Interchangeability

FUJITSU		Direct Replacement		Functions
Type No.	Marking	1st	2nd	
MB3607M	A1458	MC1458 (MOTOROLA)		Operational Amplifier
MB4002M	A4002			Voltage Comparator
	A610	μ PC610D (NEC)	DAC02 (PM)	10-bit D/A Converter
	A311	μ PC271C (NEC)	LM311 (NS)	Voltage Comparator
	A1590	MC1590G (MOTOROLA)		AGC Amplifier
	A201	DG201BK (SILICO)		Quad Analog Switch
	A7905	μ PC16305H (NEC)		–5V Regulator
	3450	MC3450L (MOTOROLA)		Quad Line Receiver
	75107A	SN75107AN (TI)		Dual Line Receiver
	75108A	SN75107AN (TI)		Dual Line Receiver (O.C.)
	75110	SN75110AN (TI)		Dual Line Driver
	3107	HD103107 (HITACHI)		ECL Voltage Controlled Oscillator
	A7952	μ PC16352H (NEC)		7952-Type –5.2V Regulator

- Notes:
- (1) NEC is Nippon Electric Co., Ltd.
 - (2) MOTOROLA is MOTOROLA Semiconductor Product Inc.
 - (3) NS is National Semiconductor Corp.
 - (4) PM is Precision Monolithics Incorporated.
 - (5) SILICO is Siliconix Incorporated.
 - (6) TI is Texas Instruments Inc.

8.3.4 FUJITSU Analog Master Slice IC

Table 8.3.4 FUJITSU Analog M/S IC

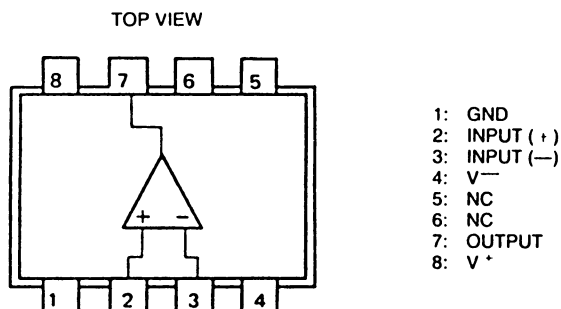
FUJITSU		Direct Replacement	Functions
Type No.	Marking		
MB4303C	A4304	None	AGC Amplifier
MB4311C	A4311	None	Peak Detector
MB4316C	A4316	None	R/W Bus Switch
MB4319C	A4319	None	Peak Hold
MB4320C	A4320	None	Pulse Shaper

Note: They are all original IC's made by FUJITSU.

8.4 FUJITSU PROPRIETARY IC DETAIL

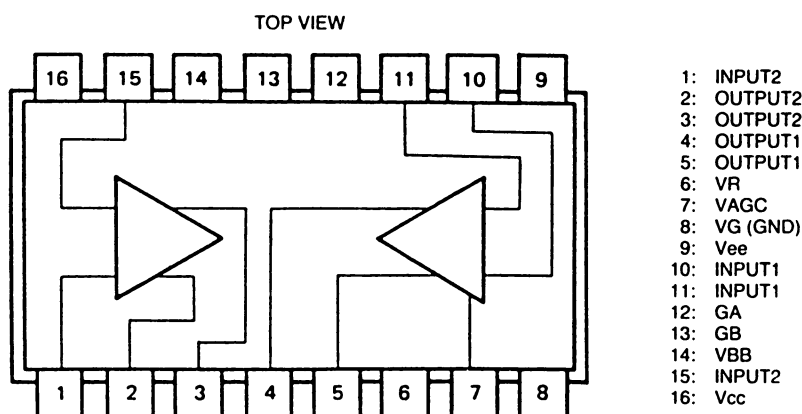
(1) MB4002M High Speed Differential Comparator

The MB4002M is a Differential Voltage Comparator intended for applications requiring high accuracy and fast response times. The device is useful as a variable threshold Schmitt trigger, a pulse height discriminator, a voltage comparator in high-speed A/D converters, a memory sense amplifier or a high-noise immunity line receiver. The output of the comparator is compatible with all integrated logic forms.

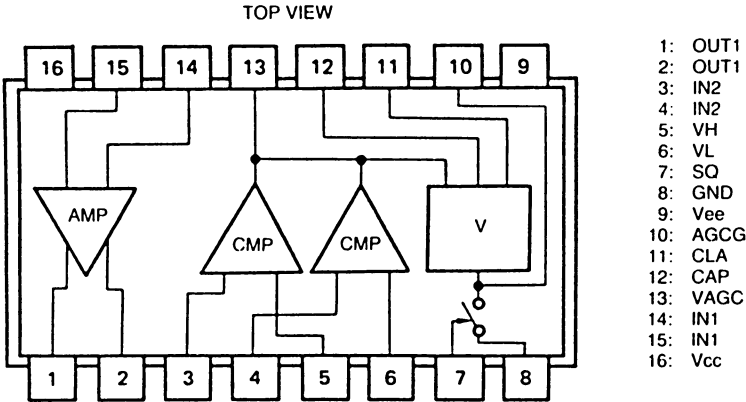


(2) MB4303C AGC Amplifier

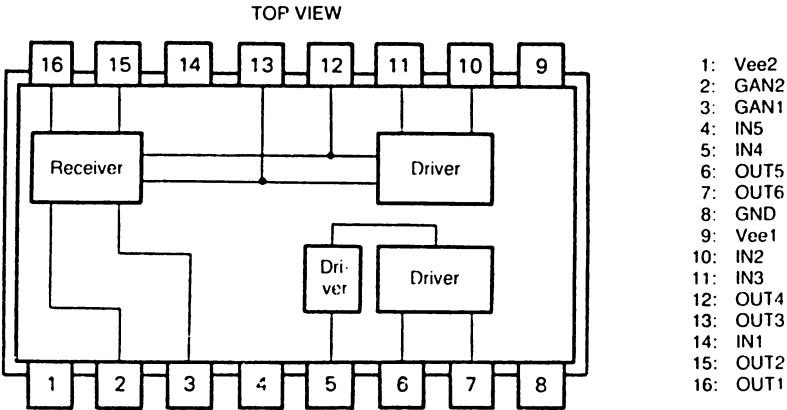
The MB4303C is an Automatic-Gain-Control Amplifier with Differential Inputs and Outputs. It contains another Differential Amplifier.



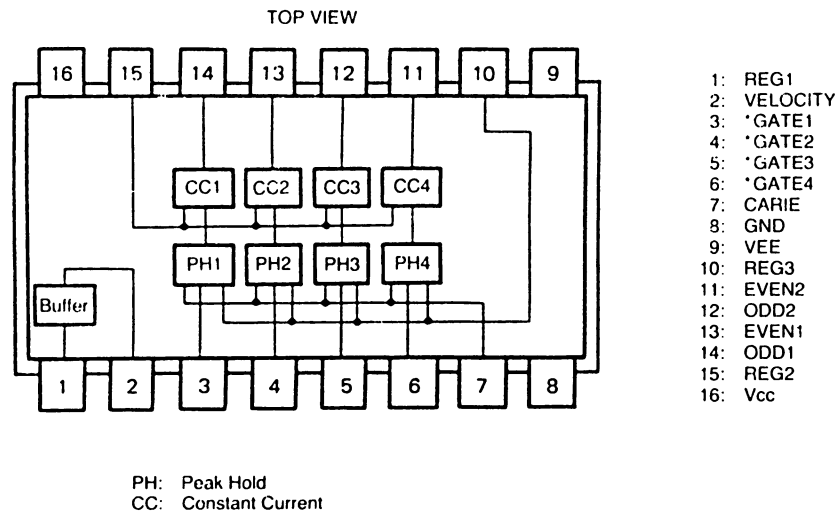
(3) MB4311C
Peak Detector



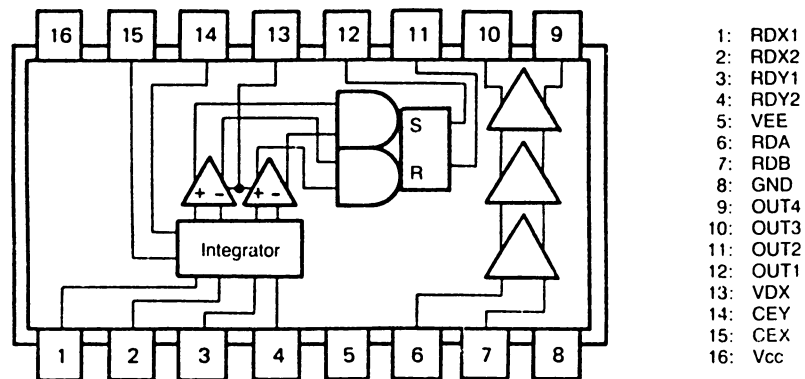
(4) MB4316C
Read/Write Bus Switch



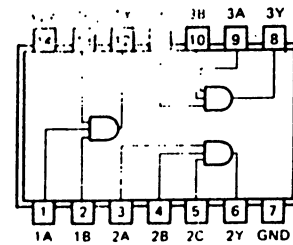
(5) MB4319C
Peak Hold



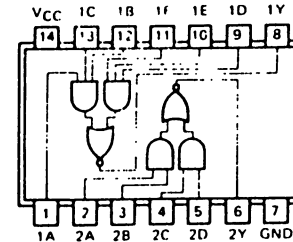
(6) MB4320C
Pulse Shaper



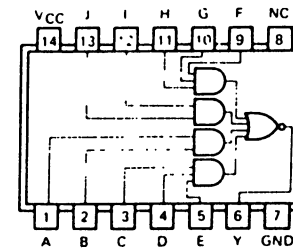
- (7) MB74LS11M (SN74LS11)
Triple 3-Input
Positive AND Gates
 $Y = A \cdot B \cdot C$



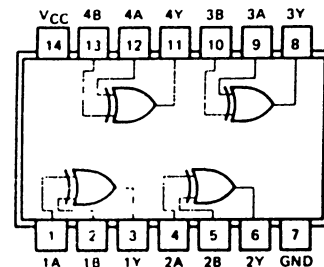
- (8) MB74LS51M (SN74LS51N)
Dual 2-Wide 2-Input
AND-OR-INVERT Gates
Positive Logic
 $1Y = \overline{(1A \cdot 1B \cdot 1C) + (1D \cdot 1E \cdot 1F)}$
 $2Y = \overline{(2A \cdot 2B) + (2C \cdot 2D)}$



- (9) MB74LS54M (SN74LS54N)
4-Wide
AND-OR-INVERT Gates
Positive Logic
 $Y = \overline{(A \cdot B) + (C \cdot D \cdot E) + (F \cdot G \cdot H) + (I \cdot J)}$



- (10) MB74LS86M (SN74LS86N)
Quadruple 2-Input
Exclusive OR Gates
Positive Logic
 $Y = A \oplus B = AB + \overline{A}\overline{B}$



(11) MB74LS279M (SN74LS279N)
Quadruple S-R Latches

FUNCTION TABLE

INPUTS		OUTPUT
$\bar{S}+$	\bar{R}	Q
H	H	Q_0
L	H	H
H	L	L
L	L	H^*

H = high level

L = low level

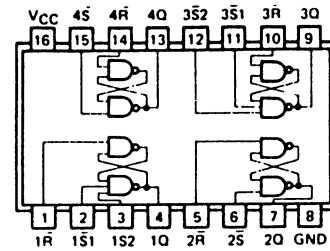
Q_0 = the level of Q before the indicated input conditions were established.

*This output level is pseudo stable; that is, it may not persist when the \bar{S} and \bar{R} inputs return to their inactive (high) level.

+ For latches with double \bar{S} inputs:

H = both \bar{S} inputs high

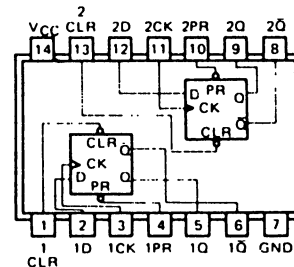
L = one or both \bar{S} inputs low



(12) MB420M (SM7474N)
MB74LS74M (SN74LS74N)
Dual D Type Positive Edge Triggered Flip-Flop
with Preset and Clear

FUNCTION TABLE

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	\bar{Q}
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H^*	H^*
H	H	\uparrow	H	H	L
H	H	\downarrow	L	L	H
H	H	L	X	Q_0	\bar{Q}_0



H = high level (steady state), L = low level (steady state), X = irrelevant

\square = high-level pulse; data inputs should be held constant while clock is high; data is transferred to output on the falling edge of the pulse.

\uparrow = transition from low to high level, \downarrow = transition from high to low level

Q_0 = the level of Q before the indicated input conditions were established.

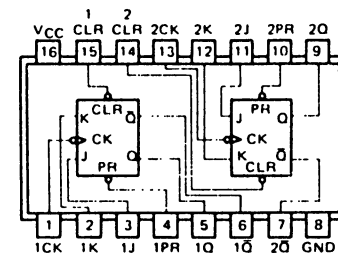
TOGGLE: Each output changes to the complement of its previous level on each active transition (pulse) of the clock.

*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

(13) SN74S112N
Dual J-K Negative Edge Triggered Flip-Flop
with Preset and Clear

FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	\bar{Q}
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H^*	H^*
H	H	\downarrow	L	L	Q_0	\bar{Q}_0
H	H	\downarrow	H	L	H	L
H	H	\downarrow	H	H	TOGGLE	TOGGLE
H	H	H	X	X	Q_0	\bar{Q}_0



H = high level (steady state), L = low level (steady state), X = irrelevant

\downarrow = transition from high to low level





Q_0 = the level of Q before the indicated input conditions were established.

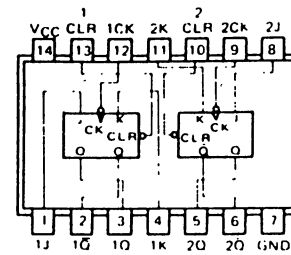
TOGGLE: Each output changes to the complement of its previous level on each active transition of the clock.

*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.


(14) MB74LS107M (SN74LS107N)
Dual J-k Master Slave Flip-Flop with clear


FUNCTION TABLE

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	\bar{Q}
L	X	X	X	L	H
H		L	L	Q_0	\bar{Q}_0
H		H	L	H	L
H		L	H	L	H
H		H	H	TOGGLE	TOGGLE



H = high level (steady state), L = low level (steady state), X = irrelevant

 : transition from high to low level

 : high-level pulse; data inputs should be held constant while clock is high; data is transferred to output on the falling edge of the pulse.










Q_0 : the level of Q before the indicated input conditions were established.

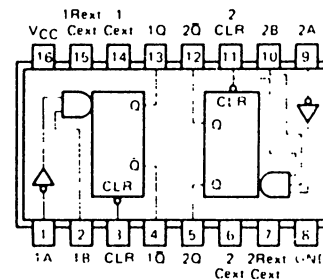
TOGGLE: Each output changes to the complement of its previous level on each active transition (pulse) of the clock.

*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

(15) MB440M (SN74123N)
Dual Retriggerable Monostable Multivibrator with Clear

FUNCTION TABLE

INPUTS			OUTPUTS	
CLEAR	A	B	Q	\bar{Q}
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L			
H		H		
	L	H		



This monolithic TTL retriggerable monostable multivibrator features d-c triggering from gated low-level-active (A) and high-level-active (B) inputs, and also provides overriding direct clear inputs. The retrigger capability simplifies the generation of output pulses of extremely long duration. By triggering the input before the output pulse terminated, the output pulses may be extended. The overriding clear capability permits any output pulse to be terminated at a predetermined time independently of the timing components R and C. The output pulse is primarily a function of the external capacitor and resistor.

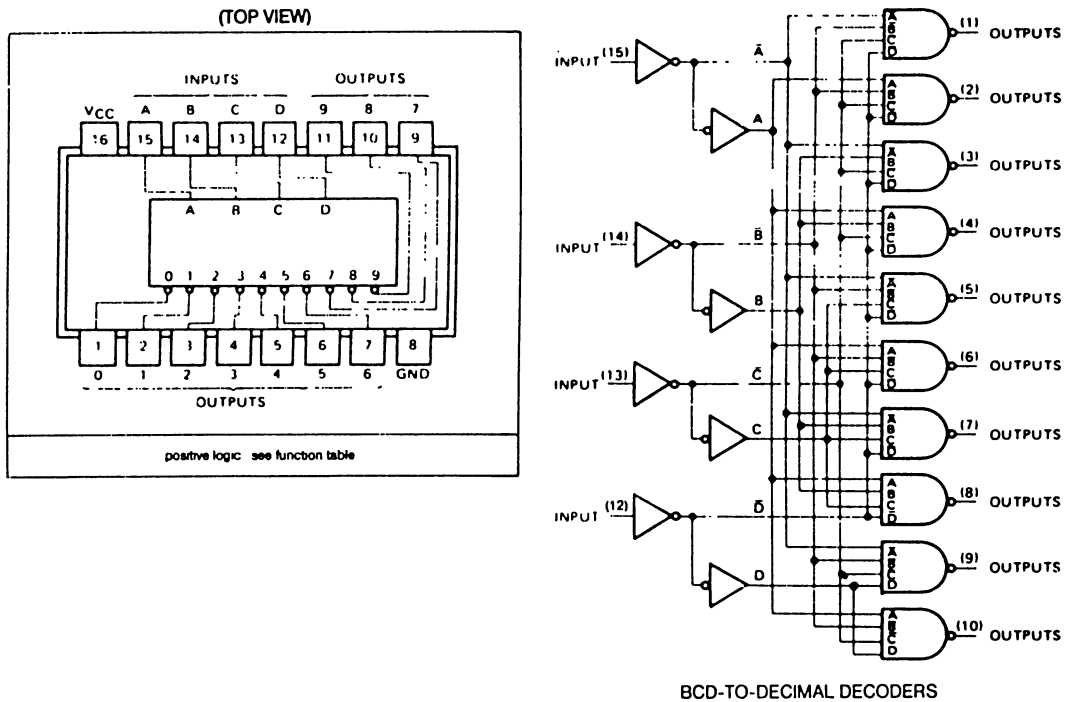
For $C_{ext} > 1000\text{pF}$, the output pulse width (t_w) is defined as:

$$t_w = 0.32R_tC_{ext} \left(1 + \frac{0.7}{R_t}\right)$$

t_w : ns
 R_t : kohms
 C_{ext} : pF

(16) MB442M (SN7442N)
BCD-to-Decimal Decoder

These monolithic decimal decoders consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all outputs remain off for all invalid input conditions.



FUNCTION TABLE

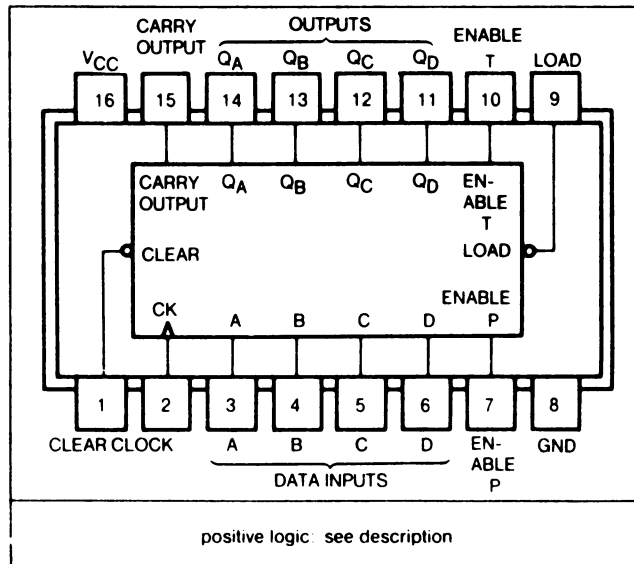
No.	BCD INPUTS				DECIMAL OUTPUT									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = high level, L = low level

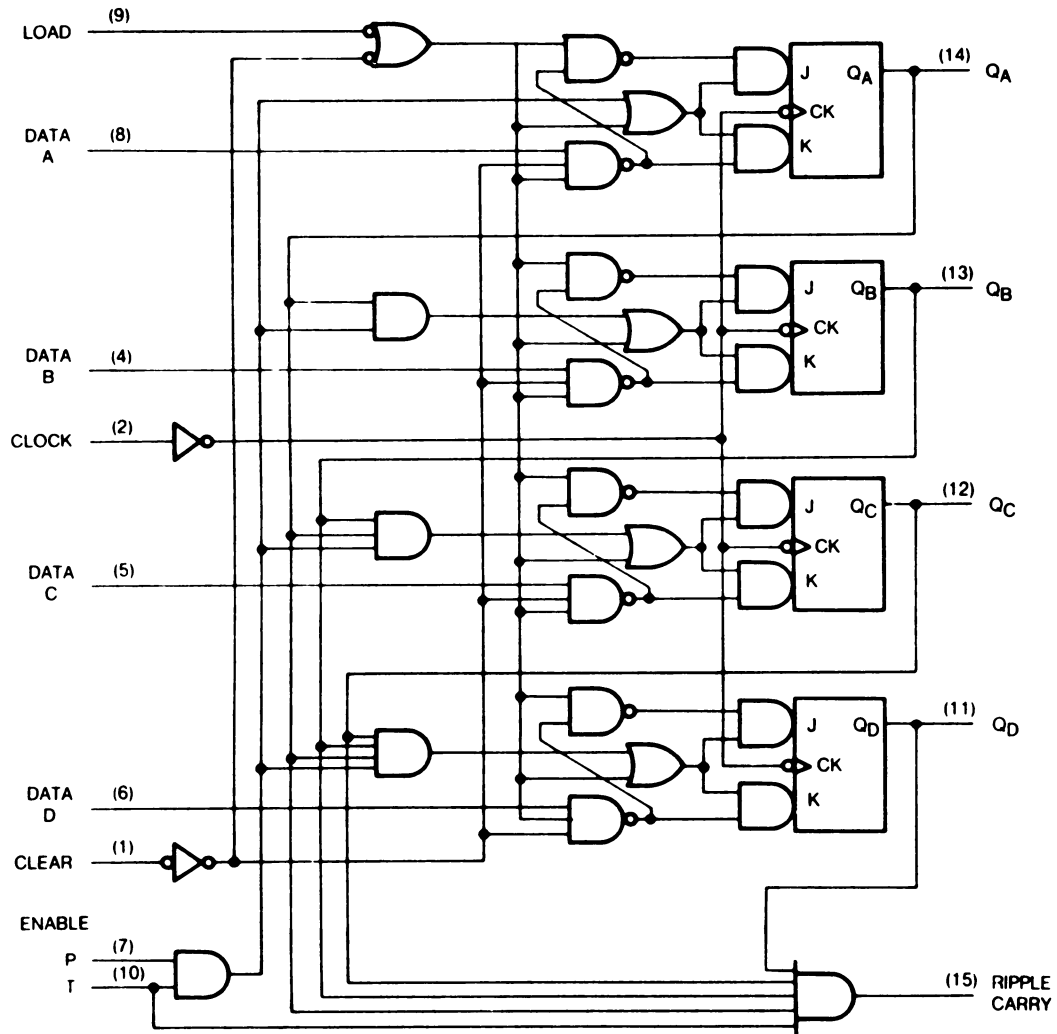
(17) MB450M (SN74161N), SN74LS161N
Synchronous 4-bit Counter with Direct Clear

This synchronous, presettable counter features an internal carry look-ahead for application in high-speed counting schemes. Synchronous operation is provided by having all flip-flop clocked simultaneously so that the outputs change coincident with each other when so instructed by the countenable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four J-K masterslave flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. Low-to-high transitions at the load input should be avoided when the clock is low if the enable inputs are high at or before the transition. The clear function for the SN74161N is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of the clock, load, or enable inputs. This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to 0000 (LLLL).

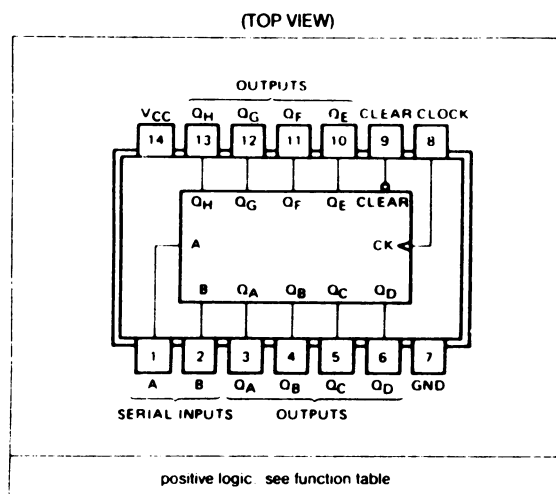


Functional block diagrams



(18) SN74164N, MB74LS164M (SN74LS164N)
8-Bit Parallel-Out Serial Shift Registers

These 8-bit shift registers feature gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data as a low at either (or both) inputs(s) inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high, but only information meeting the setup requirements will be entered. Clocking occurs on the low-to-high-level transition of the clock input. All inputs are diode-clamped to minimize transmission-line effects.



FUNCTION TABLE

INPUTS				OUTPUTS			
CLEAR	CLOCK	A	B	Q _A	Q _B ...	Q _H	
L	X	X	X	L	L	L	
H	L	X	X	Q _{A0}	Q _{B0}	Q _{H0}	
H	↑	H	H	H	Q _{An}	Q _{Gn}	
H	↑	L	X	L	Q _{An}	Q _{Gn}	
H	↑	X	L	L	Q _{An}	Q _{Gn}	

H = high level (steady state), L = low level (steady state)

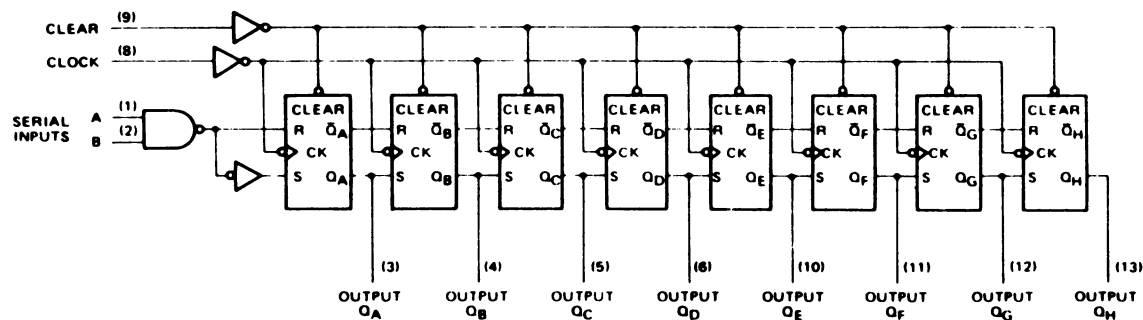
X = irrelevant (any input, including transitions)

↑ = transition from low to high level

Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.

Q_{An}, Q_{Gn} = the level of Q_A or Q_G before the most-recent transition of the clock; indicates a one-bit shift.

Functional block diagram



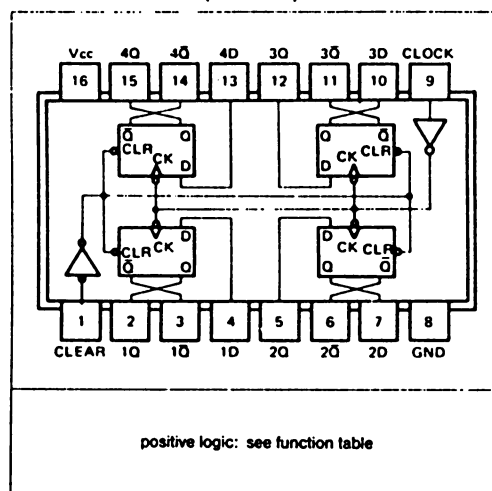
◆ . . . dynamic input activated by transition from a high level to low level

- (19) SN74175N
 MB74LS175M (SN74LS175N)
 Quadruple D-Type Flip-Flop
 MB74LS174M (SN74LS174N)
 Hex D-Type Flip-Flop

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input, and the '175, 'LS175, and feature complementary outputs from each flip-flop.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

'175, 'LS175
(TOP VIEW)

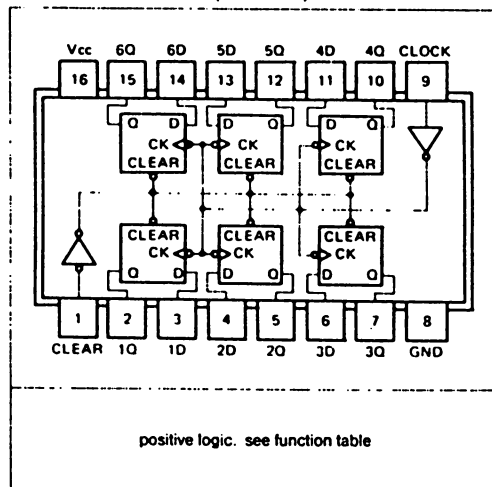


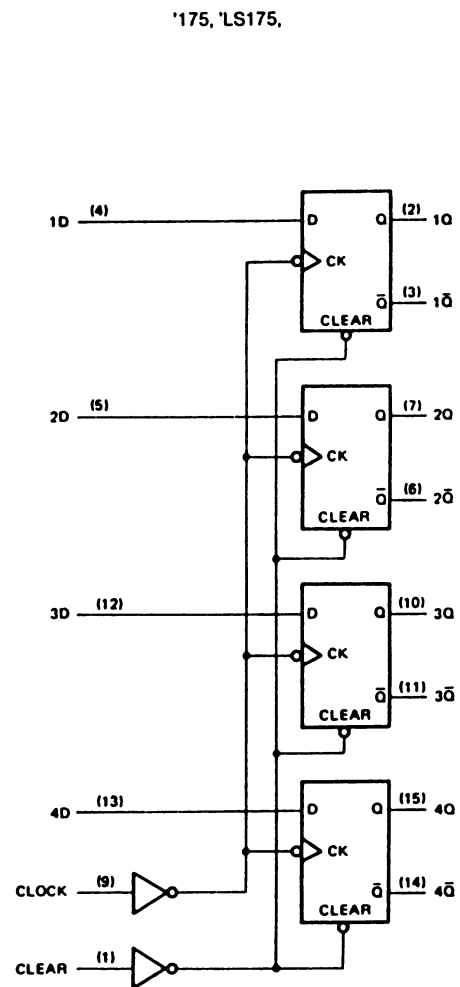
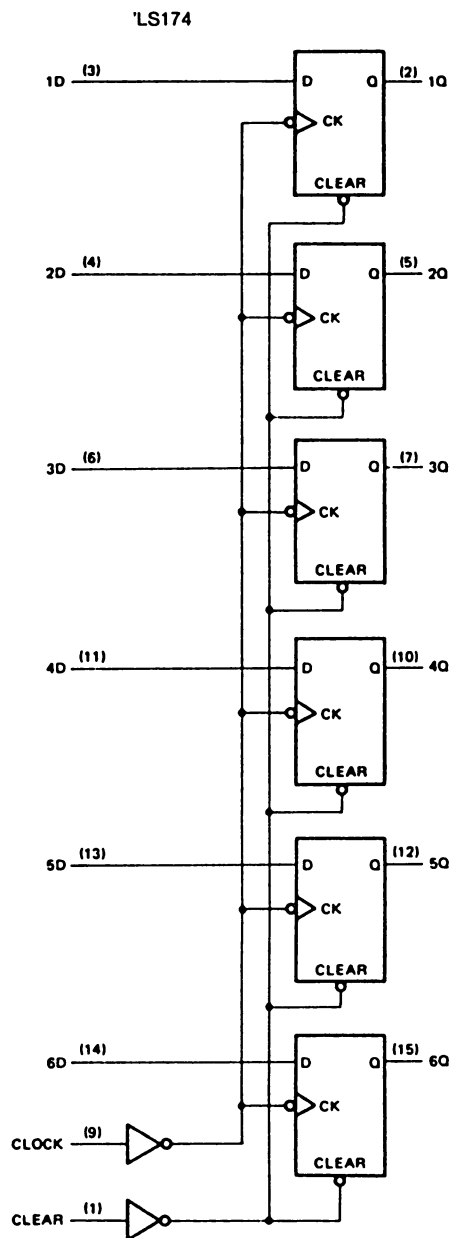
FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	Q ⁺
L	X	X	L	H
H	+	H	H	L
H	+	L	L	H
H	L	X	Q ₀	Q ₀

H = high level (steady state)
 L = low level (steady state)
 X = irrelevant
 + = transition from low to high level
 Q₀ = the level of Q before the indicated steady-state input conditions were established.
 + = '175, 'LS175, only

'LS174
(TOP VIEW)



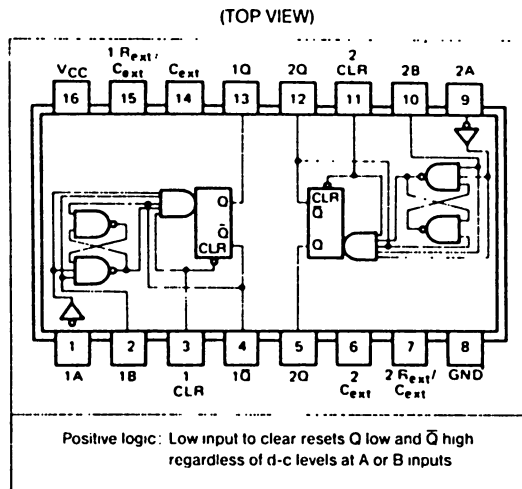


... dynamic input activated by transition from a high level to a low level

(20) SN74221N
Dual Monostable Multivibrator
with Schmitt-Trigger Input

The SN74221N are monolithic dual multivibrators with performance characteristics virtually identical to those of the SN74121N. Each multivibrator features a negative-transition-triggered input and a positive-transition-triggered input either of which can be used as an inhibit input.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry (TTL hysteresis) for B input allows jitter-free triggering from inputs with transition rates as slow as 1 volt/second, providing the circuit with excellent noise immunity of typically 1.2 volts. A high immunity to V_{CC} noise of typically 1.5 volts is also provided by internal latching circuitry.



FUNCTION TABLE
(EACH MONOSTABLE)

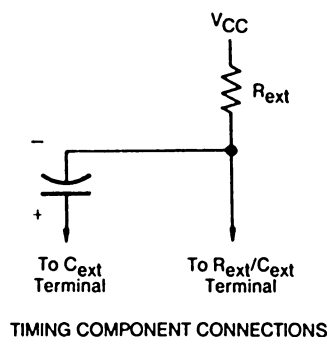
INPUTS			OUTPUTS	
CLEAR	A	B	Q	\bar{Q}
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	0		
H		H		
	L	H		

Also see description and switching characteristics

The output pulse width (tw) is defined as:

$$t_w = 0.7R_{ext}C_{ext}$$

tw; ns, rext: kohms, Cext: pf



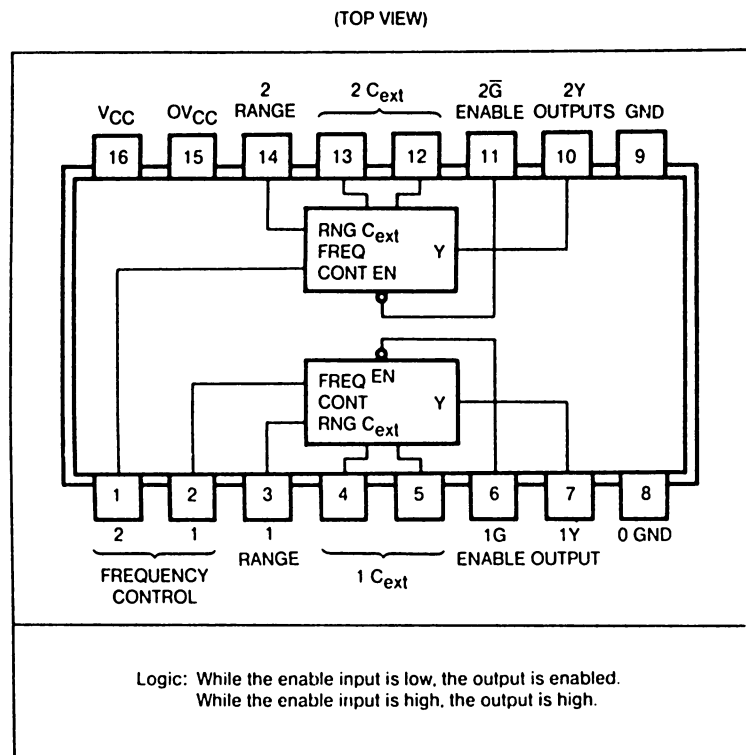
(21) SN74S124N
Dual Voltage Controlled Oscillators

The 'S124 feature two independent voltage-controlled oscillators (VCO) in a single monolithic chip. The output frequency of each VCO is established by a single external component, either a capacitor or a crystal, in combination with two voltage-sensitive inputs, one for frequency range and one for frequency control. These inputs can be used to vary the output frequency as shown under typical characteristics for the 'S124. These highly stable oscillators can be set to operate at any frequency typically between 0.12 hertz and 85 megahertz. The output frequency can be approximated as follows:

$$f_o = \frac{5 \times 10^{-4}}{C_{ext}}$$

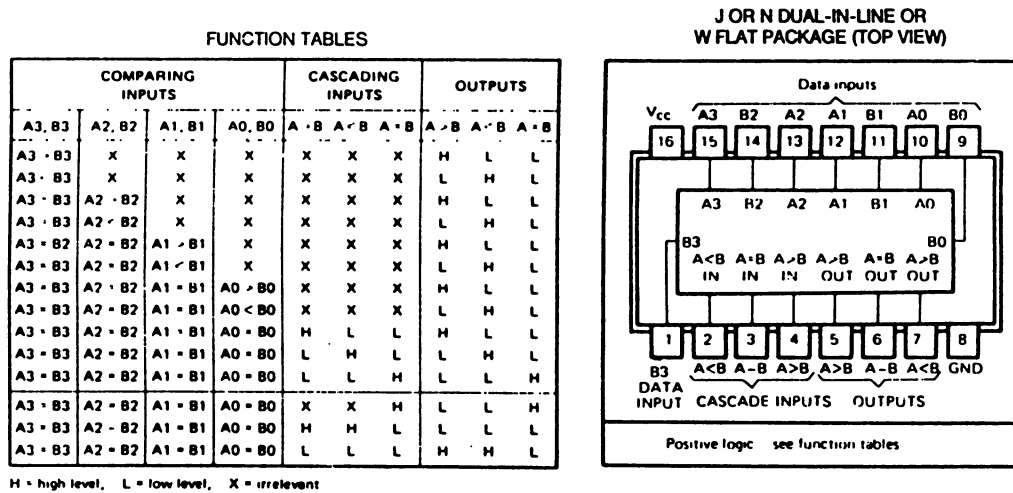
where: f_o = output frequency in hertz

C_{ext} = external capacitance in farads



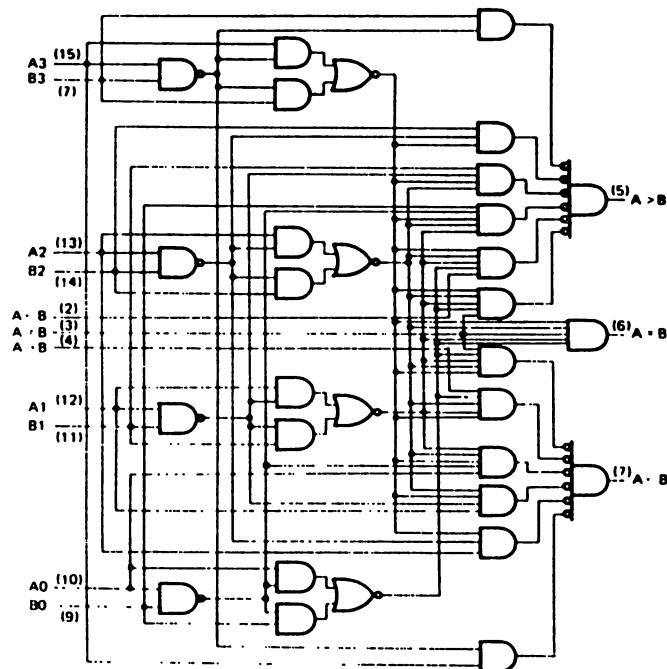
(22) SN74LS85N
4-bit Magnitude Comparators

These four-bit magnitude comparators perform comparison of straight binary and straight BCD (8.4.2.1) codes. Three fully decoded decisions about two 4-bit words (A, B) are made and are externally available at three outputs. These devices are fully expandable to any number of bits without external gates. Words of greater length may be compared by connecting comparators in cascade. The $A > B$, $A < B$, and $A = B$ outputs of a stage handling less-significant bits are connected to the corresponding $A > B$, $A < B$, and $A = B$ inputs of the next stage handling more-significant bits.



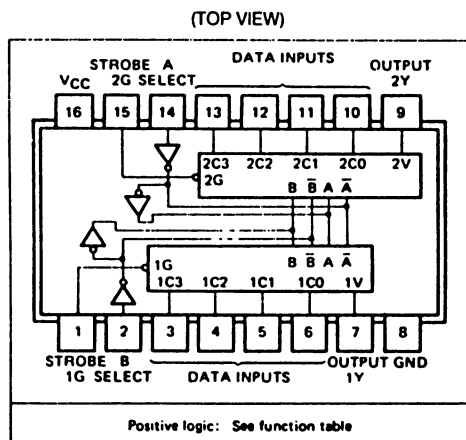
H = high level, L = low level, X = irrelevant

Functional block diagrams



(23) MB74LS153M (SN74LS153N)
Dual 4-Line-to-Line Data Selectors/Multiplexers

Each of these monolithic, data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-inverter gates. Separate strobe inputs are provided for each of the two four-line sections.

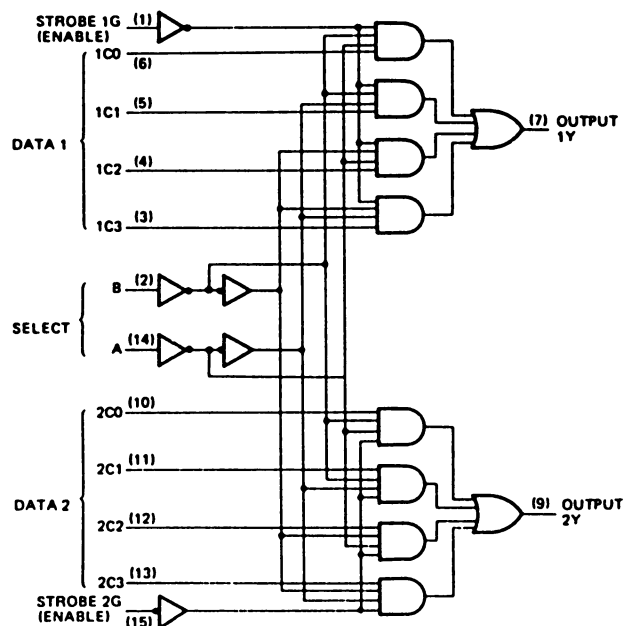


FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	G	V
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L

Select inputs A and B are common to both sections.
H = high level, L = low level, X = irrelevant

Functional block diagram

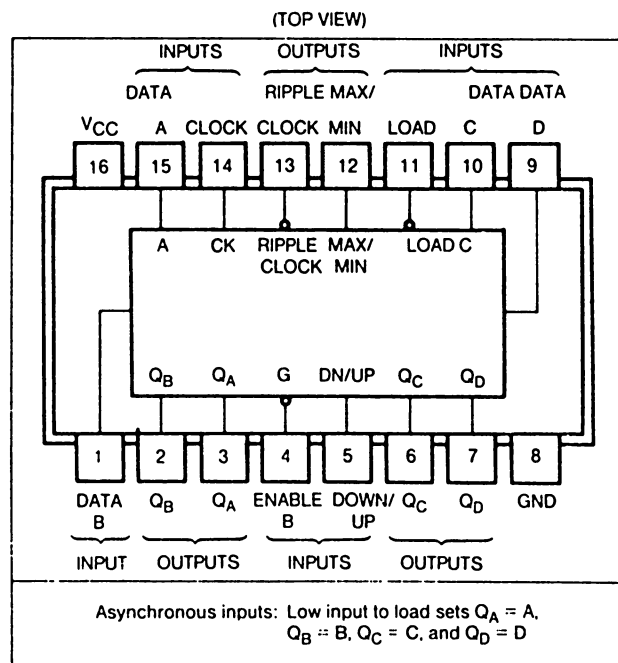


(24) SN74LS191N
Synchronous UP/DOWN Counters
with DOWN/UP Mode Control

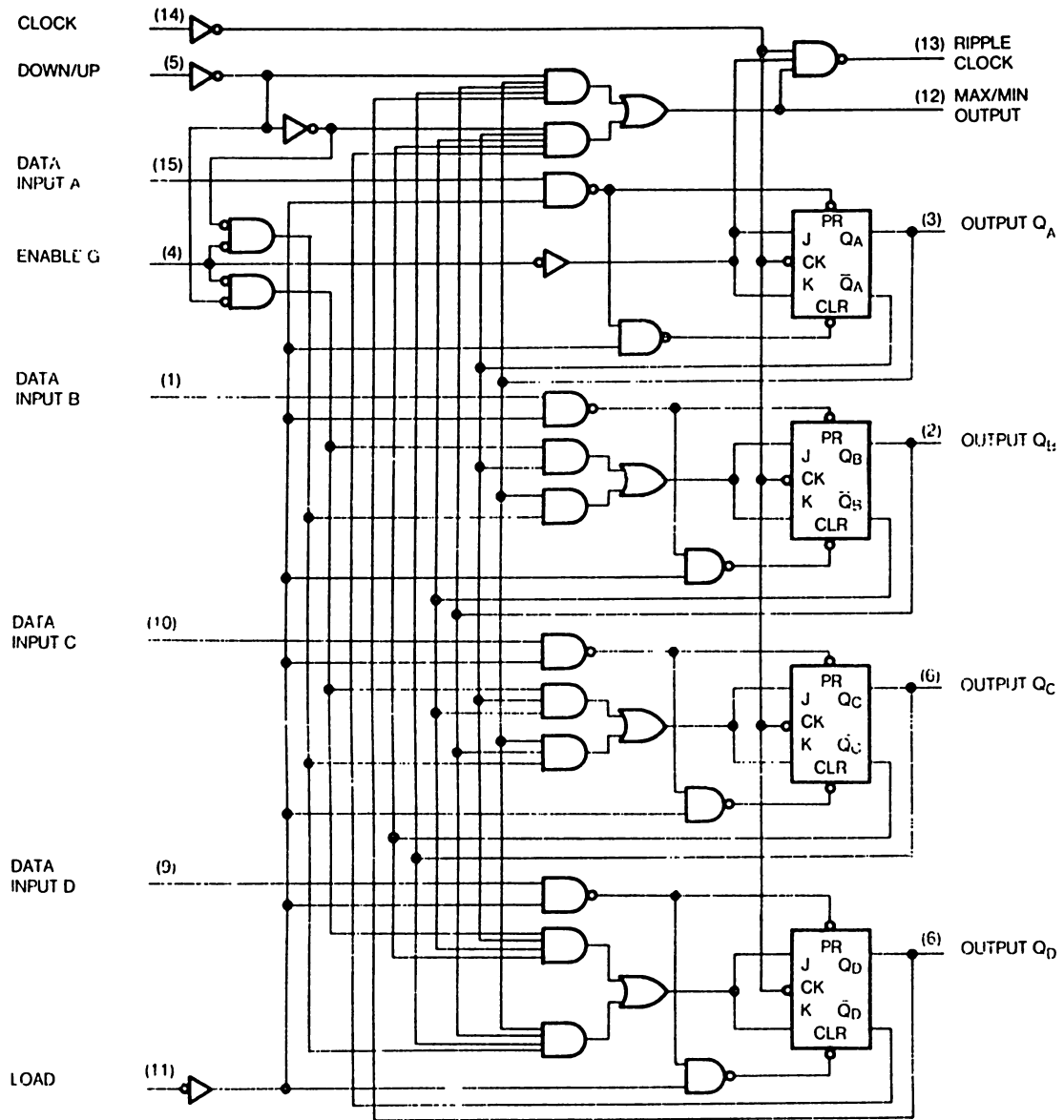
The SN74LS191N is synchronous, reversible up/down counters having a complexity of 58 equivalent gates. The SN74LS191N is 4-bit binary counters. Synchronous operation is provided by having all flip-flop clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four master-slave flip-flop are triggered on a low-to-high-level transition of the clock input if the enable input is low. A high at the enable input inhibits counting. Level changes at the enable input should be made only when the clock input is high. The direction of the count is determined by the level of the down/up input. When low, the counter counts up and when high, it counts down.

These counters are fully programmable; that is, the outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the present inputs.



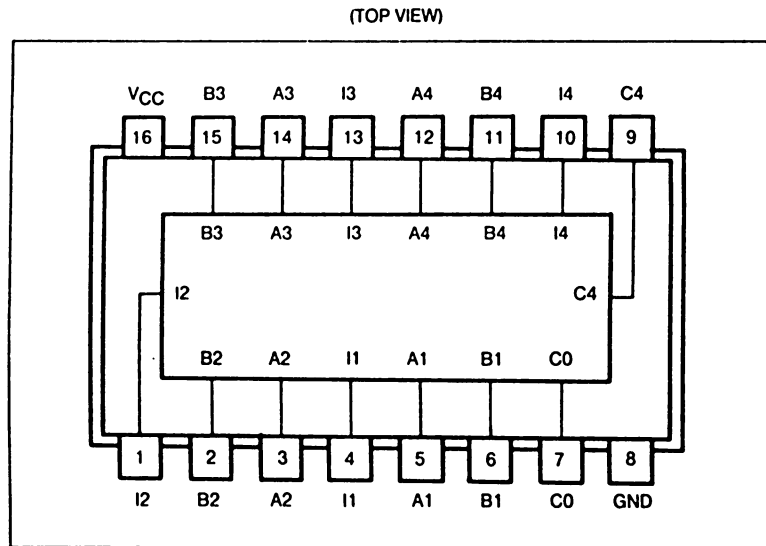
Functional block diagram



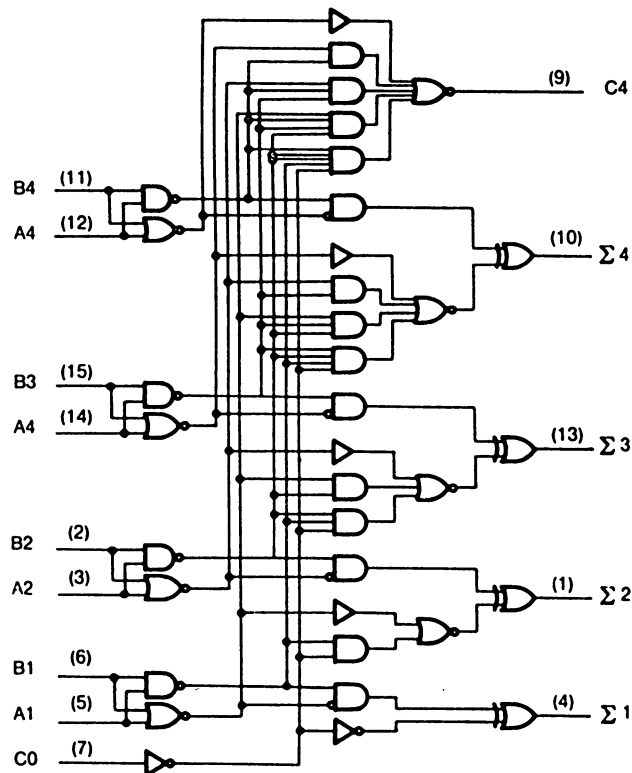
(25) SN74LS283N
4-Bit Binary Full Adders with Fast Carry

These improved 4-Bit full adders/subtractors feature full look-ahead across four bits to generate the carry term in typically 10 nanoseconds. This capability provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation.

These full adders are designed so that levels of the input and output, including the carry, are in their true form. Thus the end-around carry is accomplished without the need for level inversion.

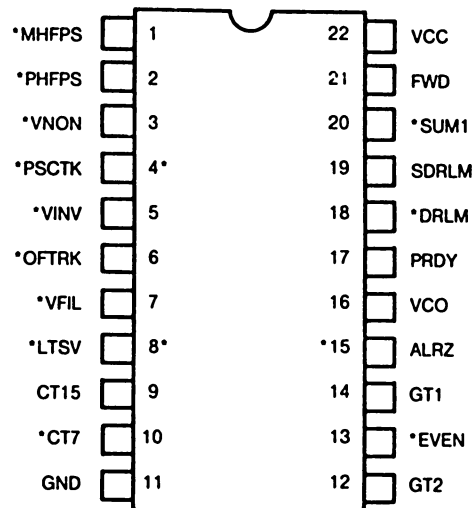


Functional block diagram



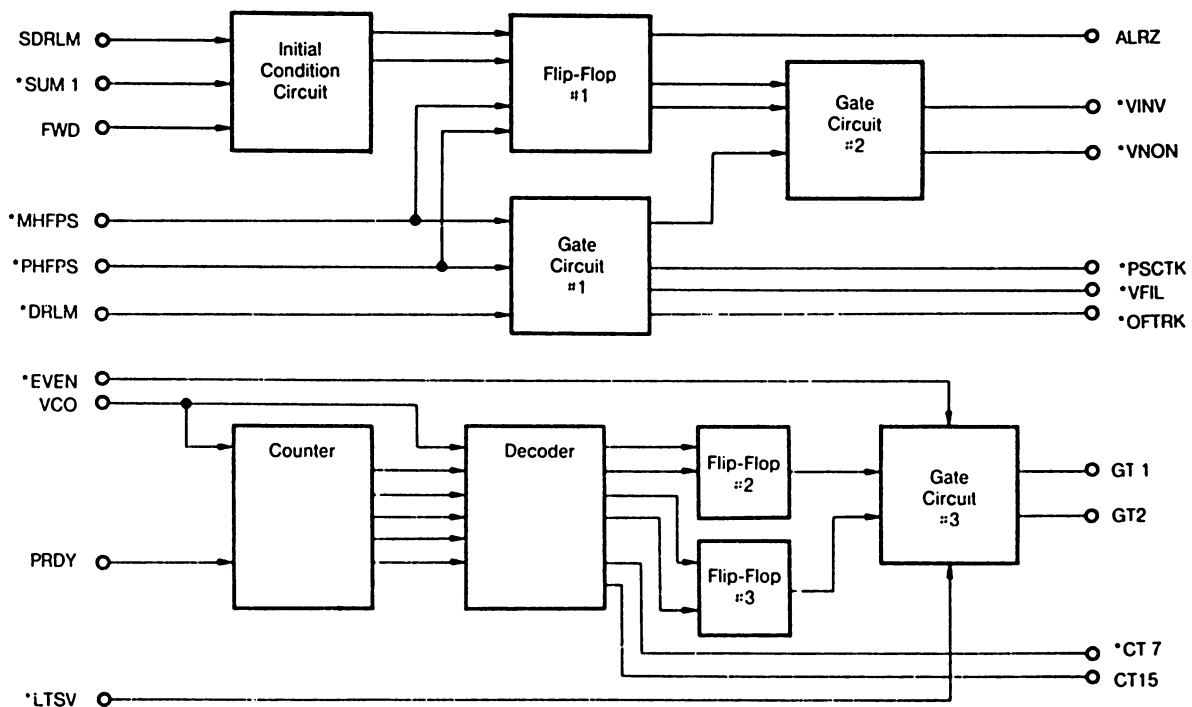
(26) MB14601C
Linear Motor Control

CONNECTION DIAGRAM
(TOP VIEW)



*NOT USED

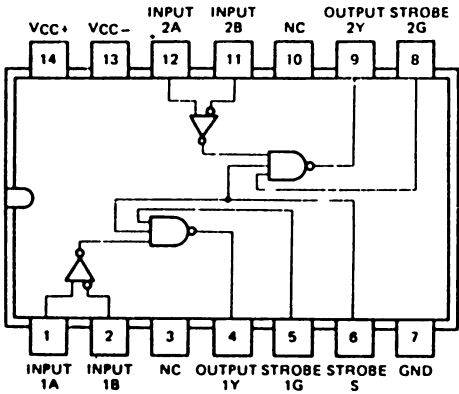
BLOCK DIAGRAM



(27) SN75107AN
Dual Line Receivers

TRUTH TABLE

DIFFERENTIAL INPUTS A-B	STROBES		OUTPUT Y
	G	S	
$V_{ID} \geq 25mV$	L or H	L or H	H
$-25mV < V_{ID} < 25mV$	L or H	L	H
	L	L or H	H
$V_{ID} < -25mV$	H	H	INDETERMINATE
	L or H	L	H
	L	L or H	H
	H	H	L

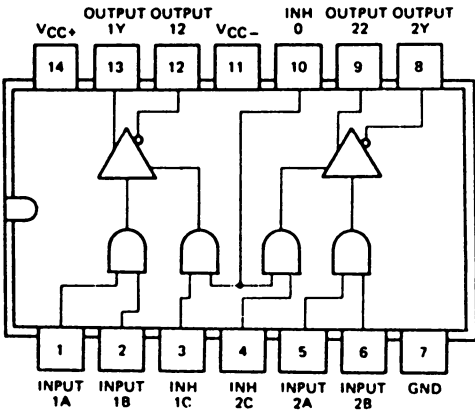


(28) SN75110N
Dual Line Drivers

TRUTH TABLE

LOGIC INPUTS		INHIBITOR INPUTS		OUTPUTS	
A	B	C	D	Y	Z
L or H	L or H	L	L or H	H	H
L or H	L or H	L or H	L	H	H
L	L or H	H	H	L	H
L or H	L	H	H	L	H
H	H	H	H	H	L

Low output represents the on state.
High output represents the off state



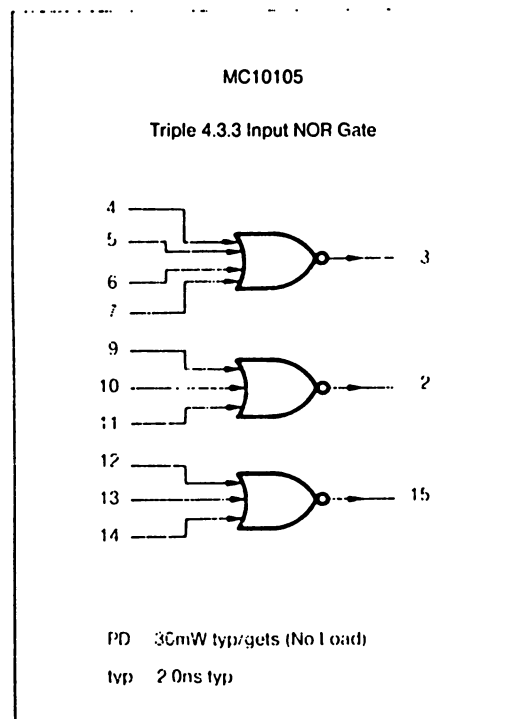
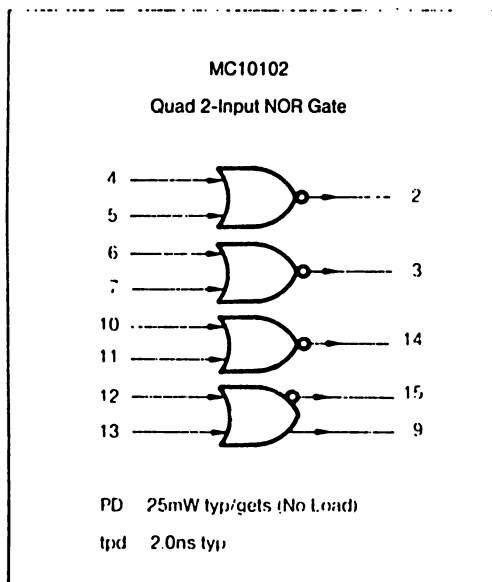
8.4.1 ECL Detail

- (1) MB10102C (MC10102L)
Quad 2-Input NOR Gates
- (2) MD10106C (MC10106L)
Triple 4.3.3 Input NOR Gates

These gates are low power (25mW), high speed (2.0ns) standard MECL logic functions. High impedance input pulldowns allow high dc and ac fanout and eliminate the need to tie unused inputs to an external supply. The open emitter output allow flexibility in the selection of termination techniques and minimize the power requirements when driving transmission lines.

Wire-O Ring of outputs is available with the open emitter outputs. These functions are used in control, bussing, and communications in high speed central processor, high speed peripherals, digital communications systems, minicomputer, and instruments.

The MB10102C is commonly used for control, and for bussing data by using the Wire-O Ring capability of the basic ECL gate.

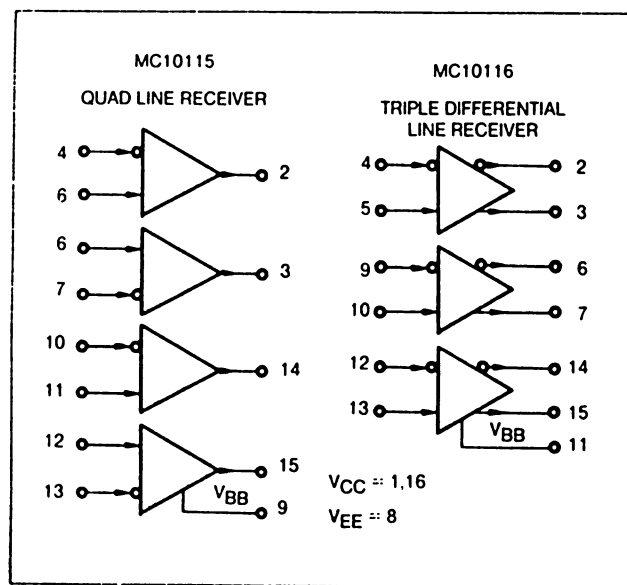


(3) MB10115C (MC10115L)
Quad Line Receiver

(4) MB10116C (MC10116L)
Triple Line Receiver

The line receivers are essentially very high speed linear differential amplifiers with standard ECL outputs. Maximum flexibility is allowed with the open-emitter outputs. Active current sources provide the line receivers with excellent common mode noise rejection. The functions are useful as both digital and linear parts in high speed central processors, minicomputers, peripheral controllers, digital communication systems, and testing and instrumentation systems.

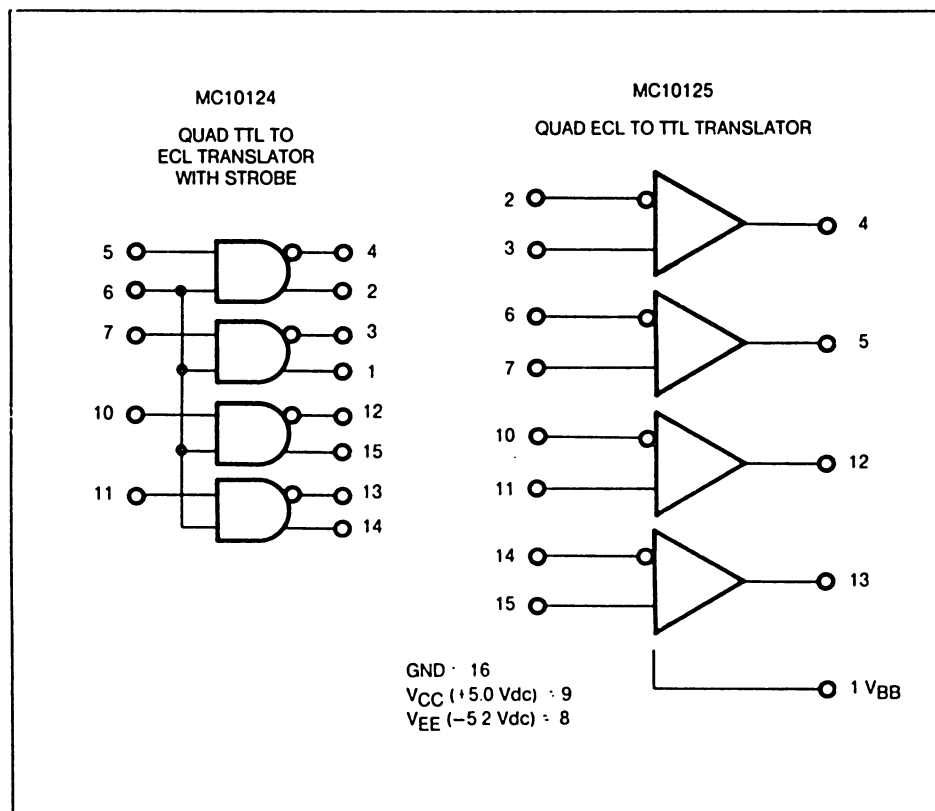
The MB10115C is a quad line receiver with a single output per gate while the MB10116C is a triple line receiver with complementary outputs. Both functions have a V_{BB} reference provided to make the devices useful as Schmitt triggers and to permit them to be used in other applications where a stable reference voltage is necessary. They are also recommended for MOS to ECL interfacing and are used as sense amplifiers for MOS RAM's.



- (5) MB10124C (MC10124L)
Quad TTL to ECL Translator
- (6) MB10125C (MC10125L)
Quad ECL to TTL Translator

The 10124 and 10125 are quad translators for interfacing data and control signals between a high speed ECL section and low speed saturated logic sections of digital equipment. The 10124 has standard TTL inputs and standard ECL, complementary, open-emitter outputs. The 10125 incorporates differential inputs and Schottky TTL "totem pole" outputs. These devices are useful in computers, instrumentation, peripheral controllers, test equipment and digital communication systems.

Power supply requirements are ground, +5Vdc and -5.2Vdc. Propagation delay of the 10124 is typically 5ns. The outputs are identical to those of a standard ECL gate. An advantage of this gate is that the translation can be done in the TTL equipment and then the information can be transmitted, via balanced twisted pair, to the ECL equipment. This isolates the ECL logic from the noisy TTL environment. The 10125 has a typical propagation delay of 5ns with a fanout of 10 TTL loads. The high speed of both of these functions makes them ideal for high speed instrumentation systems and digital communication systems.

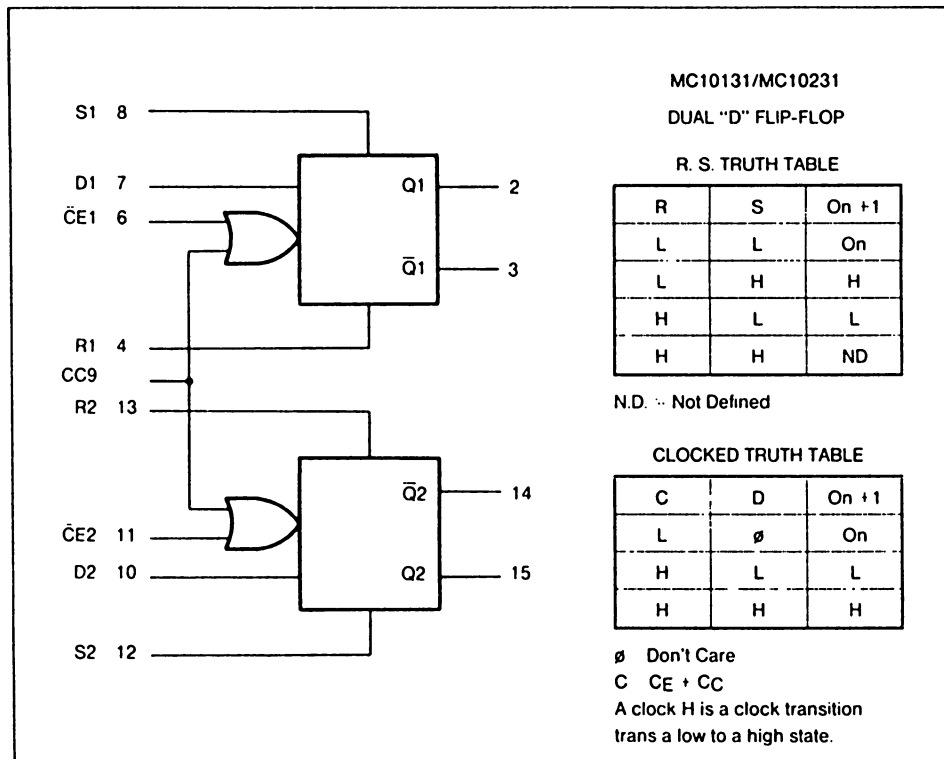


(7) MB10131C (MC10131L)
Dual D-Type Flip-Flop

Dual flip-flops are standard ECL 10,000 storage and counting functions. The inputs incorporate high impedance pulldown resistors. Emitter-follower outputs are left open for maximum flexibility and minimum power dissipation. These functions are very useful for control and storage in high speed digital communication systems, instrumentation and test equipment, high speed central processors, high speed peripheral controllers and mini-computers.

The 10131 is high speed dual D master slave flip-flop with asynchronous set and reset inputs, true and complement outputs.

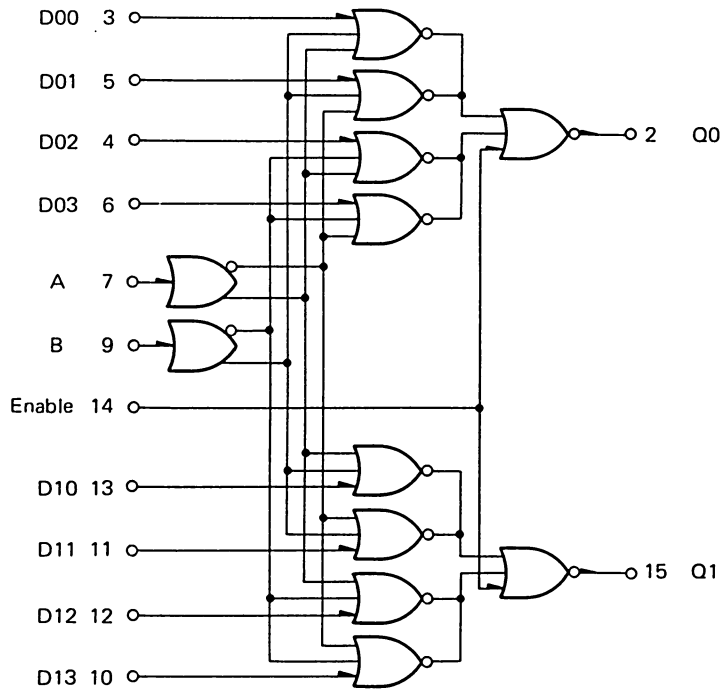
Set and reset inputs override the clock for asynchronous operation of the 10131.



(8) MB10174C (MC10174L)
Dual 4 To 1 Multiplexer

Dual 4 To 1 Multiplexer is a high speed dual channel multiplexer with output enable capability. The select inputs determine one of four active data inputs for each multiplexer. An output enable forces both outputs low when in the high state.

LOGIC DIAGRAM



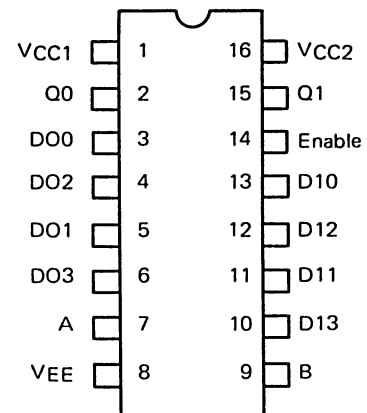
VCC1 = Pin 1
VCC2 = Pin 16
VEE = Pin 8

TRUTH TABLE

ENABLE	ADDRESS INPUTS		OUTPUTS	
E	B	A	Q0	Q1
H	φ	φ	L	L
L	L	L	D00	D10
L	L	H	D01	D11
L	H	L	D02	D12
L	H	H	D03	D13

φ = Don't Care

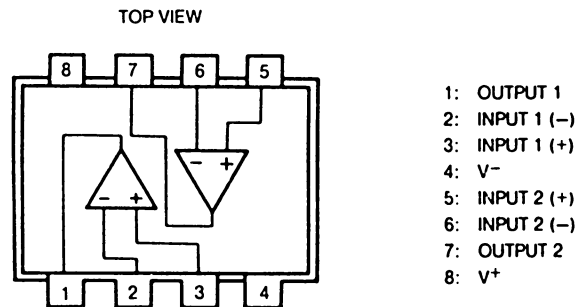
PIN ASSIGNMENT



8.4.2 Linear IC Detail

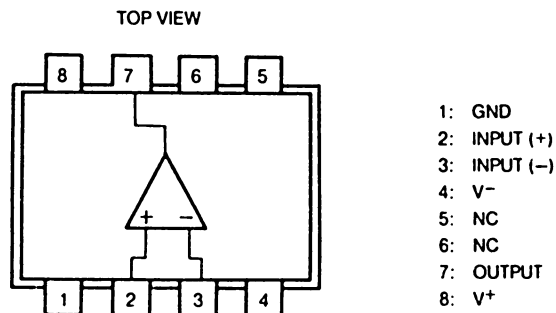
(1) MB3607M (MC1458C) Dual Operational Amplifier

The MB3607M is designed for use as a summing amplifier integrator, or amplifier with operating characteristics as a function of the external feedback components.



(2) MB4002M High Speed Differential Comparator

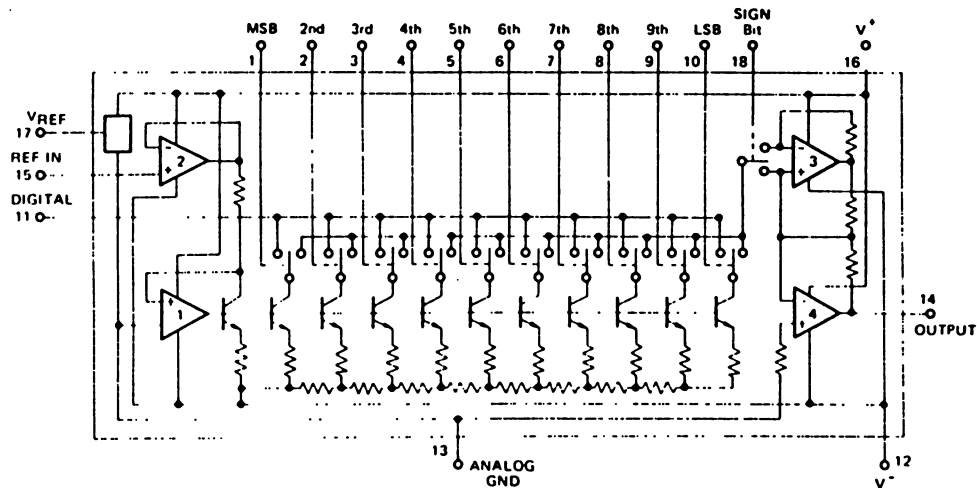
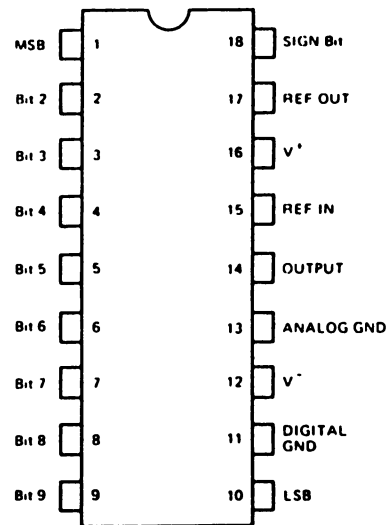
The MB4002M is a Differential Voltage Comparator intended for applications requiring high accuracy and fast response times. The device is useful as a variable threshold Schmitt trigger, a pulse height discriminator, a voltage comparator in high-speed A/D converters, a memory sense amplifier or a high noise immunity line receiver. The output of the comparator is compatible with all integrated logic forms.



(3) JPC610D
10 bit D/A Convertor

The JPC610D is a complete 10 bit plus sign D/A convertor. All elements of a complete sign/magnitude DAC are included—precision voltage reference, current steering logic, current sources, R-2R resistor network, logic controlled polarity switch and high speed internally compensated output of amp. The wide power supply range, low power consumption, choice of full scale output voltages and sign/magnitude coding assure utility in a wide range of applications.

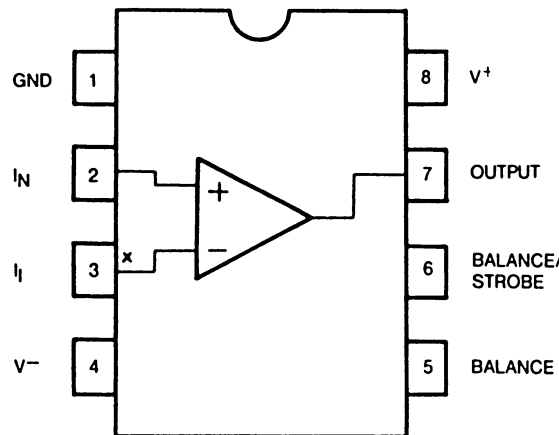
Connection Diagram
(TOP VIEW)



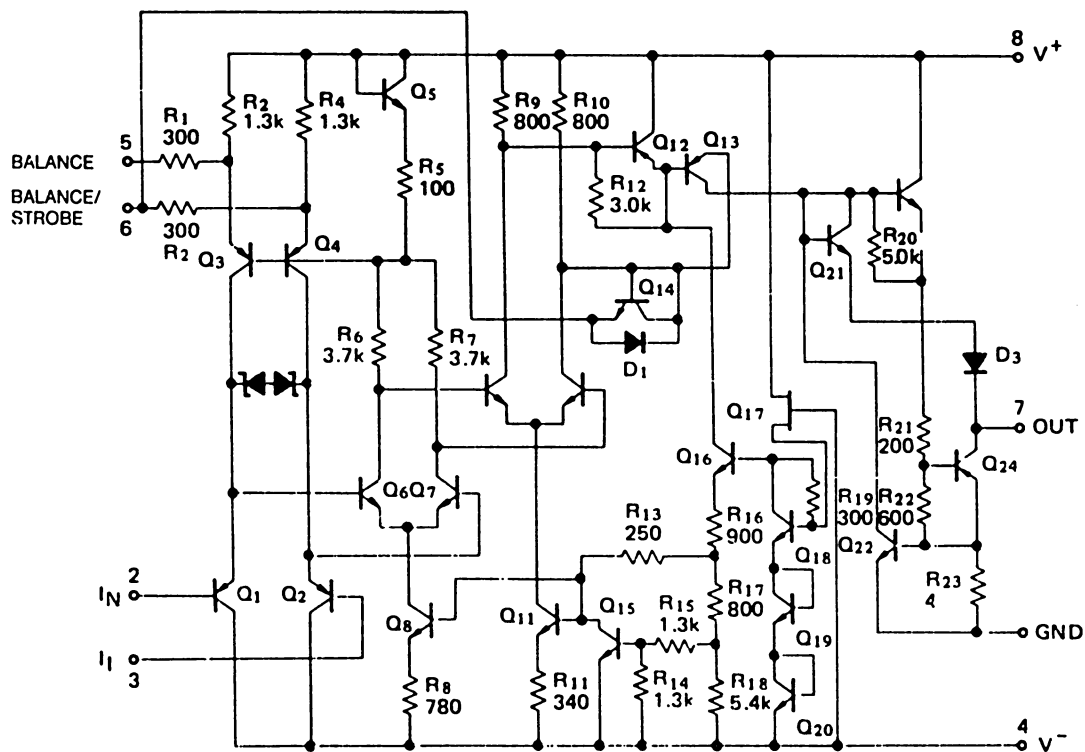
(4) μ JPC271C
Voltage Comparator

This is a single high-speed voltage comparator. This device is designed to operate from a wide range of power supply voltage, including $\pm 15\text{V}$ supplies for operational amplifiers and $+5$ supplies for logic systems. The output level is compatible with most DTL, TTL, and MOS circuits. This comparator is capable of driving Lamps or relays and switching voltage up to 50V at 50mA . All inputs and outputs can be isolated from system ground. The output can drive loads referenced to ground, V_{cc+} , V_{cc-} . Offset balancing and strobe capability are available and the output can be wire-OR connected. If the strobe input is low, the output will be in the off state regardless of the differential input.

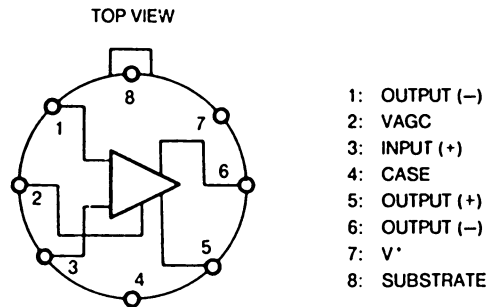
Connection Diagram
(TOP VIEW)



Equivalent Circuit

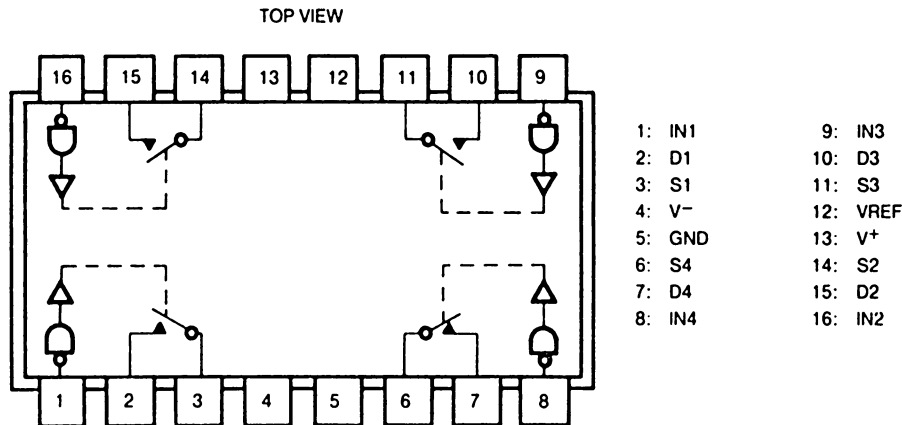


(5) MC1590G
AGC Amplifier



(6) DG201BK
Quad Mono lithic SPST CMOS Analog Switch

The DG201 is a 4-channel single pole signal throw analog switch which employs CMOS technology to insure low and nearly constant ON resistance over the entire analog signal range. The switch will conduct current in either direction with no offset voltage in the ON condition, and block voltages up to 30V peak-to-peak in the OFF condition. The ON-OFF state of each switch is controlled by a driver. With a logic "0" at the input to the driver (0V to 0.8V) the switch will be ON, and a logic "1" (2.4V to 15V) will turn the switch OFF. Switch action is break-before-make.



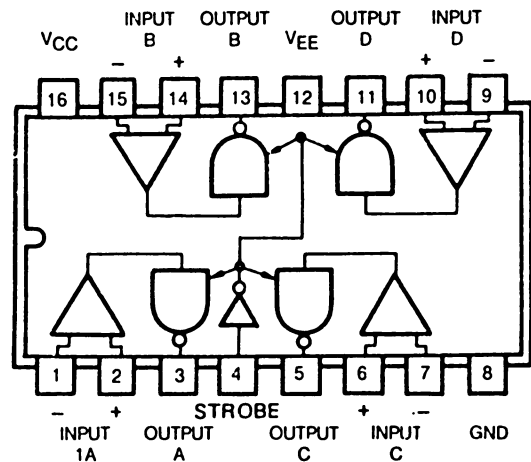
LOGIC	SWITCH
0	ON
1	OFF

(7) MC3450L
Quad Line Receivers

TRUTH TABLE

INPUT		STROBE	OUTPUT
V_{ID}	+24mV	L	H
		H	Z
-25mV	V_{ID}	L	I
		H	Z
V_{ID}	+24mV	L	L
		H	Z

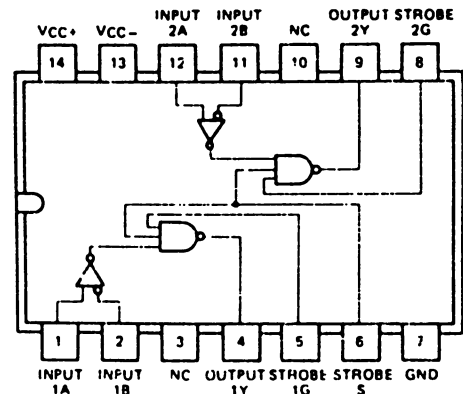
L: Low Logic State
H: High Logic State
Z: Third (High Impedance) State
I: Indeterminate State



(8) SN75108AN
Dual Line Receivers with Open-collector

TRUTH TABLE

DIFFERENTIAL INPUTS A-B	STROBES		OUTPUT Y
	G	S	
V_{ID} 25mV	L or H	L or H	H
-25mV V_{ID} 25mV	L or H	L	H
	L	L or H	H
V_{ID} -25mV	L or H	L	H
	L	L or H	INTERMEDIATE
V_{ID} -25mV	L or H	L	H
	L	L or H	L

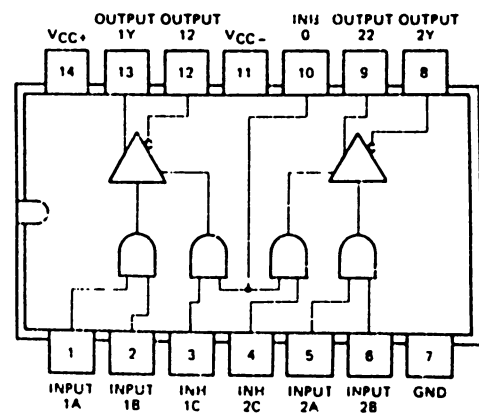


(9) SN75110AN
Dual Line Drivers

TRUTH TABLE

LOGIC INPUTS		INHIBITOR INPUTS		OUTPUTS	
A	B	C	D	Y	Z
L or H	L or H	L	L or H	H	H
L or H	L or H	L or H	L	H	H
L	L or H	H	H	L	H
L or H	L	H	H	L	H
H	H	H	H	H	L

Low output represents the on state
High output represents the off state

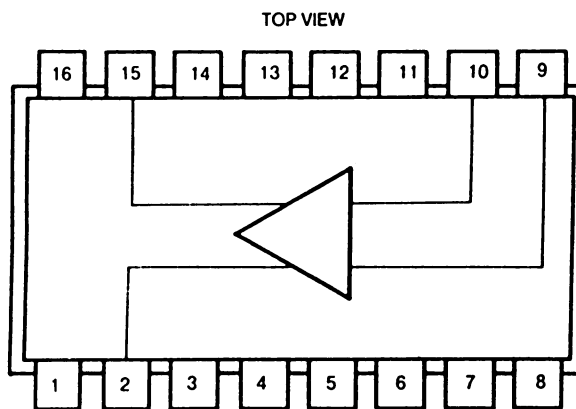


8.4.3 FUJITSU Analog Master Slice IC Detail

(1) MB4301C

Differential Amplifier

The MB4301C is a three-stage Differential input, Differential output Amplifier. All stages are gain-selectable with external resistors.

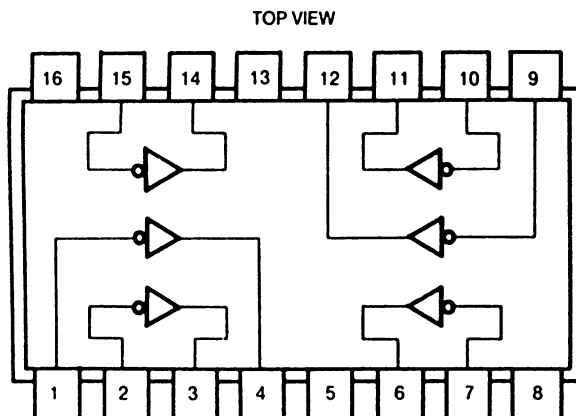


- 1: Vcc2
- 2: OUTPUT 2
- 3: G3A
- 4: G2A
- 5: G2B
- 6: AMP ENABLE
- 7: NC
- 8: GND
- 9: INPUT 2
- 10: INPUT 1
- 11: G1B
- 12: G1A
- 13: GC
- 14: G3B
- 15: OUTPUT 1
- 16: Vcc1

G1A G3A: GAIN
G1B G3B: SELECT
GC : GAIN CHANGE

(2) MB4302C

Head Selection Circuit

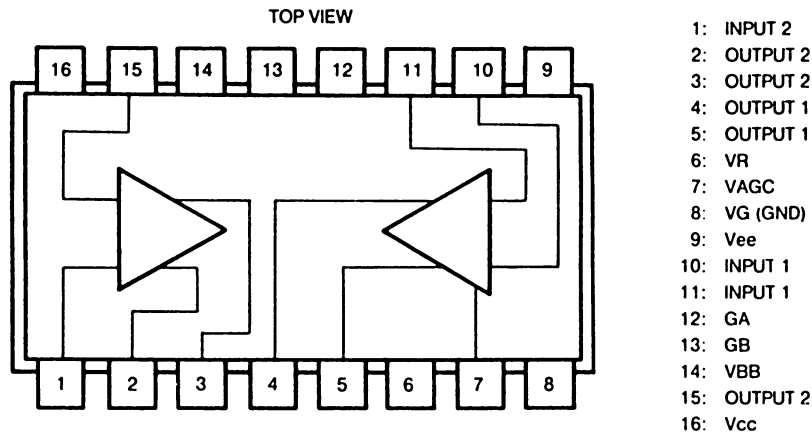


- 1:
- 2:
- 3:
- 4:
- 5: CE
- 6:
- 7:
- 8: GND
- 9:
- 10:
- 11:
- 12:
- 13: CD
- 14:
- 15:
- 16: Vcc

CE: Chip Enable
CD: Detection for Multi selection

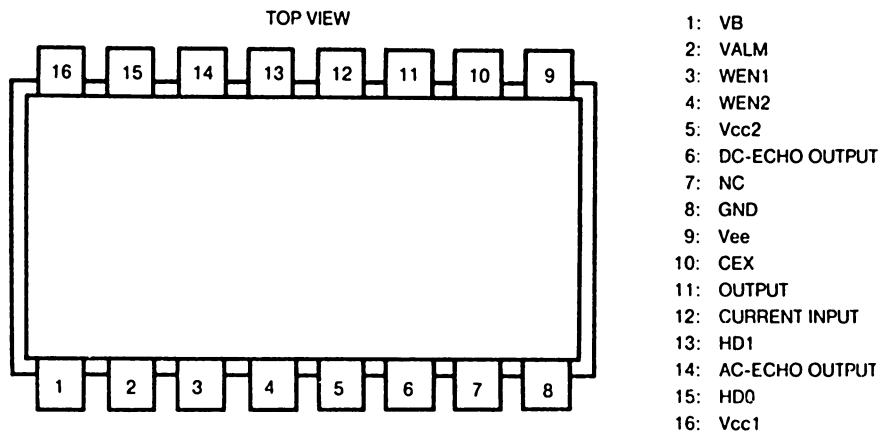
(3) MB4303C
AGC Amp

The MB4303C is an Automatic-Gain-Control Amplifier with Differential Inputs and Outputs. It contains another Differential Amplifier.

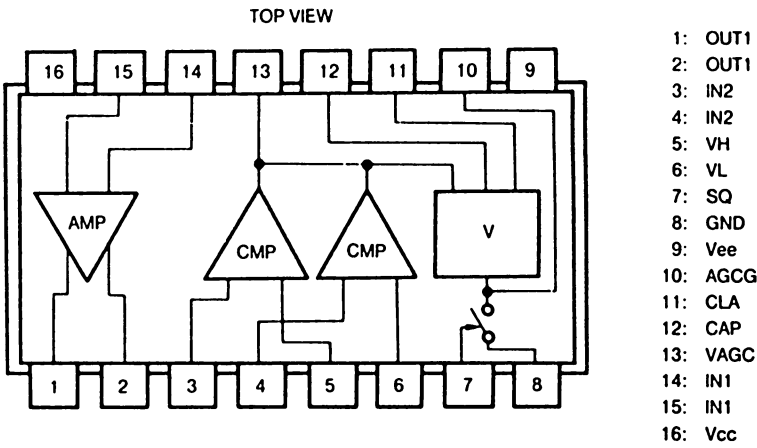


(4) MB4305C
Write Amplifier

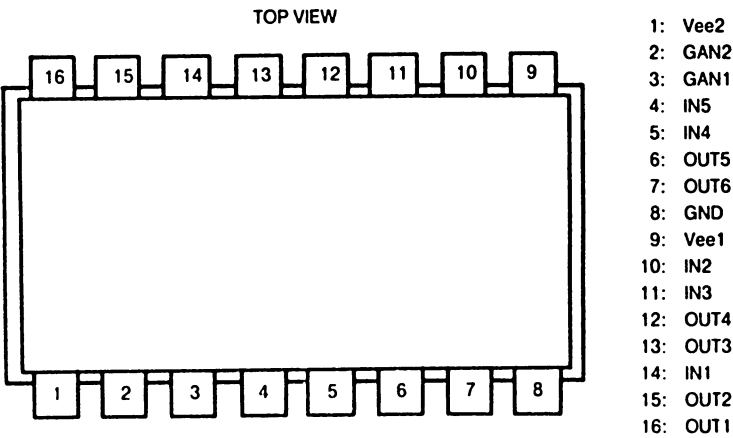
The MB4305C is a Write Amplifier with two write enables (WEN1 and WEN2), AC and DC echo detection output and Current-off circuit in case of power failure.



(5) MB4311C
Charge Pump



(6) MB4316C
R/W Bus Switch



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Section 9

Parts List

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9. PARTS LIST

9.1 ASSEMBLY DRAWINGS (ILLUSTRATION)

The assembly drawing is the illustration that each part of every block was analyzed relationally on the assembly. Each analyzed part is given the number, which corresponds to the number in the INDEX No. column of the list. And mechanical assembly showing which part of the unit is analyzed, is given on the page.

(NOTE) The parts that can't be disassembled on a usual maintenance work are not illustrated in their assembled state, and given a number of the parts. And the quantity of parts, and specification are entered in the list corresponding to the number of parts.

When all parts are entered in the list, the INDEX No. column will be blank.

9.2 LIST

The quantity of parts, the name of parts and specification are entered corresponding to the number of the illustration.

9.2.1 Index No.

A number is assigned on each part in the illustration. The number corresponds with the INDEX No. But in case INDEX No. is given at every part of assembly, the column of INDEX No. will be blank.

9.2.2 Composition & Quantity

Quantity of composition represents the major and minor relation to the setting No. of assembly parts. (The left side indicates large assembly, and the parts in the assembly shift to the right in turn).

9.2.3 Specification

Specifications of parts (drawing No.) are represented.

9.2.4 Description

Name of the part (in Japanese), maker of parts and applicable machine etc. are entered.

9.3 EXAMPLE

COMPOSITION & QUANTITY:

"B010-3110-T001A" consists of "B010-3110-V044A", "F6-SWINA-4 x 10S" "B010-3110-V035A" and "F6-SAHT-4 x 6" of these; "B010-3110-V044A" consists of 1-4 of the INDEX No. column, and "B010-3110-V035A" consists of 6-13.

The quantity of each part that is mounted is given by the number in this column.

Parts whose INDEX No. has *mark are maintenance parts.

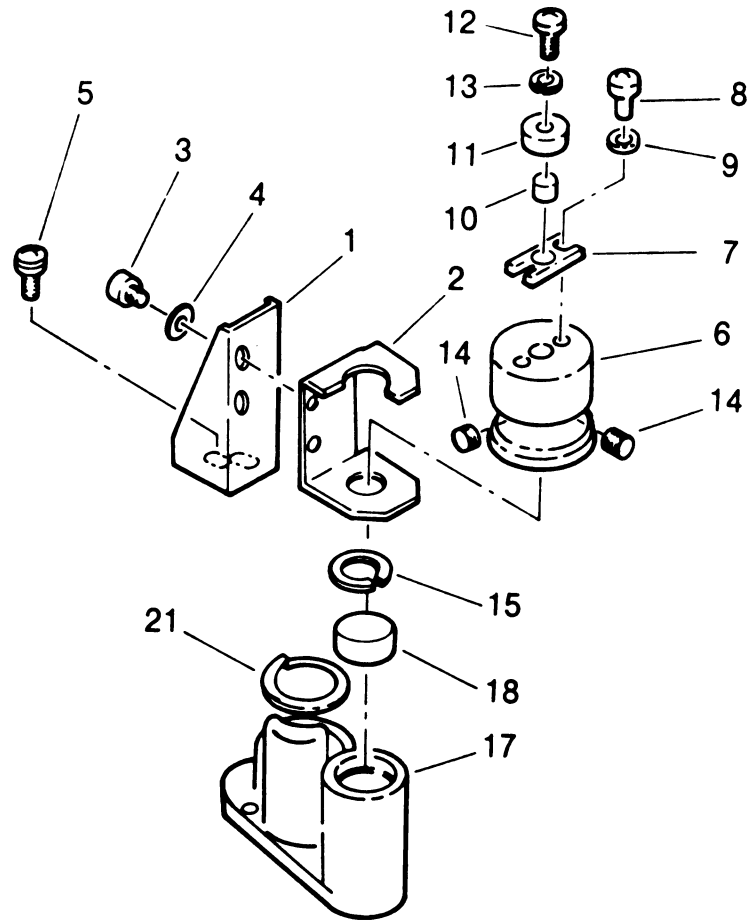


Figure 9.1 PARTS LIST EXAMPLE

Table 9.1 Part List Example

INDEX NO.	COMPOSITION & QUANTITY	SPECIFICATION	DESCRIPTION	CHARACTER	REMARK	REVISION
	1	B010-3110-T001A	Card Reader Unit			
	1	B010-3110-V044A	Guid			
1	1	B010-3110-X098A	Plate			
2	1	B010-3110-Y002A	Plate			
3	2	F6-SNA-3x5S65	Screw			
4	2	F6-WB-3S	Washer			
5	2	F6-SW1NA-4x10S	Screw			
	1	B010-3110-V035A	Eccentric Roller Assy.			
6	1	B010-3110-W026A	Roller Assembly			
	1	B010-3110-X068A	Roller			
7	1	B010-3110-X077A	Plate			
8	2	F6-SNA-3x6S65	Screw			
9	2	F6-WM-3S	Washer			
10	1	B010-3110-X018A	Distance Piece			
11	1	623ZZS	Ball Bearing			
12	1	F6-SNA-3x6S65	Screw			
13	1	F6-WB-3S	Washer			
14	2	F6-SAHT-4x6	Screw			

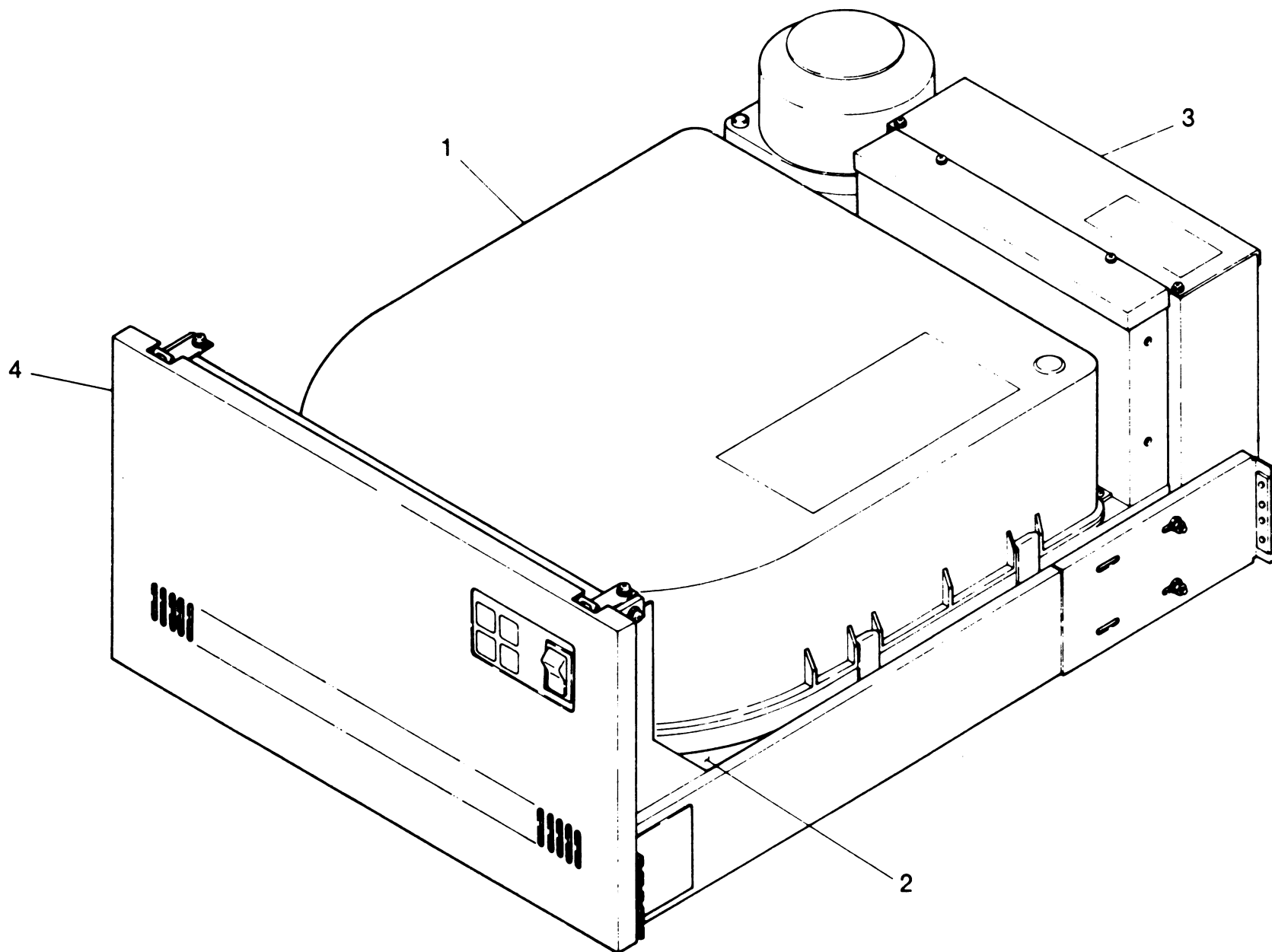


Figure 9.2 FIXED DISK UNIT

Table 9.2 Fixed Disk Unit

INDEX NO.	COMPOSITION & QUANTITY				SPECIFICATION	DESCRIPTION	CHARACTER	REMARK	REVISION
1	1				B03B-4585-B181A	M2298K Fixed Disk		M2298K only	
	1				B03B-4585-B183A	M2298N Fixed Disk		M2298N only	
	1				B030-4540-T012A	Disk Enclosure		M2298 only	
	1				B03B-4585-E511A	Sub Frame Unit		M2298K	
	1				B03B-4585-E512A	Sub Frame Unit		M2298N	
	1				B03-4540-E010A	Gate Unit		M2298	
	1				B03B-4540-E352A	Panel Unit		Optional	
	1				B03B-4540-E353A	Panel Unit 24" Slide		Optional	
4	1				B03B-4540-E354A	Panel Unit 24" Slide		Optional	

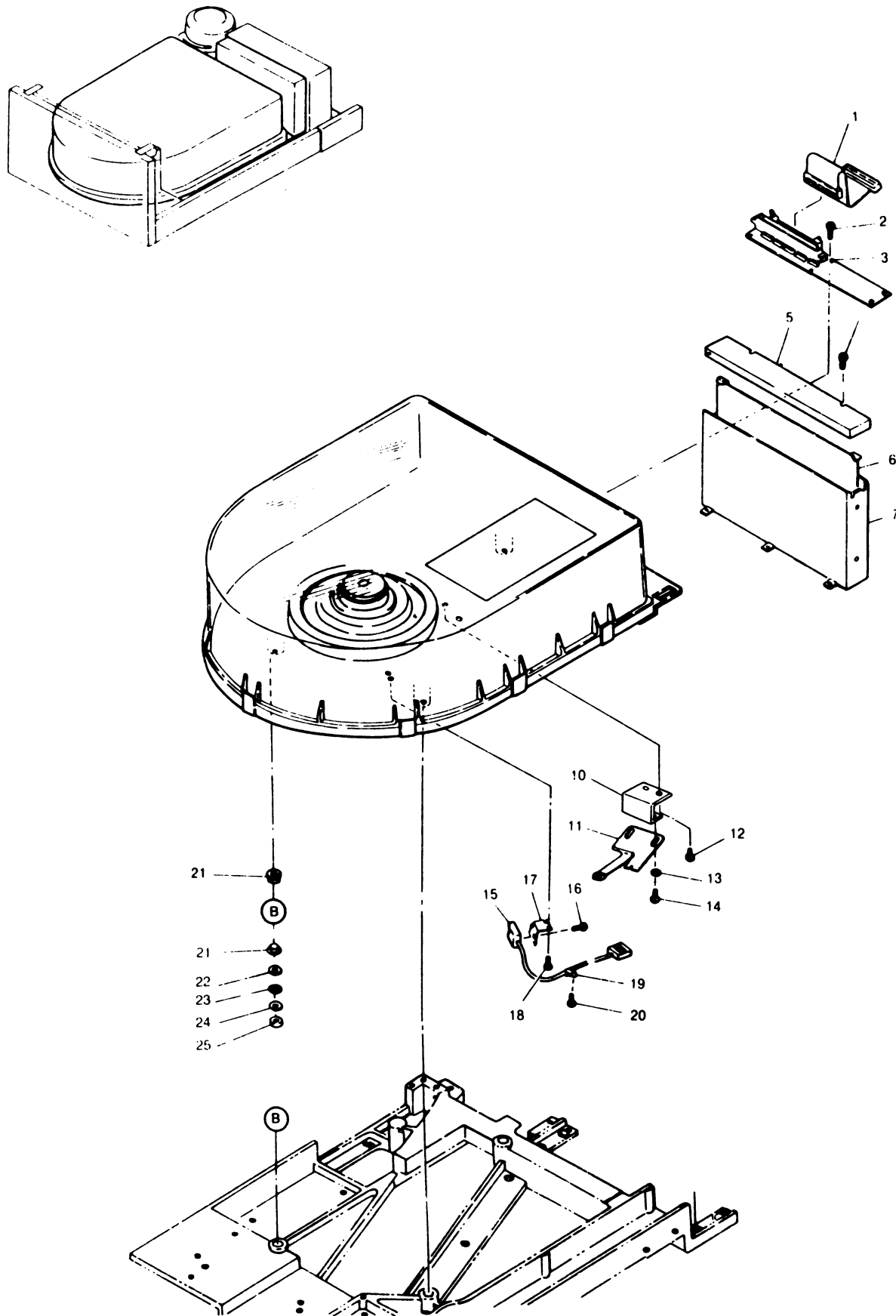


Figure 9.3 DISK ENCLOSURE

Table 9.3 Disk Enclosure

INDEX NO.	COMPOSITION & QUANTITY					SPECIFICATION	DESCRIPTION	CHARACTER	REMARK	REVISION
	1					B030-4540-T012A	Disk Enclosure		M2298	
1		1				B030-4420-W031A	Cable Assy.			
2		5				F6-SW2NA-4x12S	Screw with Washer			
3		1				B16B-8940-0010A	Through Connector I	TISM		
4		2				F6-SW2NA-3x6S	Screw with Washer			
5		1				B030-4420-W370A	Cover Assy.			
*6		1				B16B-9000-0060A	Read Switch	ROWM		
7		1				B030-4540-W042A	Frame Assy.			
10		1				B030-4420-X008A	Plate			
*11		1				B030-4420-W006A	Antistatic Brush			
12		2				F6-SW2NA-4x8S	Screw with Washer			
13		2				F6-WM-4S	Washer			
14		2				F6-SW2NA-4x8S	Screw with Washer			
*15		1				B030-4420-W030A	Switch Assy.		Speed Transducer	
16		2				F6-SW2NA-2.6x5S	Screw with Washer			
17		1				B030-4420-X009A	Plate			
18		2				F6-SW2NA-4x10S	Screw with Washer			
19		3				F6-NYC-2.5	Nylon Clip			
20		3				F6-SW1NA-4x8S	Screw with Washer			
21	6					B030-4420-Y043A	Bush			
22	3					B030-4540-X514A	Rubber packing			
23	3					B030-4540-X513A	Washer			
24	3					F6-WB-8S	Washer			
25	3					F6-NI-8S	Hexagon Nut			

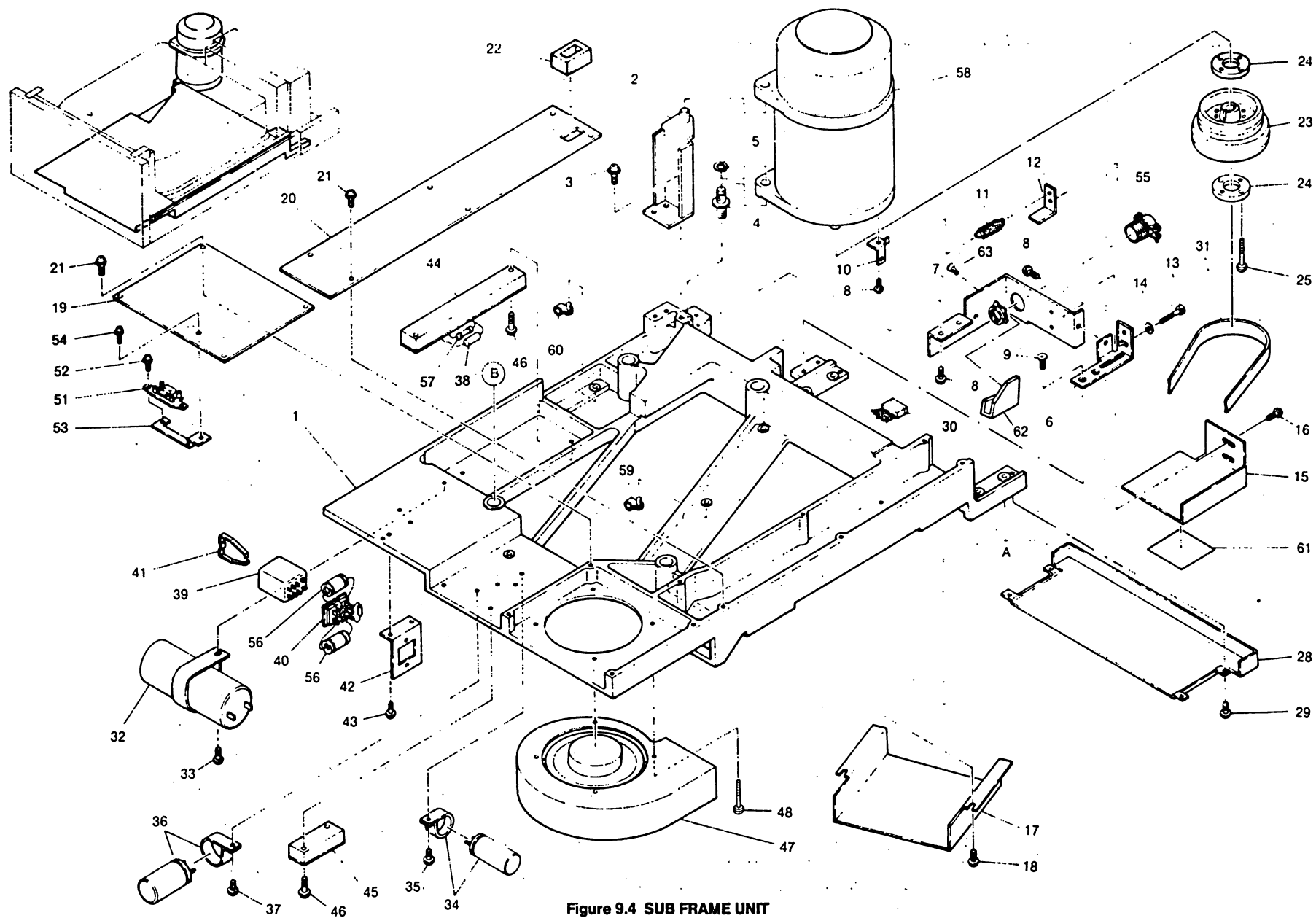


Figure 9.4 SUB FRAME UNIT

Table 9.4 Sub-Frame Unit

INDEX NO.	COMPOSITION & QUANTITY					SPECIFICATION	DESCRIPTION	CHARACTER	REMARK	REVISION
	1					B03B-4585-E511A	Sub Frame Unit		M2298K	
	1					B03B-4585-E512A	Sub Frame Unit		M2298N	
		1				B030-4585-V120A	Sub Frame Assy.			
1			1			B030-4585-X112A	Sub Frame			
2				1		B030-4420-W103A	Pivot			
3				3		F6-SW2NA-4x12S	Screw with Washer			
4				1		B030-4420-X153A	Shaft			
5				1		F6-ER-8sus	Retaining Ring			
6				1		B030-4585-X107A	Plate			
7				1		B030-4585-X101A	Plate			
8				4		F6-SW2NA-4x12S	Screw with Washer			
9				2		F6-SSA-4x12S	Screw			
10				1		B030-4585-X102A	Plate			
11				1		B030-4420-X143A	Spring			
12				1		B030-4420-Z144A	Slide Plate			
13				1		B030-4420-Y154A	Bolt			
14				1		F6-WM-4S	Washer			
15				1		B030-4585-W102A	Motor Cover Assy.			
16				2		F6-SW2NA-4x8S	Screw with Washer			
17				1		B030-4420-W106A	Spindle Cover Assy.			
18				2		F6-SW2NA-4x8S	Screw with Washer			
19				1		B030-4420-X156A	Plate			
20				1		B030-4420-X146A	Plate			
21				10		F6-SW2NA-4x10S	Screw with Washer			
22				1		B030-4420-X109A	Packing			
				1		B030-4585-W114A	Pulley Assy			
23					1	B030-4585-X113A	Pulley			
24					2	B030-1190-Z117A	Tapered Plate			
25					2	F6-SW3NA-4x35S	Screw with Washer			
28				1		B030-4420-X150A	Gate Cover			
29					4	F6-SW2NA-4x6S	Screw with Washer			
30				1		C63L-0670-0011 #5	Housing	CNJ4		
31				1		B30L-1000-0108A #L1026	Belt			

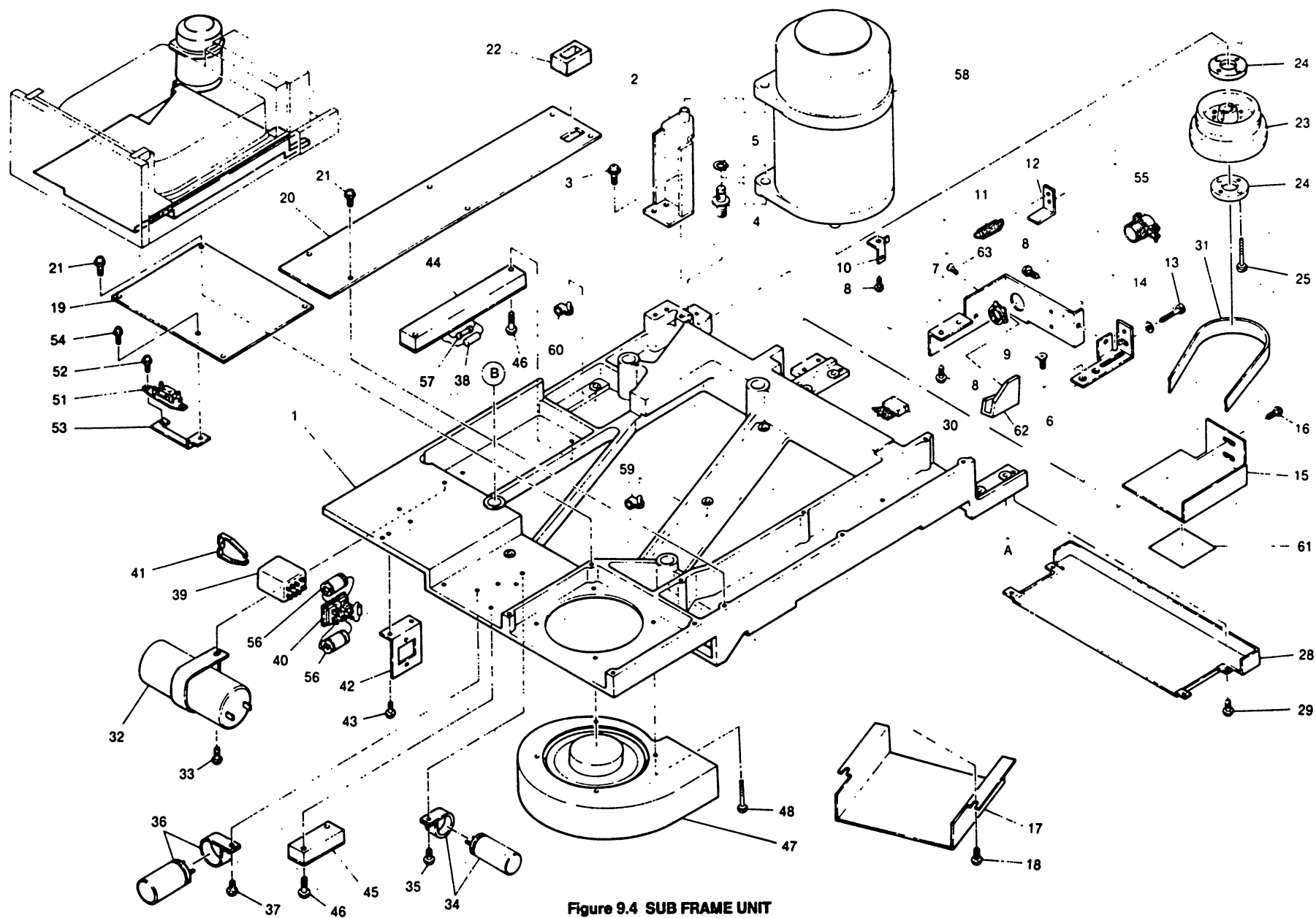


Table 9.4 Sub-Frame Unit (continued)

INDEX NO.	COMPOSITION & QUANTITY					SPECIFICATION	DESCRIPTION	CHARACTER	REMARK	REVISION
32	1					CT-EFL23M326U-U	Capacitor	C3	M2294K/M2298K	
32						CT-EFL45M605U-U	Capacitor	C3	M2294N/M2298N	
33	1					F6-SW2NA-4x10S	Screw with Washer			
34	1					C42L-1520-0001#2E	Capacitor	C2		
35	1					F6-SW2NA-4x10S	Screw with Washer			
36	1					CT-CE62W1E682A#P	Capacitor	C1		
37	1					F6-SW2NA-4x10S	Screw with Washer			
38	1					R010V-1G-10R00-J02	Resistor	R1		
39	1					B58L-0170-0001A	Relay	RL	Brake Relay	
40	1					C58L-0080-0001	Socket			
41	1					C58L-0090-0001	Holder			
42	1					B030-4420-Z106A	Plate			
43	2					F6-SW2NA-4x10S	Screw with Washer			
44	1					C65L-2100-0003	Terminal	TRM3		
45	1					C65L-2100-0008	Terminal	TRM2		
46	4					F6-SW3NA-3x16S	Screw with Washer			
47	1					B90L-1190-0001A	Blower	FAN		
48	4					F6-SW2NA-4x45S	Screw with Washer			
51	1					B57L-0040-0003A	Fan Alarm Assy	FALM		
52	2					F6-SW2NA-3x6S	Screw with Washer			
53	1					B030-4420-X157A	Plate			
54	1					F6-SW2NA-3x6S	Screw with Washer			
55	1					C30L-2010-0001	Clamp			
56	2					N42L-1911-0002 #FQ-13	Spark Killer	SQ1, SQ2		
57	2					C50L-2090-0006	Diode	D1, D2		
58	1					B90L-0980-0002A	Motor	M	M2294K/M2298K	
59	3					CT-AD-04	Clamp			
60	2					CT-AD-11	Clamp			
61	1					B370-0950-0232A	Label			
58						B90L-0980-0004A	Motor	M	M2294N/M2298N	
62	1					B030-4585-X106A	Plate			
63	2					F6-SSA-4x6S	Screw			

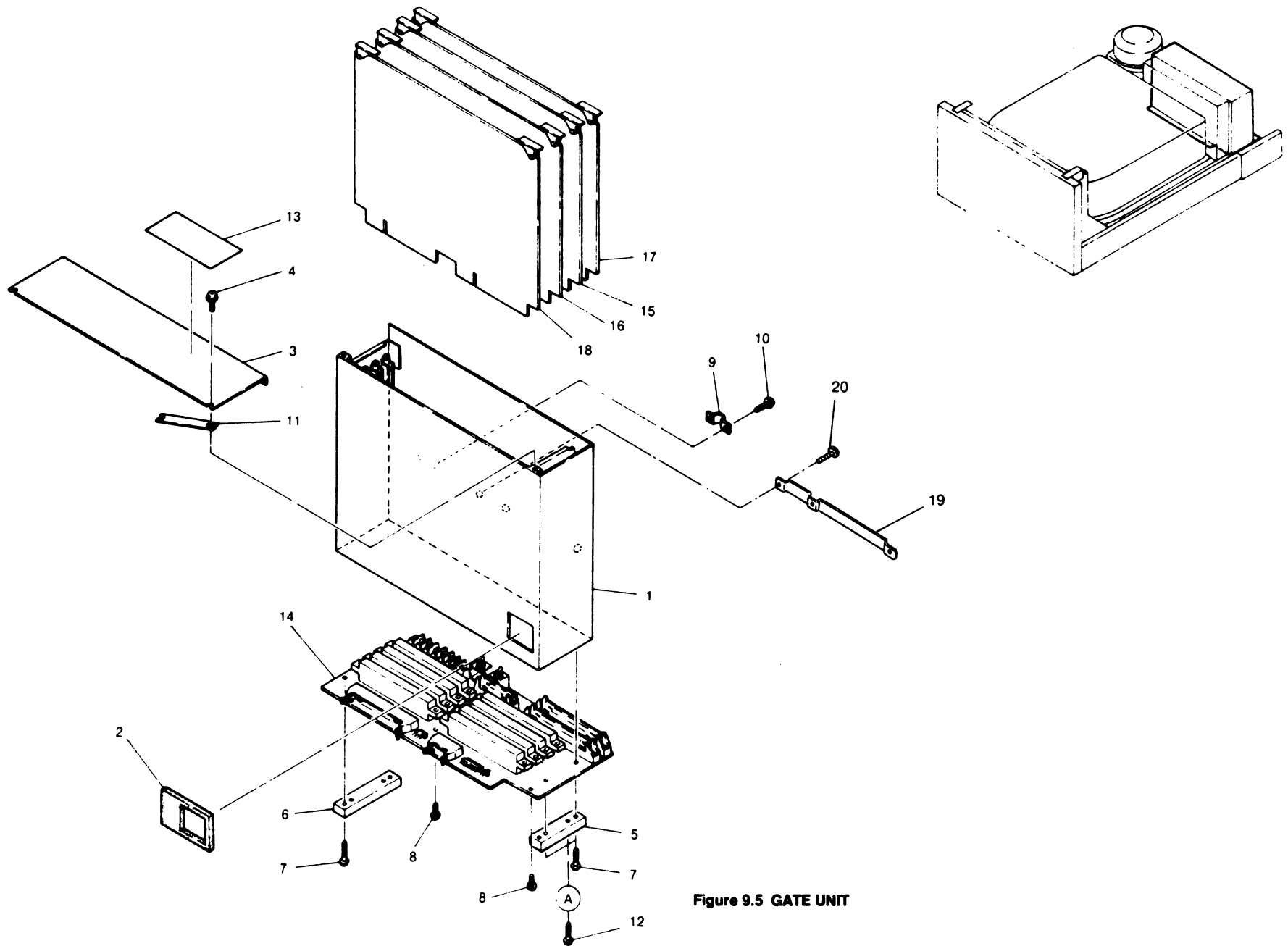


Figure 9.5 GATE UNIT

Table 9.5 Gate Unit

INDEX NO.	COMPOSITION & QUANTITY				SPECIFICATION	DESCRIPTION	CHARACTER	REMARK	REVISION
	1				B03B-4540-E010A	Gate Unit			
		1			B030-4420-V349A	Gate Assy.			
1			1		B030-4420-W351A	Gate Box			
2				1	B030-4420-X306A	Packing			
3				1	B030-4420-W353A	Cover			
4			2		F6-SBD-3x10S	Screw			
5		1			B030-4420-Y314A	Insulator			
6		1			B030-4420-Y315A	Insulator			
7		4			F6-SW2NA-3x12S	Screw with Washer			
8		3			F6-SW2NA-3x6S	Screw with Washer			
9		1			F6-CBHB-10	Holder			
10		2			F6-SW2NA-3x8S	Screw with Washer			
11		1			B030-4420-X319A	Ground Plate			
12		4			F6-SW2NA-4x14S	Screw with Washer			
13		1			B370-0950-0419A	Label			
14		1			B030B-4540-F012A	Gate Circuit R	GBRM		
15		1			B16B-9820-0010A	Variable Oscillator I	VOIM		
16		1			B16B-6150-0050A	Controller W	CWWM		
17		1			B16B-6160-0060A	Controller E	KGEM		
18		1			B16B-8990-0060A	Speed Controller R	SDRM		
19		1			B030-4420-V322A	Holding Plate Assy.			
20		3			SW2NA-3x8S	Screw with Washer			

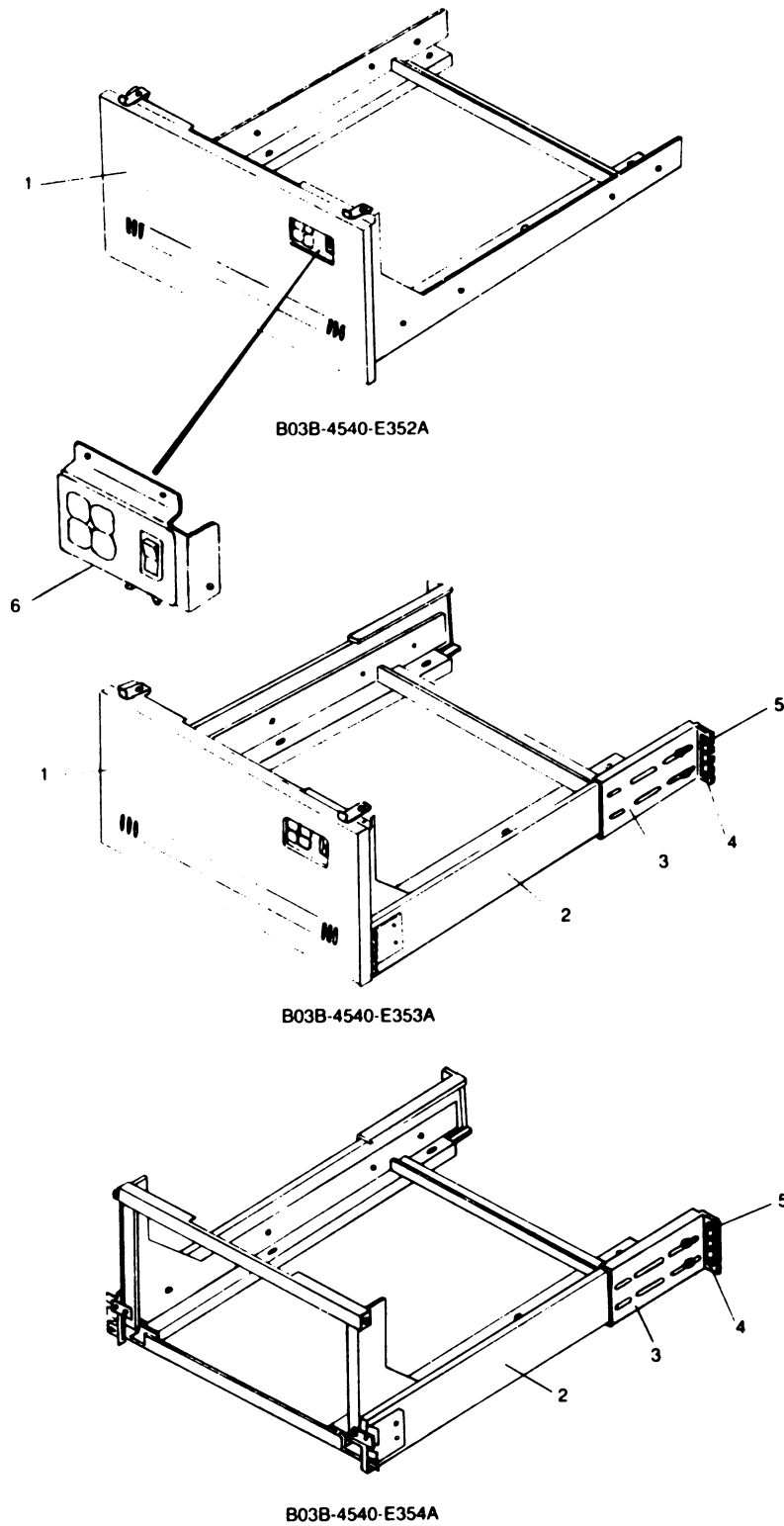


Figure 9.6 Panel Unit

Table 9.6 Panel Unit

INDEX NO.	COMPOSITION & QUANTITY						SPECIFICATION	DESCRIPTION	CHARACTER	REMARK	REVISION
1	1						B03B-4540-E352A	Panel Unit			
		1					B030-4540-W401A	Front Panel			
6		1					N860-3251-T002	Operator Panel			
	1						B03B-4540-E353A	Panel Unit			
1		1					B030-4540-W401A	Front Panel			
2		1					B27L-0230-0004A	Slide Guide		24", 1 pair	
3		2					B030-4540-X418A	Bracket			
4		4					B030-4380-X042A	Nut Bar			
5		16					F6-SW2NA-5x12S	Screw with Washer			
6		1					N860-3251-T002	Operator Panel			
	1						B03B-4540-E354A	Panel Unit			
2		1					B27L-0230-0004A	Slide Guide		24", 1 pair	
3		2					B030-4540-X418A	Bracket			
4		4					B030-4380-X042A	Nut Bar			
5		16					F6-SW2NA-5x14S	Screw with Washer			

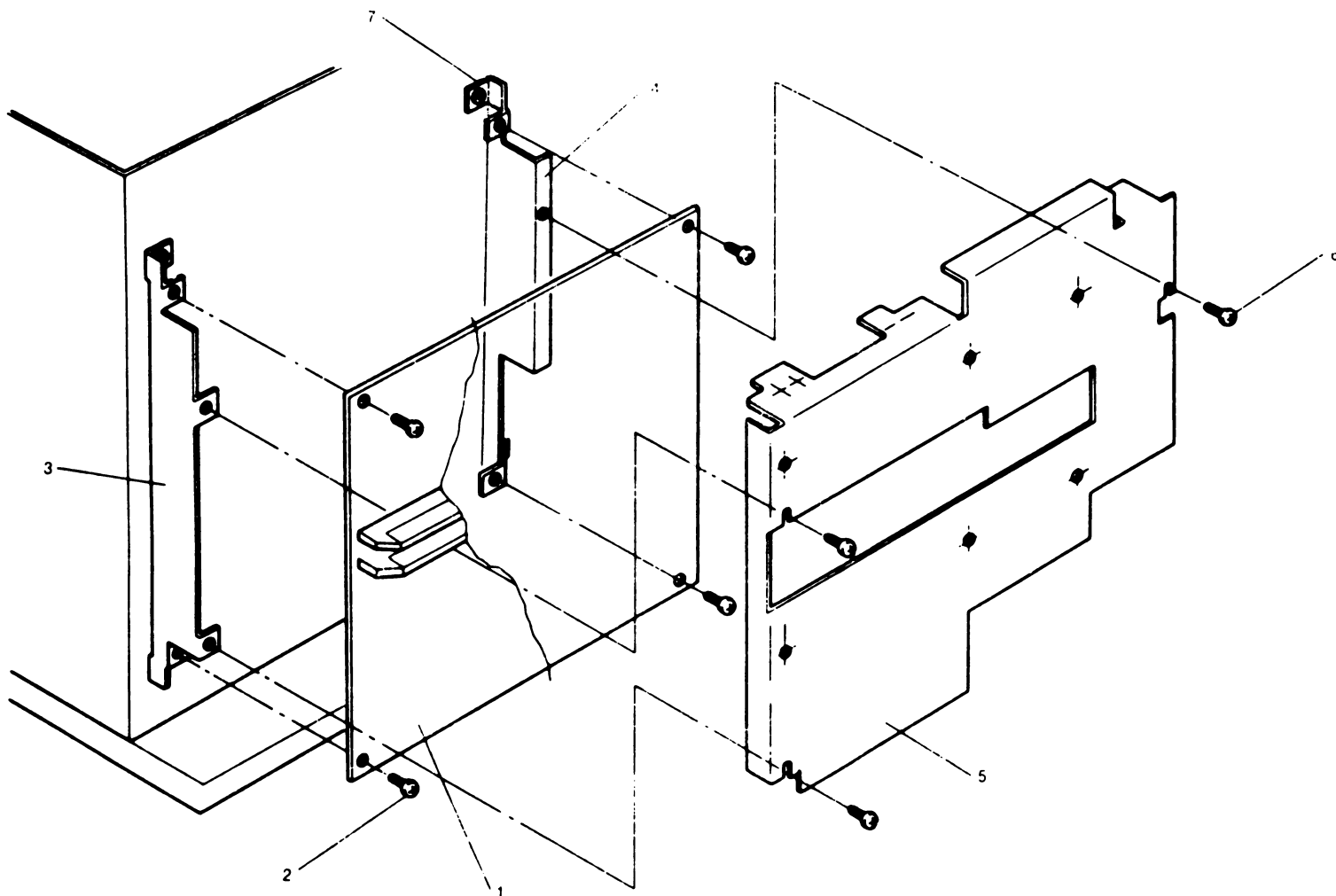


Figure 9.7 Dual Port Unit

Table 9.7 Dual Port Unit

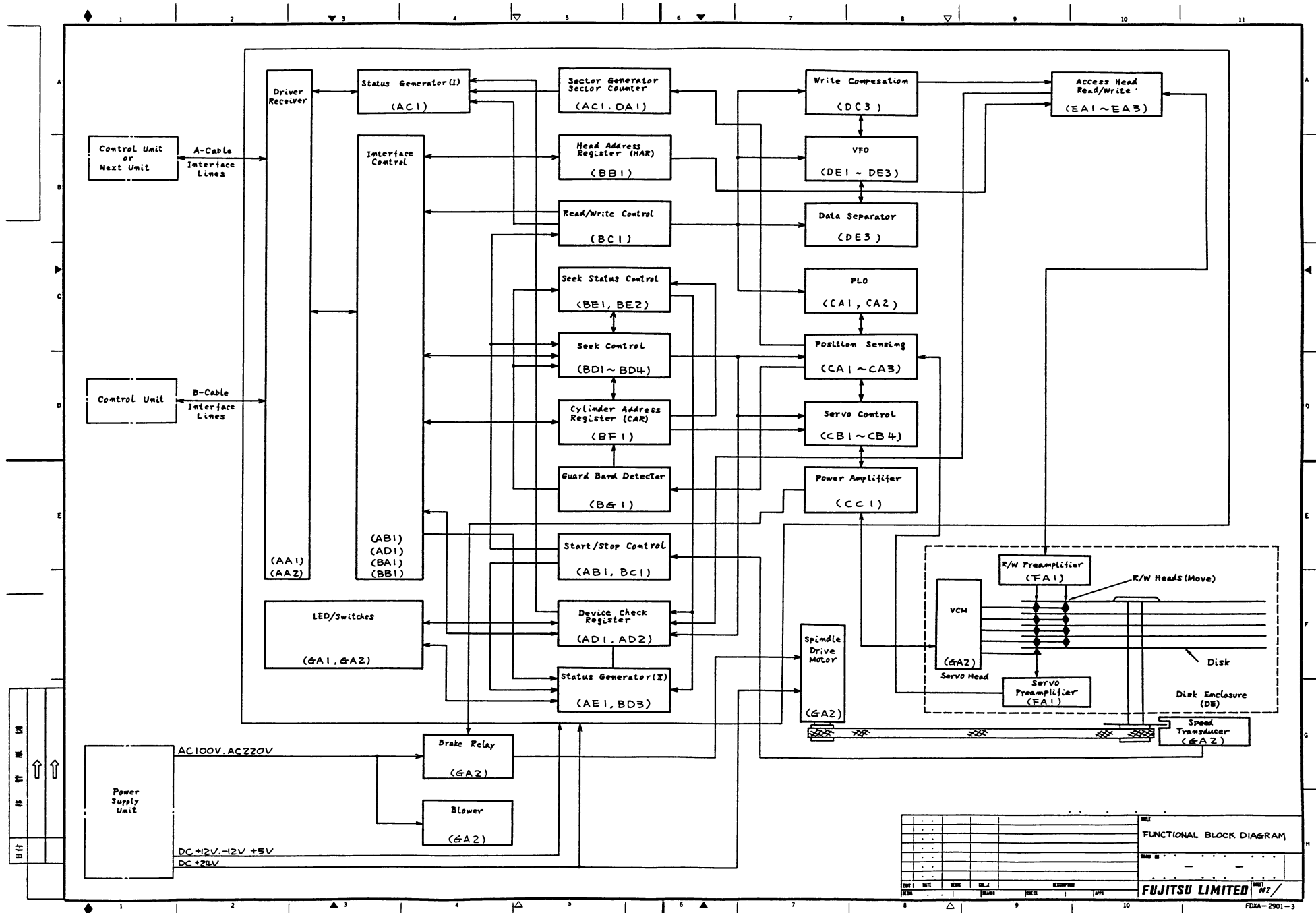
INDEX NO.	COMPOSITION & QUANTITY	SPECIFICATION	DESCRIPTION	CHARACTER	REMARK	REVISION
*1	1	B03B-4540-E901A	Dual Port Unit	XCBM		
2	1	B16B-7990-0020A	Cross Call B			
3	4	F6-SBD-3x6S	Screw			
4	1	B030-4540-X903A	Plate			
5	1	B030-4540-X904A	Plate			
6	1	B030-4540-X901A	Cover			
7	3	F6-SBD-3x6S	Screw			
	4	F6-SBD-3x6S	Screw			
	1	B660-1065-T037A	Cable		50P	
	1	B660-1060-T089A	Cable		10P	
	1	B660-1065-T061A	Cable		26P	

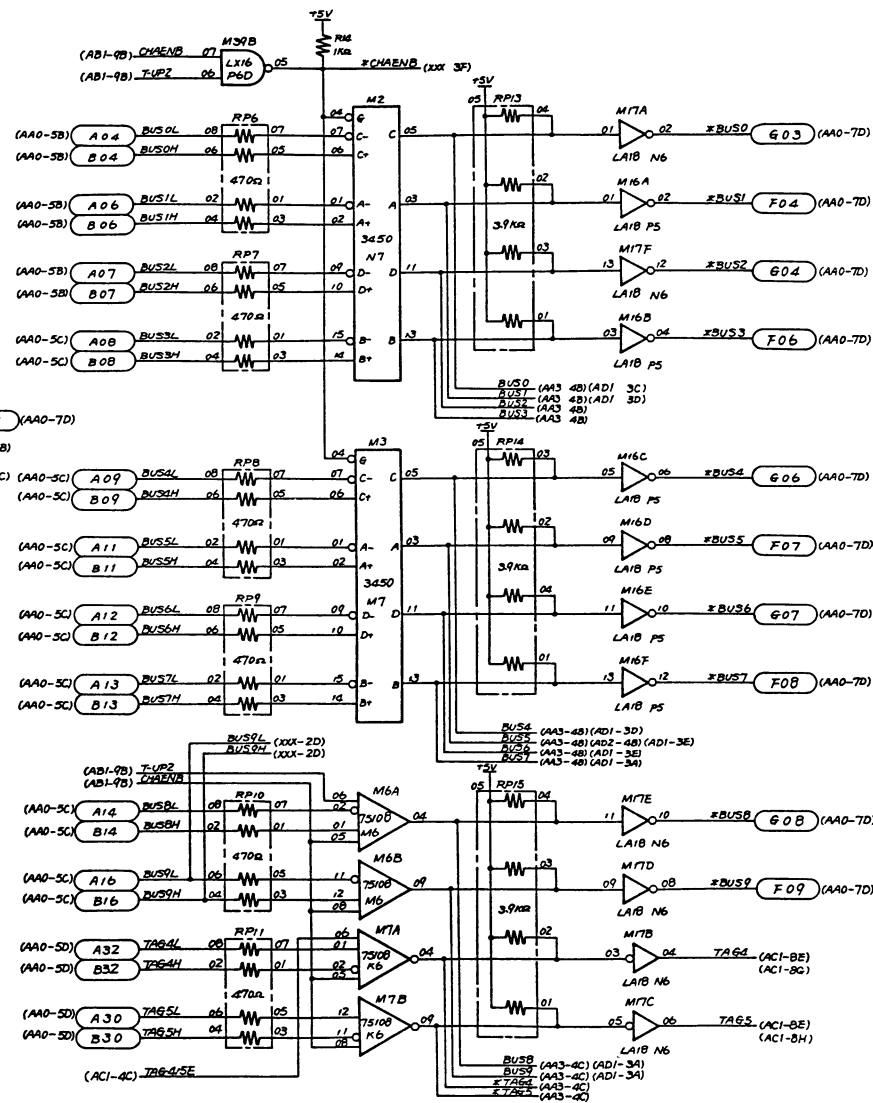
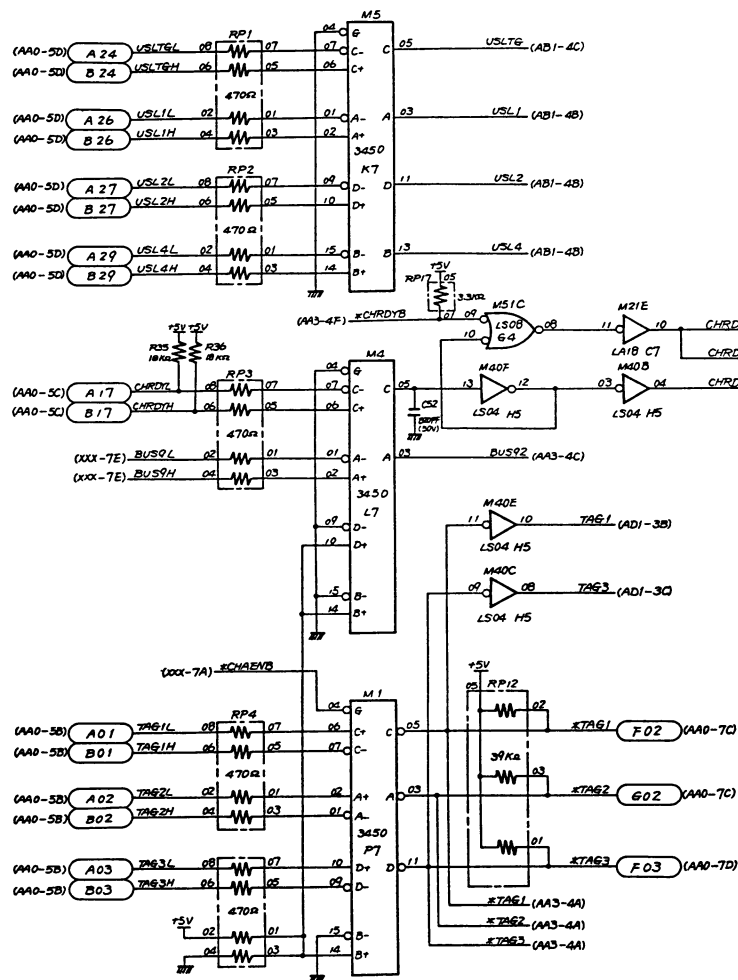
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SHEET	ABBR	TITLE	SHEET	ABBR	TITLE	SHEET	ABBR	TITLE
001		SCHEMATICS/DRAWINGS LIST	031	CB4	POWER DRIVE MPX			
002		FUNCTIONAL BLOCK DIAGRAM	032	CC1	SERVO POWER AMP DRIVE			
003	AA0	KGEM I/O SIGNALS	033	CD1	IC POWER SUPPLY			
004	AA1	A-CABLE RECEIVERS	034	DA0	VOIM I/O SIGNALS			
005	AA2	A/B-CABLE DRIVERS	035	DA1	SECTOR GENERATOR SECTOR/INDEX BUFFER			
006	AA3	DUAL PORT CONNECTION	036	DB1	VFO CONTROL			
007	AB1	UNIT SELECTION START/STOP CONTROL	037	DC1	ENCODER			
008	AC1	SECTOR ADDRESS REG. STATUS GENERATOR (1)	038	DC2	ENCODER/DECODER CONTROL			
009	AD1	CONTROL CHECK DETECTOR	039	DC3	WRITE COMPENSATION			
010	AD2	READ/WRITE CHECK DETECTOR	040	DD1	DECODER			
011	AE1	STATUS GENERATOR (2)	041	DE1	VFO (1)			
012	BA0	CWMM I/O SIGNALS	042	DE2	VFO CHARGE PUMP & VCO			
013	BA1	BUFFERS	043	DE3	VFO (2)			
014	BB1	HEAD ADDRESS REG. OFF SET CONTROL	044	EA0	ROWM I/O SIGNALS			
015	BC1	VFO/PLO CONTROL	045	EA1	READ/WRITE (1)			
016	BD1	SEEK CONTROL (1)	046	EA2	READ/WRITE (2)			
017	BD2	SEEK CONTROL (2)	047	EA3	READ/WRITE (3)			
018	BD3	SEEK CONTROL (3)	048	EA4	READ/WRITE (4)			
019	BD4	SEEK CONTROL (4)	049	FA1	READ/WRITE HEAD, SERVO HEAD PREAMPLIFIER			
020	BE1	SEEK STATUS GENERATOR	050	GA1	I/O CONNECTORS LEDS' SWITCHES			
021	BE2	SEEK ERROR DETECTOR	051	GA2	AC/DC PWER SUPPLY			
022	BF1	CYLINDER ADDRESS REGISTER (CAR)	052		KGEM PCA ASSEMBLY			
023	BG1	GUARD BANDS DETECTOR	053		CWMM PCA ASSEMBLY			
024	CA0	SDRM I/O SIGNALS	054		SDRM PCA ASSEMBLY			
025	CA1	CARRIER AMP PLO PHASE COMPARATOR	055		VOIM PCA ASSEMBLY			
026	CA2	PLO CHARGE PUMP & VCO	056		ROWM PCA ASSEMBLY			
027	CA3	POSITION SENSING	057		GBRM PCA ASSEMBLY			
028	CB1	VELOCITY GENERATOR FINE POSITION DETECT						
029	CB2	DAC ERROR AMPLIFIER						
030	CB3	SERVO CONTROL LOGIC						

SCHEMATICS/DRAWING LIST			
REV C			
DATE	BY	CHKD	APP'D
1984.06.11	2717		
FUJITSU LIMITED			001/57

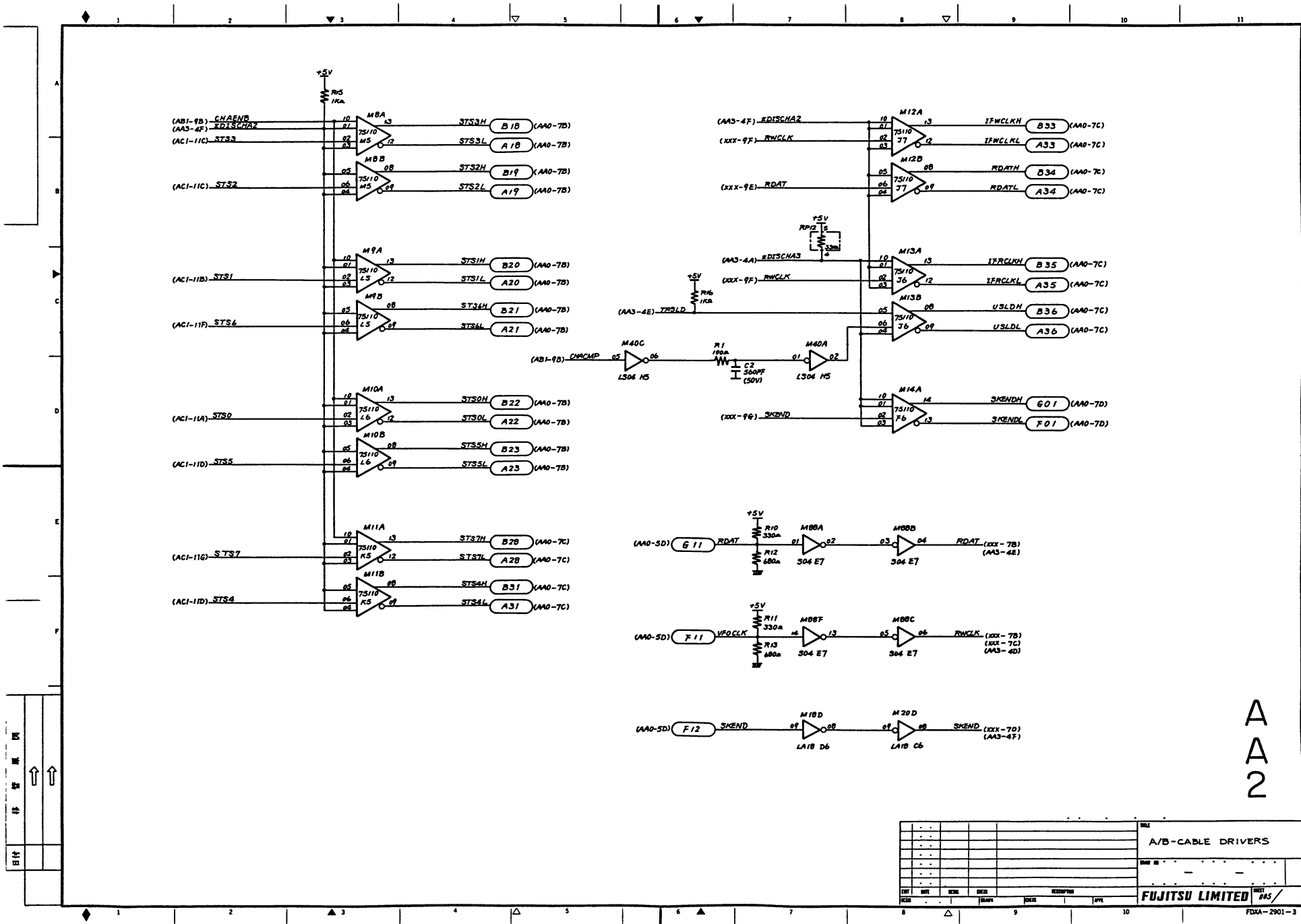
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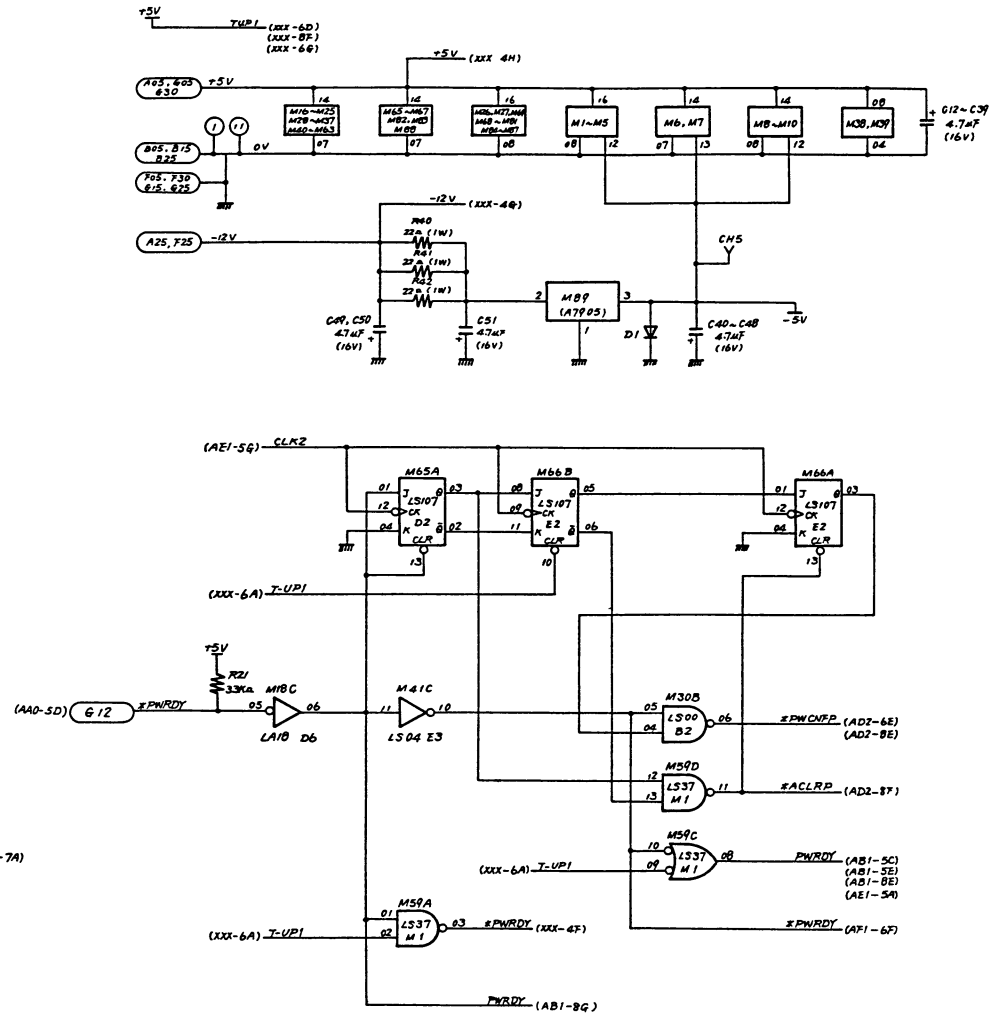
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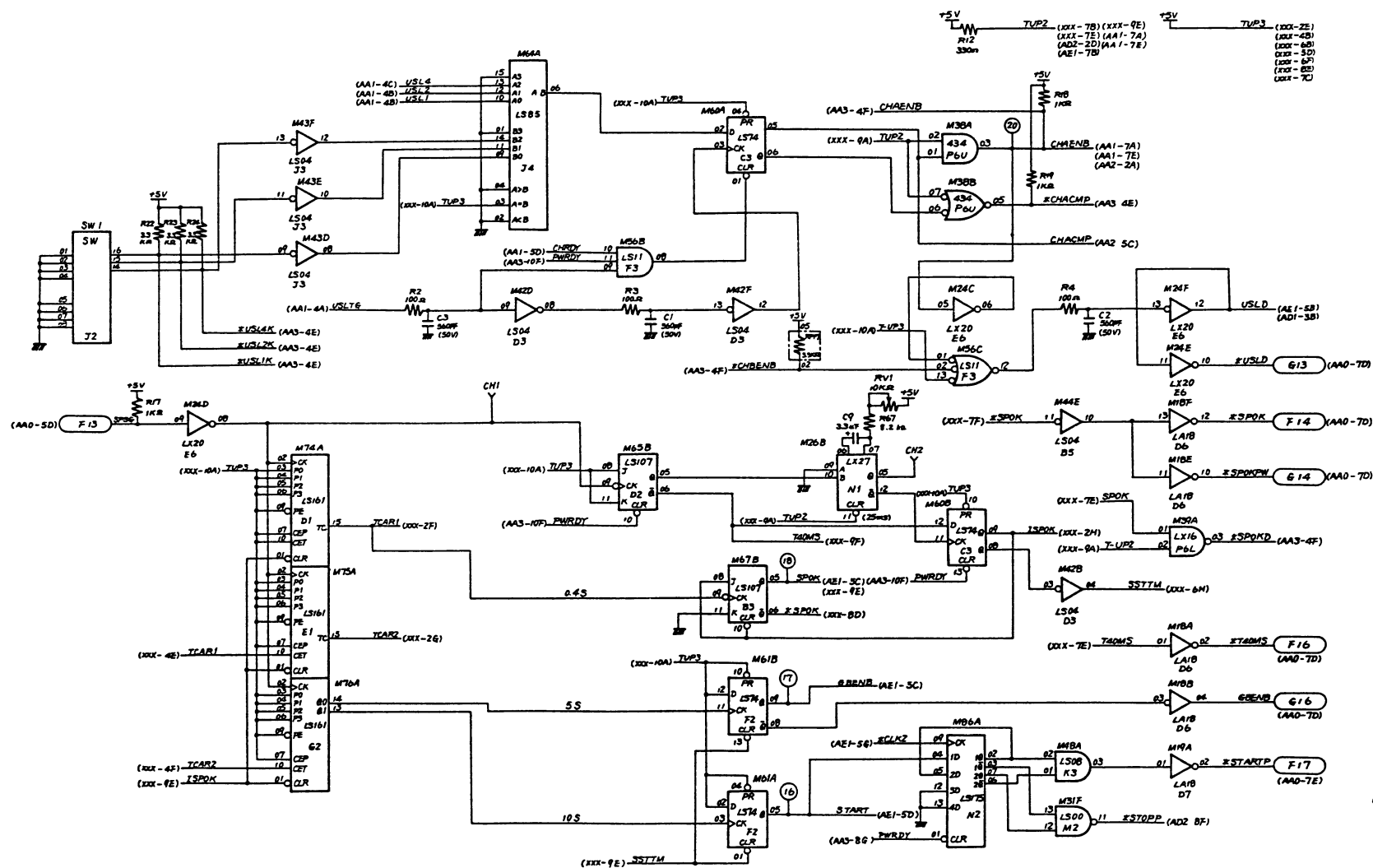
FUJITSU LIMITED

045/

FDXA-2901-3

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DUAL PORT CONNECTION	
PLAN NO.	
CITY	DATE
DESIGNER	CHECKED
DRAWN	APPROVED
FUJITSU LIMITED	SHEET 006 /



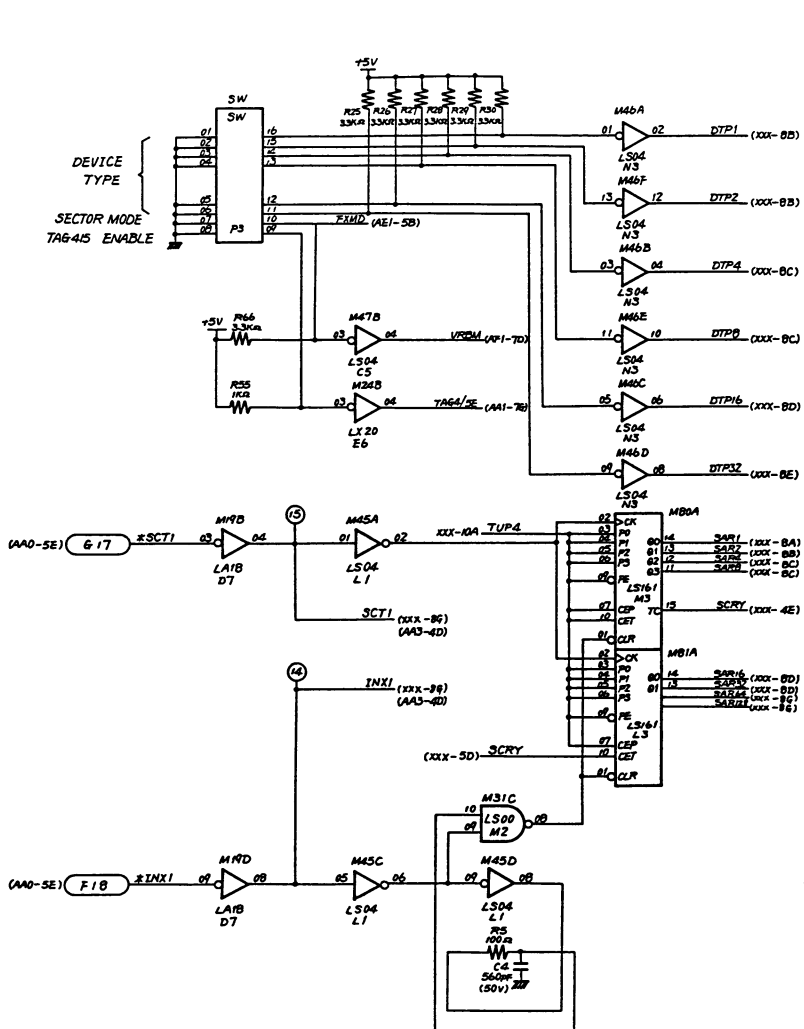
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UNIT SELECTION									
START/STOP CONTROL									
UNIT	MODEL	REVISION	DATE	DESIGNER	DATE	APPROVED	DATE	REMARKS	
UNIT	MODEL	REVISION	DATE	DESIGNER	DATE	APPROVED	DATE	REMARKS	

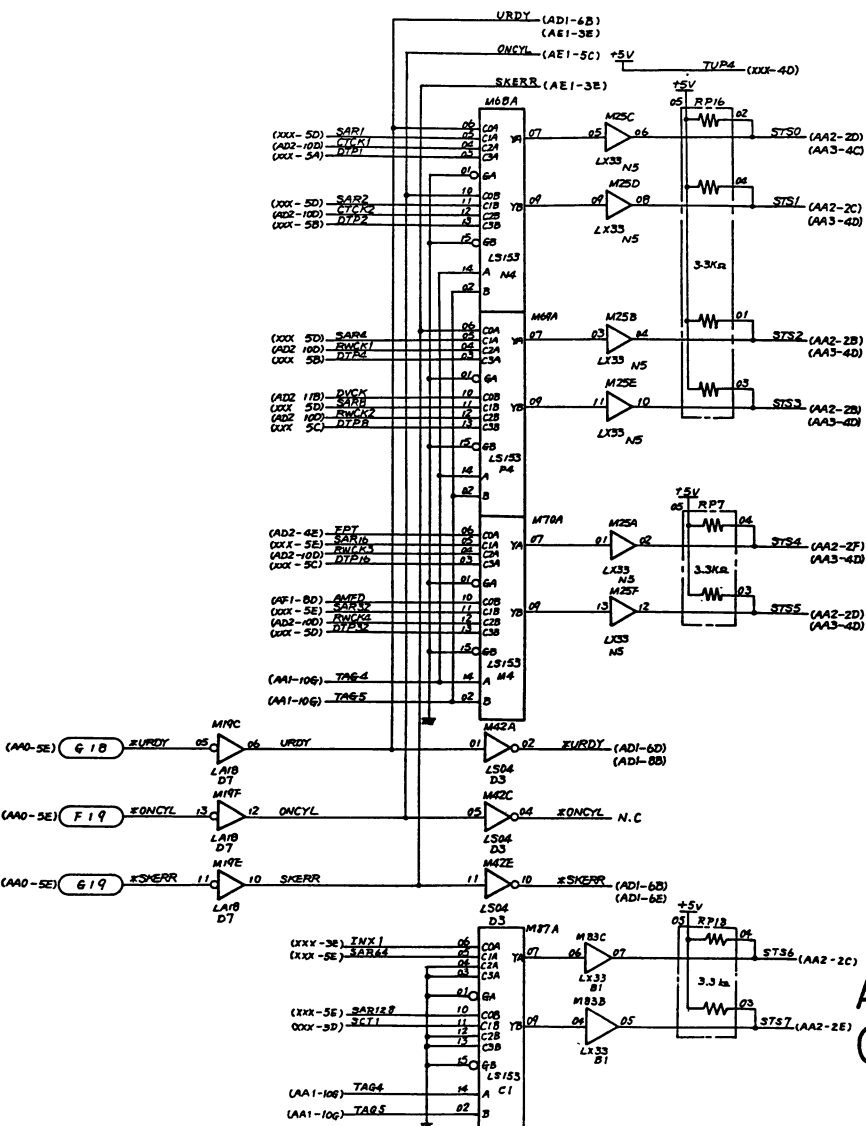
FUJITSU LIMITED 007/

FDXA-2901-3

DEVICE
TYPE
SECTOR MODE
TAG415 ENABLE



SECTOR COUNTER



STATUS MULTIPLEXER

UNIT	NAME	VALUE	DESCRIPTION
1	SECTOR ADDRESS REG.		
2	STATUS GENERATOR (1)		
3	SECTOR ADDRESS REG.		
4	STATUS GENERATOR (1)		
5	SECTOR ADDRESS REG.		
6	STATUS GENERATOR (1)		
7	SECTOR ADDRESS REG.		
8	STATUS GENERATOR (1)		
9	SECTOR ADDRESS REG.		
10	STATUS GENERATOR (1)		

FUJITSU LIMITED

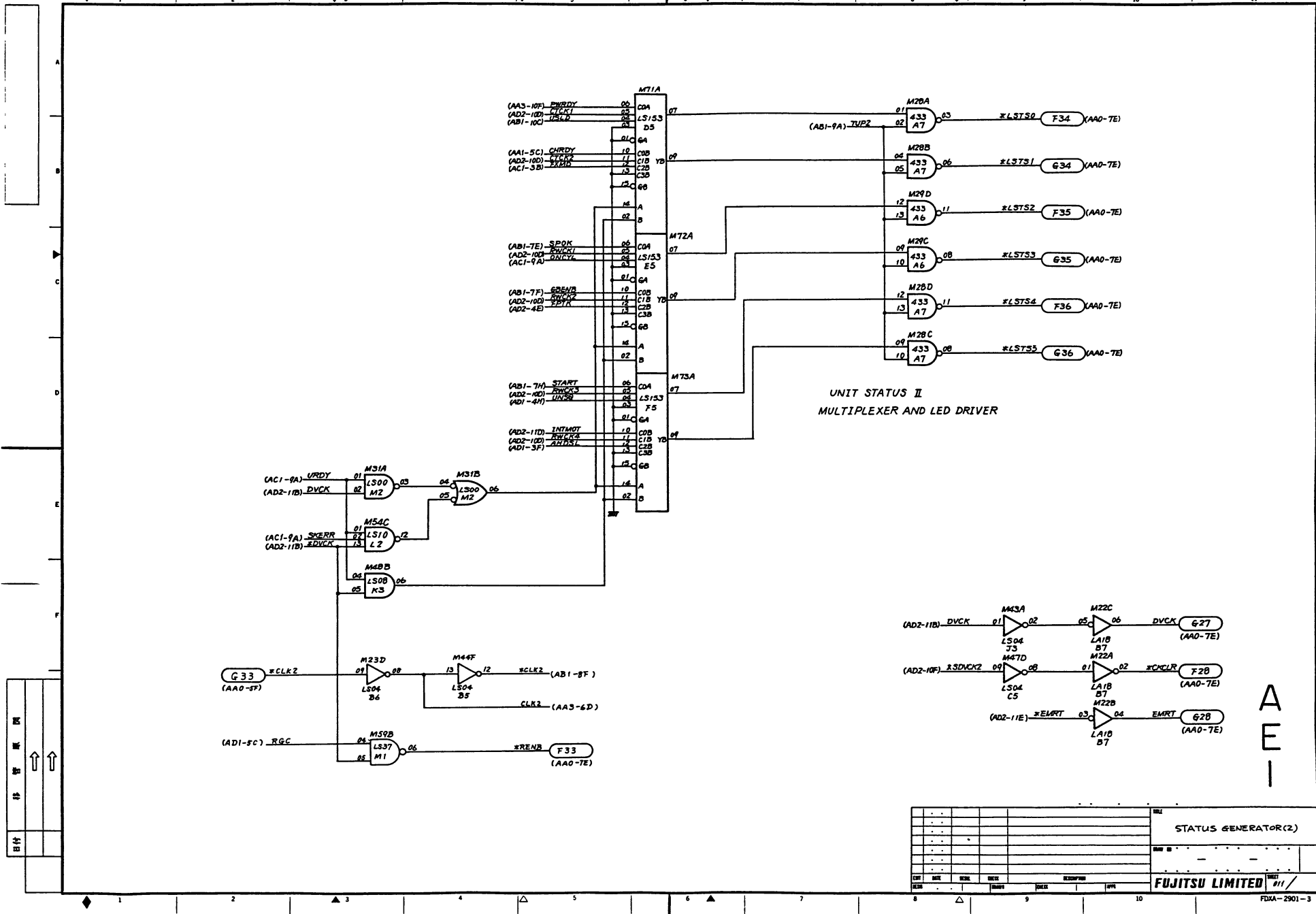
FDXA-2901-3



CONTROL CHECK DETECTOR.

FUJITSU LIMITED SHEET 009/

FDXA-2901-3

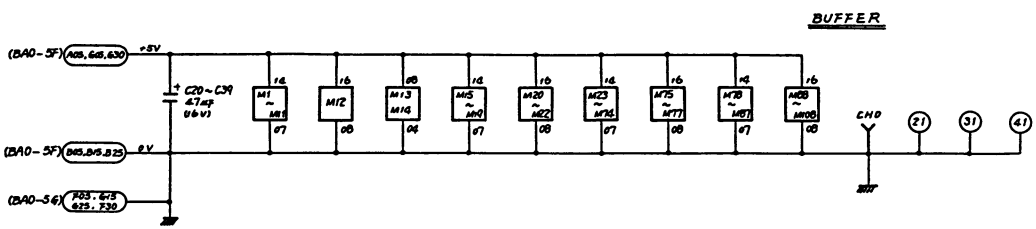
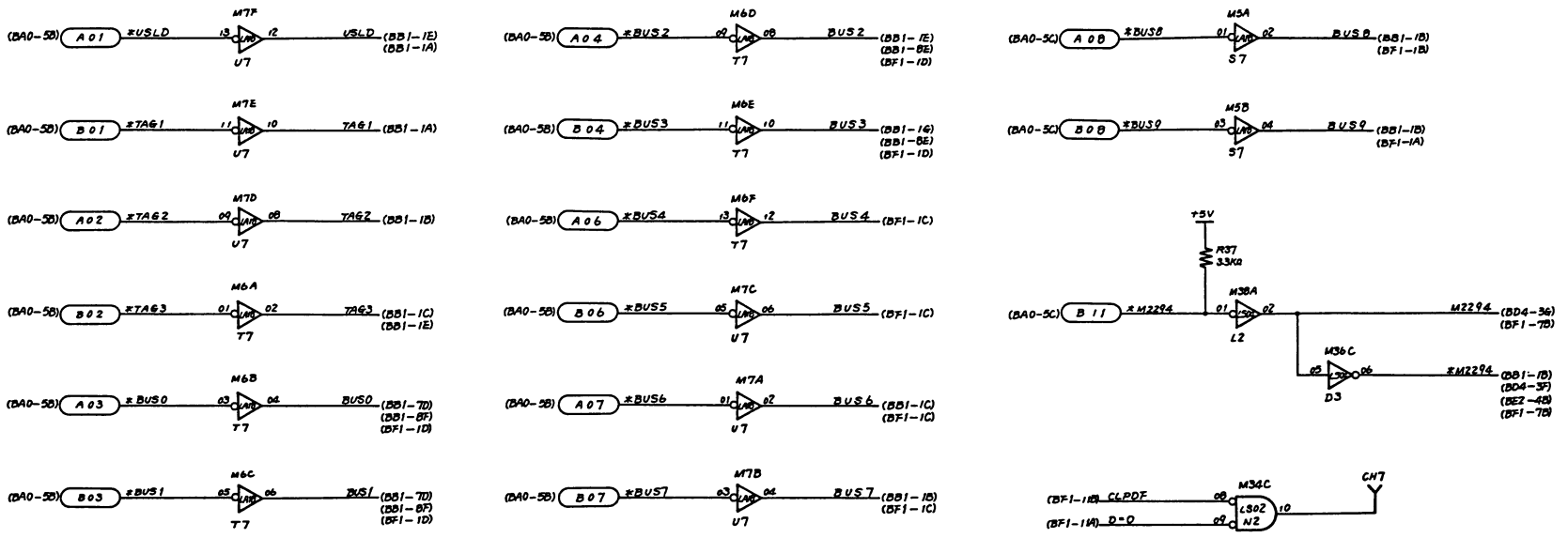


CWMM B16 B-6150-0050A

(AA0-8D)	EUGL2	A01	EUGL2	(BA1-2B)	(BD1-4F)	EATR	A1	EATR	(CA0-4C)
(AA0-8C)	EYAG1	A01	EYAG1	(BA1-3B)	(BD1-1E)	EYAG1	A1	EYAG1	(CA0-5D)
(AA0-8C)	EYAG2	A02	EYAG2	(BA1-2C)	(BD1-1E)	EYAG2	A1	EYAG2	(BA1-3D)
(AA0-8D)	EYAG3	A03	EYAG3	(BA1-2C)	(BD1-1E)	EYAG3	A1	EYAG3	(DA0-4B)
(AA0-8D)	EYAG4	A04	EYAG4	(BA1-2D)	(BD1-1F)	EYAG4	A1	EYAG4	(DA0-5F)
(AA0-8D)	EYAG5	A05	EYAG5	(BA1-2E)	(BD1-1F)	EYAG5	A1	EYAG5	(BA1-3E)
(AA0-8D)	EYAG6	A06	EYAG6	(BA1-2B)	(BD1-3C)	EYAG6	A1	EYAG6	(BA1-3E)
(AA0-8D)	EYAG7	A07	EYAG7	(BA1-3B)	(BD1-4D)	EYAG7	A1	EYAG7	(CA0-4D)
(AA0-8D)	EYAG8	A08	EYAG8	(BA1-3C)	(BD1-10B)	EYAG8	A1	EYAG8	(CA0-4D)(DA0-4C)
(AA0-8D)	EYAG9	A09	EYAG9	(BA1-3C)	(BD1-10B)	EYAG9	A1	EYAG9	(CA0-4D)
(AA0-8D)	EYAG10	A10	EYAG10	(BA1-3C)	(BD1-10B)	EYAG10	A1	EYAG10	(CA0-4D)
(AA0-8D)	EYAG11	A11	EYAG11	(BA1-3B)	(BD1-10B)	EYAG11	A1	EYAG11	(CA0-4D)
(AA0-8D)	EYAG12	A12	EYAG12	(BA1-3B)	(BD1-10B)	EYAG12	A1	EYAG12	(CA0-4D)
(AA0-8D)	EYAG13	A13	EYAG13	(BA1-3B)	(BD1-10B)	EYAG13	A1	EYAG13	(CA0-4D)
(AA0-8D)	EYAG14	A14	EYAG14	(BA1-3B)	(BD1-10B)	EYAG14	A1	EYAG14	(CA0-4D)
(AA0-8D)	EYAG15	A15	EYAG15	(BA1-3B)	(BD1-10B)	EYAG15	A1	EYAG15	(CA0-4D)
(AA0-8D)	EYAG16	A16	EYAG16	(BA1-3B)	(BD1-10B)	EYAG16	A1	EYAG16	(CA0-4D)
(AA0-8D)	EYAG17	A17	EYAG17	(BA1-3B)	(BD1-10B)	EYAG17	A1	EYAG17	(CA0-4D)
(AA0-8D)	EYAG18	A18	EYAG18	(BA1-3B)	(BD1-10B)	EYAG18	A1	EYAG18	(CA0-4D)
(AA0-8D)	EYAG19	A19	EYAG19	(BA1-3B)	(BD1-10B)	EYAG19	A1	EYAG19	(CA0-4D)
(AA0-8D)	EYAG20	A20	EYAG20	(BA1-3B)	(BD1-10B)	EYAG20	A1	EYAG20	(CA0-4D)
(AA0-8D)	EYAG21	A21	EYAG21	(BA1-3B)	(BD1-10B)	EYAG21	A1	EYAG21	(CA0-4D)
(AA0-8D)	EYAG22	A22	EYAG22	(BA1-3B)	(BD1-10B)	EYAG22	A1	EYAG22	(CA0-4D)
(AA0-8D)	EYAG23	A23	EYAG23	(BA1-3B)	(BD1-10B)	EYAG23	A1	EYAG23	(CA0-4D)
(AA0-8D)	EYAG24	A24	EYAG24	(BA1-3B)	(BD1-10B)	EYAG24	A1	EYAG24	(CA0-4D)
(AA0-8D)	EYAG25	A25	EYAG25	(BA1-3B)	(BD1-10B)	EYAG25	A1	EYAG25	(CA0-4D)
(AA0-8D)	EYAG26	A26	EYAG26	(BA1-3B)	(BD1-10B)	EYAG26	A1	EYAG26	(CA0-4D)
(AA0-8D)	EYAG27	A27	EYAG27	(BA1-3B)	(BD1-10B)	EYAG27	A1	EYAG27	(CA0-4D)
(AA0-8D)	EYAG28	A28	EYAG28	(BA1-3B)	(BD1-10B)	EYAG28	A1	EYAG28	(CA0-4D)
(AA0-8D)	EYAG29	A29	EYAG29	(BA1-3B)	(BD1-10B)	EYAG29	A1	EYAG29	(CA0-4D)
(AA0-8D)	EYAG30	A30	EYAG30	(BA1-3B)	(BD1-10B)	EYAG30	A1	EYAG30	(CA0-4D)
(AA0-8D)	EYAG31	A31	EYAG31	(BA1-3B)	(BD1-10B)	EYAG31	A1	EYAG31	(CA0-4D)
(AA0-8D)	EYAG32	A32	EYAG32	(BA1-3B)	(BD1-10B)	EYAG32	A1	EYAG32	(CA0-4D)
(AA0-8D)	EYAG33	A33	EYAG33	(BA1-3B)	(BD1-10B)	EYAG33	A1	EYAG33	(CA0-4D)
(AA0-8D)	EYAG34	A34	EYAG34	(BA1-3B)	(BD1-10B)	EYAG34	A1	EYAG34	(CA0-4D)
(AA0-8D)	EYAG35	A35	EYAG35	(BA1-3B)	(BD1-10B)	EYAG35	A1	EYAG35	(CA0-4D)
(AA0-8D)	EYAG36	A36	EYAG36	(BA1-3B)	(BD1-10B)	EYAG36	A1	EYAG36	(CA0-4D)
(AA0-8D)	EYAG37	A37	EYAG37	(BA1-3B)	(BD1-10B)	EYAG37	A1	EYAG37	(CA0-4D)
(AA0-8D)	EYAG38	A38	EYAG38	(BA1-3B)	(BD1-10B)	EYAG38	A1	EYAG38	(CA0-4D)
(AA0-8D)	EYAG39	A39	EYAG39	(BA1-3B)	(BD1-10B)	EYAG39	A1	EYAG39	(CA0-4D)
(AA0-8D)	EYAG40	A40	EYAG40	(BA1-3B)	(BD1-10B)	EYAG40	A1	EYAG40	(CA0-4D)
(AA0-8D)	EYAG41	A41	EYAG41	(BA1-3B)	(BD1-10B)	EYAG41	A1	EYAG41	(CA0-4D)
(AA0-8D)	EYAG42	A42	EYAG42	(BA1-3B)	(BD1-10B)	EYAG42	A1	EYAG42	(CA0-4D)
(AA0-8D)	EYAG43	A43	EYAG43	(BA1-3B)	(BD1-10B)	EYAG43	A1	EYAG43	(CA0-4D)
(AA0-8D)	EYAG44	A44	EYAG44	(BA1-3B)	(BD1-10B)	EYAG44	A1	EYAG44	(CA0-4D)
(AA0-8D)	EYAG45	A45	EYAG45	(BA1-3B)	(BD1-10B)	EYAG45	A1	EYAG45	(CA0-4D)
(AA0-8D)	EYAG46	A46	EYAG46	(BA1-3B)	(BD1-10B)	EYAG46	A1	EYAG46	(CA0-4D)
(AA0-8D)	EYAG47	A47	EYAG47	(BA1-3B)	(BD1-10B)	EYAG47	A1	EYAG47	(CA0-4D)
(AA0-8D)	EYAG48	A48	EYAG48	(BA1-3B)	(BD1-10B)	EYAG48	A1	EYAG48	(CA0-4D)
(AA0-8D)	EYAG49	A49	EYAG49	(BA1-3B)	(BD1-10B)	EYAG49	A1	EYAG49	(CA0-4D)
(AA0-8D)	EYAG50	A50	EYAG50	(BA1-3B)	(BD1-10B)	EYAG50	A1	EYAG50	(CA0-4D)
(AA0-8D)	EYAG51	A51	EYAG51	(BA1-3B)	(BD1-10B)	EYAG51	A1	EYAG51	(CA0-4D)
(AA0-8D)	EYAG52	A52	EYAG52	(BA1-3B)	(BD1-10B)	EYAG52	A1	EYAG52	(CA0-4D)
(AA0-8D)	EYAG53	A53	EYAG53	(BA1-3B)	(BD1-10B)	EYAG53	A1	EYAG53	(CA0-4D)
(AA0-8D)	EYAG54	A54	EYAG54	(BA1-3B)	(BD1-10B)	EYAG54	A1	EYAG54	(CA0-4D)
(AA0-8D)	EYAG55	A55	EYAG55	(BA1-3B)	(BD1-10B)	EYAG55	A1	EYAG55	(CA0-4D)
(AA0-8D)	EYAG56	A56	EYAG56	(BA1-3B)	(BD1-10B)	EYAG56	A1	EYAG56	(CA0-4D)
(AA0-8D)	EYAG57	A57	EYAG57	(BA1-3B)	(BD1-10B)	EYAG57	A1	EYAG57	(CA0-4D)
(AA0-8D)	EYAG58	A58	EYAG58	(BA1-3B)	(BD1-10B)	EYAG58	A1	EYAG58	(CA0-4D)
(AA0-8D)	EYAG59	A59	EYAG59	(BA1-3B)	(BD1-10B)	EYAG59	A1	EYAG59	(CA0-4D)
(AA0-8D)	EYAG60	A60	EYAG60	(BA1-3B)	(BD1-10B)	EYAG60	A1	EYAG60	(CA0-4D)
(AA0-8D)	EYAG61	A61	EYAG61	(BA1-3B)	(BD1-10B)	EYAG61	A1	EYAG61	(CA0-4D)
(AA0-8D)	EYAG62	A62	EYAG62	(BA1-3B)	(BD1-10B)	EYAG62	A1	EYAG62	(CA0-4D)
(AA0-8D)	EYAG63	A63	EYAG63	(BA1-3B)	(BD1-10B)	EYAG63	A1	EYAG63	(CA0-4D)
(AA0-8D)	EYAG64	A64	EYAG64	(BA1-3B)	(BD1-10B)	EYAG64	A1	EYAG64	(CA0-4D)
(AA0-8D)	EYAG65	A65	EYAG65	(BA1-3B)	(BD1-10B)	EYAG65	A1	EYAG65	(CA0-4D)
(AA0-8D)	EYAG66	A66	EYAG66	(BA1-3B)	(BD1-10B)	EYAG66	A1	EYAG66	(CA0-4D)
(AA0-8D)	EYAG67	A67	EYAG67	(BA1-3B)	(BD1-10B)	EYAG67	A1	EYAG67	(CA0-4D)
(AA0-8D)	EYAG68	A68	EYAG68	(BA1-3B)	(BD1-10B)	EYAG68	A1	EYAG68	(CA0-4D)
(AA0-8D)	EYAG69	A69	EYAG69	(BA1-3B)	(BD1-10B)	EYAG69	A1	EYAG69	(CA0-4D)
(AA0-8D)	EYAG70	A70	EYAG70	(BA1-3B)	(BD1-10B)	EYAG70	A1	EYAG70	(CA0-4D)
(AA0-8D)	EYAG71	A71	EYAG71	(BA1-3B)	(BD1-10B)	EYAG71	A1	EYAG71	(CA0-4D)
(AA0-8D)	EYAG72	A72	EYAG72	(BA1-3B)	(BD1-10B)	EYAG72	A1	EYAG72	(CA0-4D)
(AA0-8D)	EYAG73	A73	EYAG73	(BA1-3B)	(BD1-10B)	EYAG73	A1	EYAG73	(CA0-4D)
(AA0-8D)	EYAG74	A74	EYAG74	(BA1-3B)	(BD1-10B)	EYAG74	A1	EYAG74	(CA0-4D)
(AA0-8D)	EYAG75	A75	EYAG75	(BA1-3B)	(BD1-10B)	EYAG75	A1	EYAG75	(CA0-4D)
(AA0-8D)	EYAG76	A76	EYAG76	(BA1-3B)	(BD1-10B)	EYAG76	A1	EYAG76	(CA0-4D)
(AA0-8D)	EYAG77	A77	EYAG77	(BA1-3B)	(BD1-10B)	EYAG77	A1	EYAG77	(CA0-4D)
(AA0-8D)	EYAG78	A78	EYAG78	(BA1-3B)	(BD1-10B)	EYAG78	A1	EYAG78	(CA0-4D)
(AA0-8D)	EYAG79	A79	EYAG79	(BA1-3B)	(BD1-10B)	EYAG79	A1	EYAG79	(CA0-4D)
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(AA0-8D)	EYAG82	A82	EYAG82	(BA1-3B)	(BD1-10B)	EYAG82	A1	EYAG82	(CA0-4D)
(AA0-8D)	EYAG83	A83	EYAG83	(BA1-3B)	(BD1-10B)	EYAG83	A1	EYAG83	(CA0-4D)
(AA0-8D)	EYAG84	A84	EYAG84	(BA1-3B)	(BD1-10B)	EYAG84	A1	EYAG84	(CA0-4D)
(AA0-8D)	EYAG85	A85	EYAG85	(BA1-3B)	(BD1-10B)	EYAG85	A1	EYAG85	(CA0-4D)
(AA0-8D)	EYAG86	A86	EYAG86	(BA1-3B)	(BD1-10B)	EYAG86	A1	EYAG86	(CA0-4D)
(AA0-8D)	EYAG87	A87	EYAG87	(BA1-3B)	(BD1-10B)	EYAG87	A1	EYAG87	(CA0-4D)
(AA0-8D)	EYAG88	A88	EYAG88	(BA1-3B)	(BD1-10B)	EYAG88	A1	EYAG88	(CA0-4D)
(AA0-8D)	EYAG89	A89	EYAG89	(BA1-3B)	(BD1-10B)	EYAG89	A1	EYAG89	(CA0-4D)
(AA0-8D)	EYAG90	A90	EYAG90	(BA1-3B)	(BD1-10B)	EYAG90	A1	EYAG90	(CA0-4D)
(AA0-8D)	EYAG91	A91	EYAG91	(BA1-3B)	(BD1-10B)	EYAG91	A1	EYAG91	(CA0-4D)
(AA0-8D)	EYAG92	A92	EYAG92	(BA1-3B)	(BD1-10B)	EYAG92	A1	EYAG92	(CA0-4D)
(AA0-8D)	EYAG93	A93	EYAG93	(BA1-3B)	(BD1-10B)	EYAG93	A1	EYAG93	(CA0-4D)
(AA0-8D)	EYAG94	A94	EYAG94	(BA1-3B)	(BD1-10B)	EYAG94	A1	EYAG94	(CA0-4D)
(AA0-8D)	EYAG95	A95	EYAG95	(BA1-3B)	(BD1-10B)	EYAG95	A1	EYAG95	(CA0-4D)
(AA0-8D)	EYAG96	A96	EYAG96	(BA1-3B)	(BD1-10B)	EYAG96	A1	EYAG96	(CA0-4D)
(AA0-8D)	EYAG97	A97	EYAG97	(BA1-3B)	(BD1-10B)	EYAG97	A1	EYAG97	(CA0-4D)
(AA0-8D)	EYAG98	A98	EYAG98	(BA1-3B)	(BD1-10B)	EYAG98	A1	EYAG98	(CA0-4D)
(AA0-8D)	EYAG99	A99	EYAG99	(BA1-3B)	(BD1-10B)	EYAG99	A1	EYAG99	(CA0-4D)
(AA0-8D)	EYAG100	A100	EYAG100	(BA1-3B)	(BD1-10B)	EYAG100	A1	EYAG100	(CA0-4D)
(AA0-8D)	EYAG101	A101	EYAG101	(BA1-3B)	(BD1-10B)	EYAG101	A1	EYAG101	(CA0-4D)
(AA0-8D)	EYAG102	A102	EYAG102	(BA1-3B)	(BD1-10B)	EYAG102	A1	EYAG102	(CA0-4D)
(AA0-8D)	EYAG103	A103	EYAG103	(BA1-3B)	(BD1-10B)	EYAG103	A1	EYAG103	(CA0-4D)
(AA0-8D)	EYAG104	A104	EYAG104	(BA1-3B)	(BD1-10B)	EYAG104	A1	EYAG104	(CA0-4D)
(AA0-8D)	EYAG105	A105	EYAG105	(BA1-3B)	(BD1-10B)	EYAG105	A1	EYAG105	(CA0-4D)
(AA0-8D)	EYAG106	A106	EYAG106	(BA1-3B)	(BD1-10B)	EYAG106	A1	EYAG106	(CA0-4D)
(AA0-8D)	EYAG107	A107	EYAG107	(BA1-3B)	(BD1-10B)	EYAG107	A1	EYAG107	(CA0-4D)
(AA0-8D)	EYAG108	A108	EYAG108	(BA1-3B)	(BD1-10B)	EYAG108	A1	EYAG108	(CA0-4D)
(AA0-8D)	EYAG109	A109	EYAG109	(BA1-3B)	(BD1-10B)	EYAG109	A1	EYAG109	(CA0-4D)
(AA0-8D)	EYAG110	A110	EYAG110	(BA1-3B)	(BD1-10B)	EYAG110	A1	EYAG110	(CA0-4D)
(AA0-8D)	EYAG111	A111	EYAG111	(BA1-3B)	(BD1-10B)	EYAG111	A1	EYAG111	(CA0-4D)
(AA0-8D)	EYAG112	A112	EYAG112	(BA1-3B)	(BD1-10B)	EYAG112	A1	EYAG112	(CA0-4D)
(AA0-8D)	EYAG113	A113	EYAG113	(BA1-3B)	(BD1-10B)	EYAG113	A1	EYAG113	(CA0-4D)
(AA0-8D)	EYAG114	A114	EYAG114	(BA1-3B)	(BD1-10B)	EYAG114	A1	EYAG114	(CA0-4D)
(AA0-8D)	EYAG115	A115	EYAG115	(BA1-3B)	(BD1-10B)	EYAG115	A1	EYAG115	(CA0-4D)
(AA0-8D)	EYAG116	A116	EYAG116	(BA1-3B)	(BD1-10B)	EYAG116	A1	EYAG116	(CA0-4D)
(AA0-8D)	EYAG117	A117	EYAG117	(BA1-3B)	(BD1-10B)	EYAG117	A1	EYAG117	(CA0-4D)
(AA0-8D)	EYAG118	A118	EYAG118	(BA1-3B)	(BD1-10B)	EYAG118	A1	EYAG118	(CA0-4D)
(AA0-8D)	EYAG119	A119	EYAG119	(BA1-3B)	(BD1-10B)	EYAG119	A1	EYAG119	(CA0-4D)
(AA0-8D)	EYAG120	A120	EYAG120	(BA1-3B)	(BD1-10B)	EYAG120	A1	EYAG120	(CA0-4D)
(AA0-8D)	EYAG121	A121	EYAG121	(BA1-3B)	(BD1-10B)	EYAG121	A1	EYAG121	(CA0-4D)
(AA0-8D)	EYAG122	A122	EYAG122	(BA1-3B)	(BD1-10B)	EYAG122	A1	EYAG122	(CA0-4D)
(AA0-8D)	EYAG123	A123	EYAG123	(BA1-3B)	(BD1-10B)	EYAG123	A1	EYAG123	(CA0-4D)
(AA0-8D)	EYAG124	A124	EYAG124	(BA1-3B)	(BD1-10B)	EYAG124	A1	EYAG124	(CA0-4D)
(AA0-8D)	EYAG125	A125	EYAG125	(BA1-3B)	(BD1-10B)	EYAG125	A1	EYAG125	(CA0-4D)
(AA0-8D)	EYAG126	A126	EYAG126	(BA1-3B)	(BD1-10B)	EYAG126	A1	EYAG126	(CA0-4D)
(AA0-8D)	EYAG127	A127</							

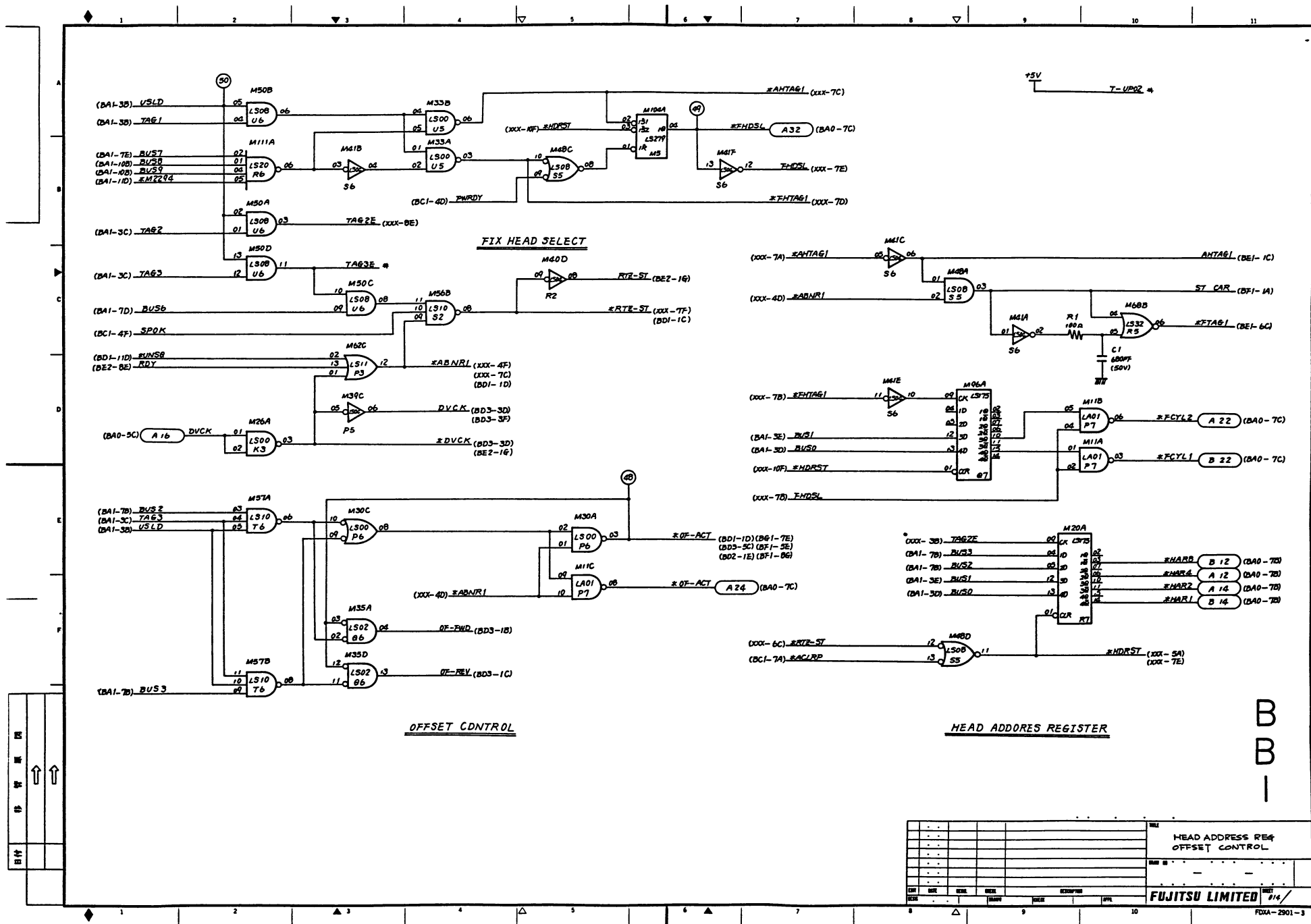
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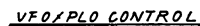
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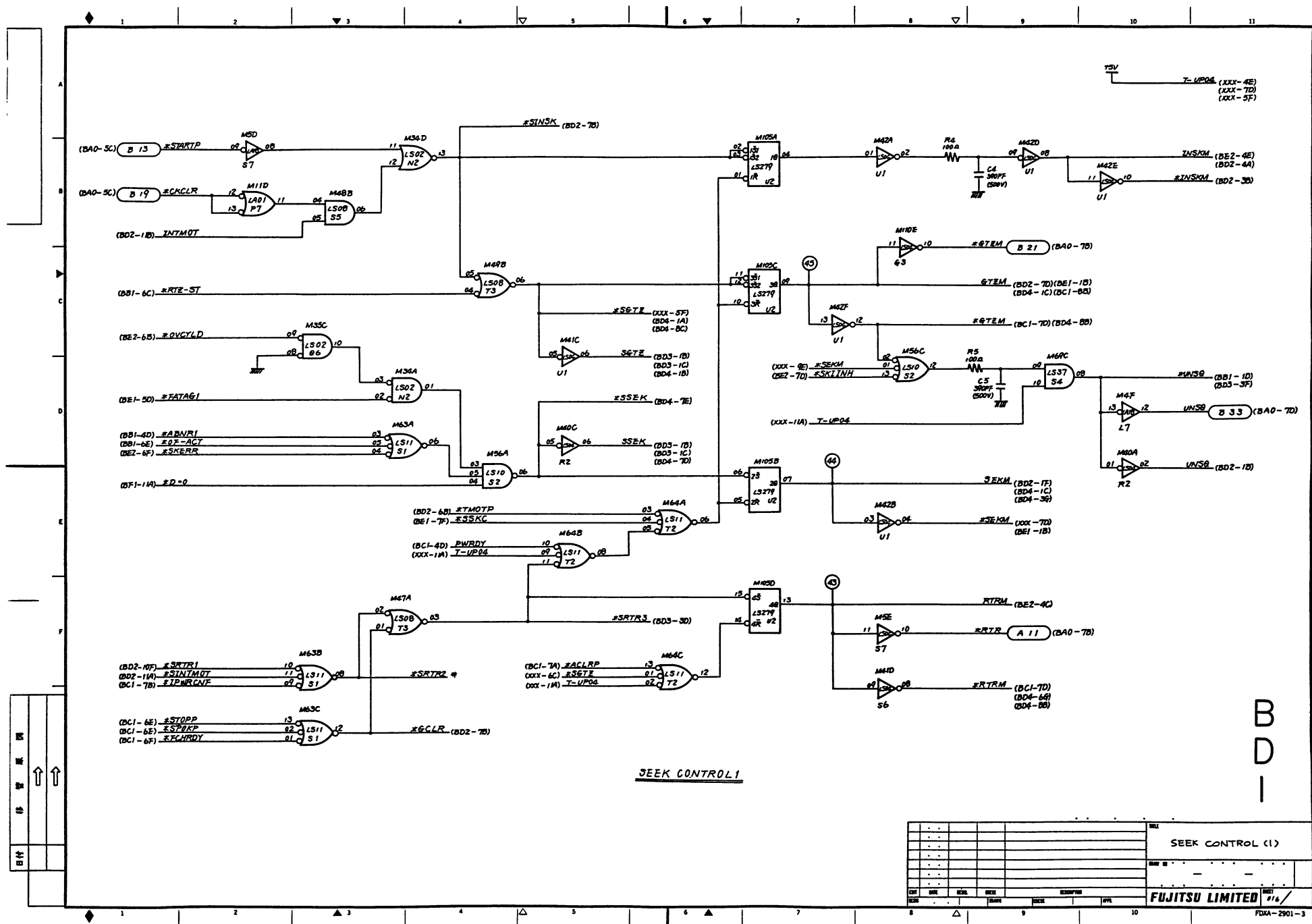
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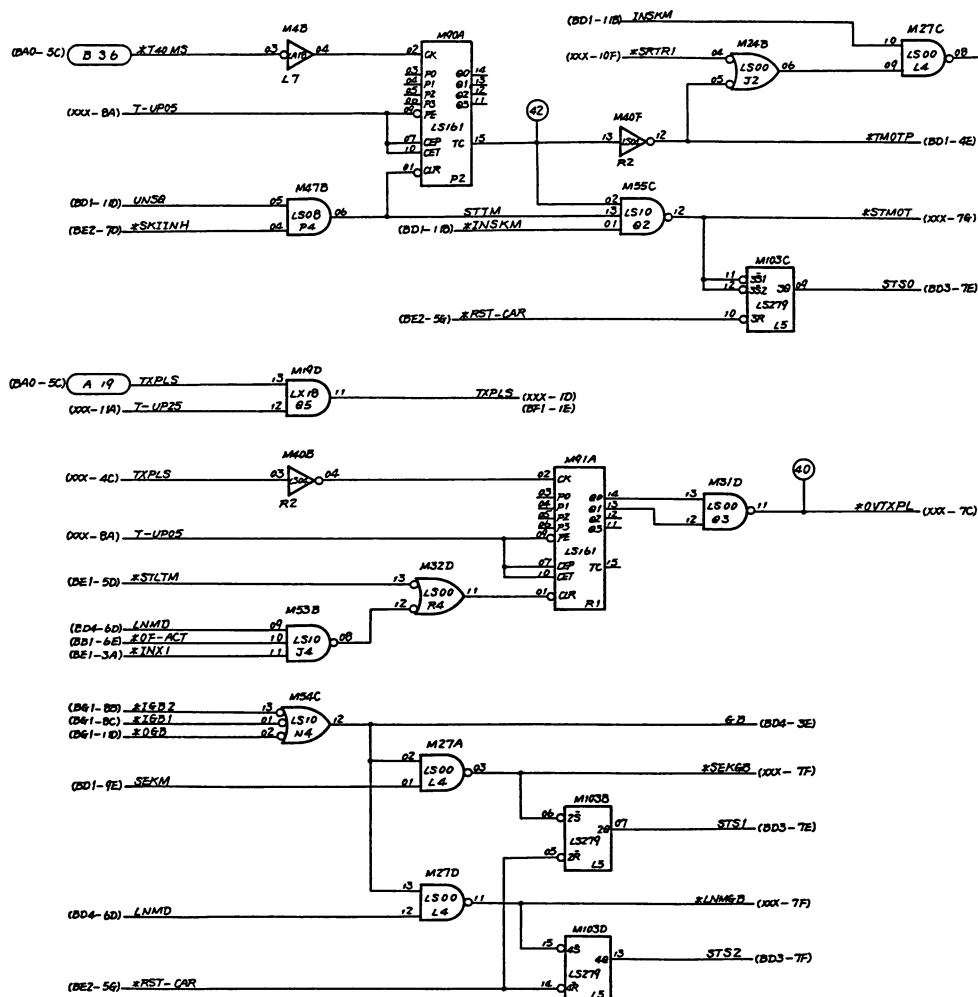


ECI

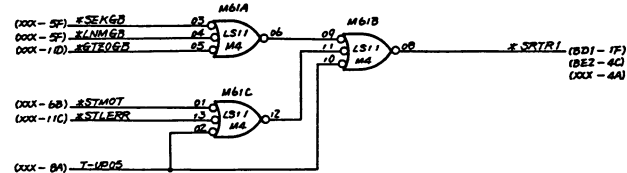
FDXA-2901-1



SEEK CONTROL 2



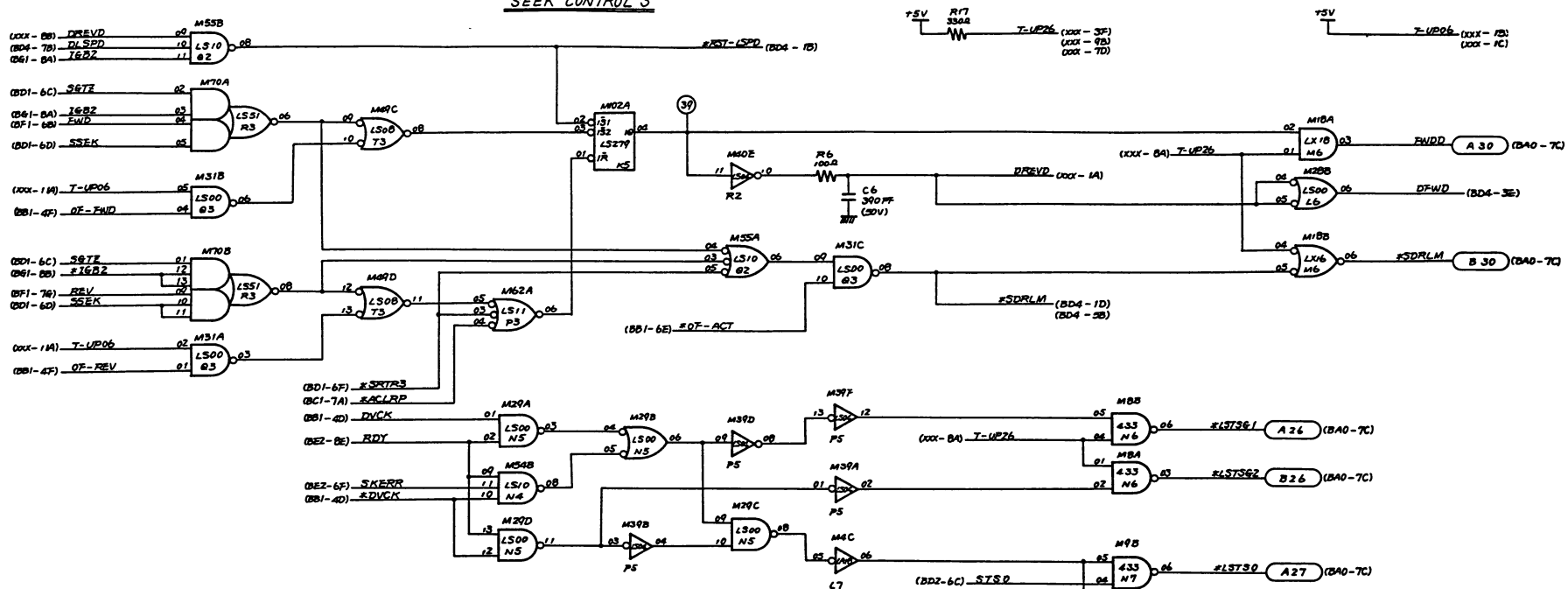
SEEK ERROR LATCH



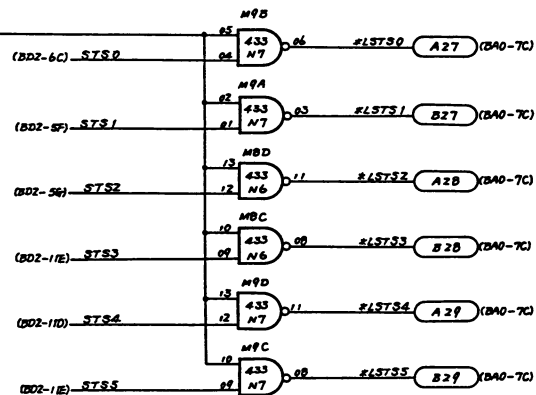
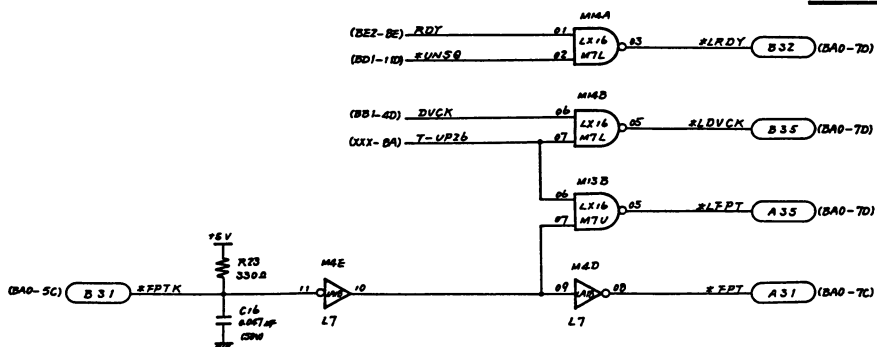
BD 2

SEEK CONTROL(2) SEEK ERROR LATCH									
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FUJITSU LIMITED

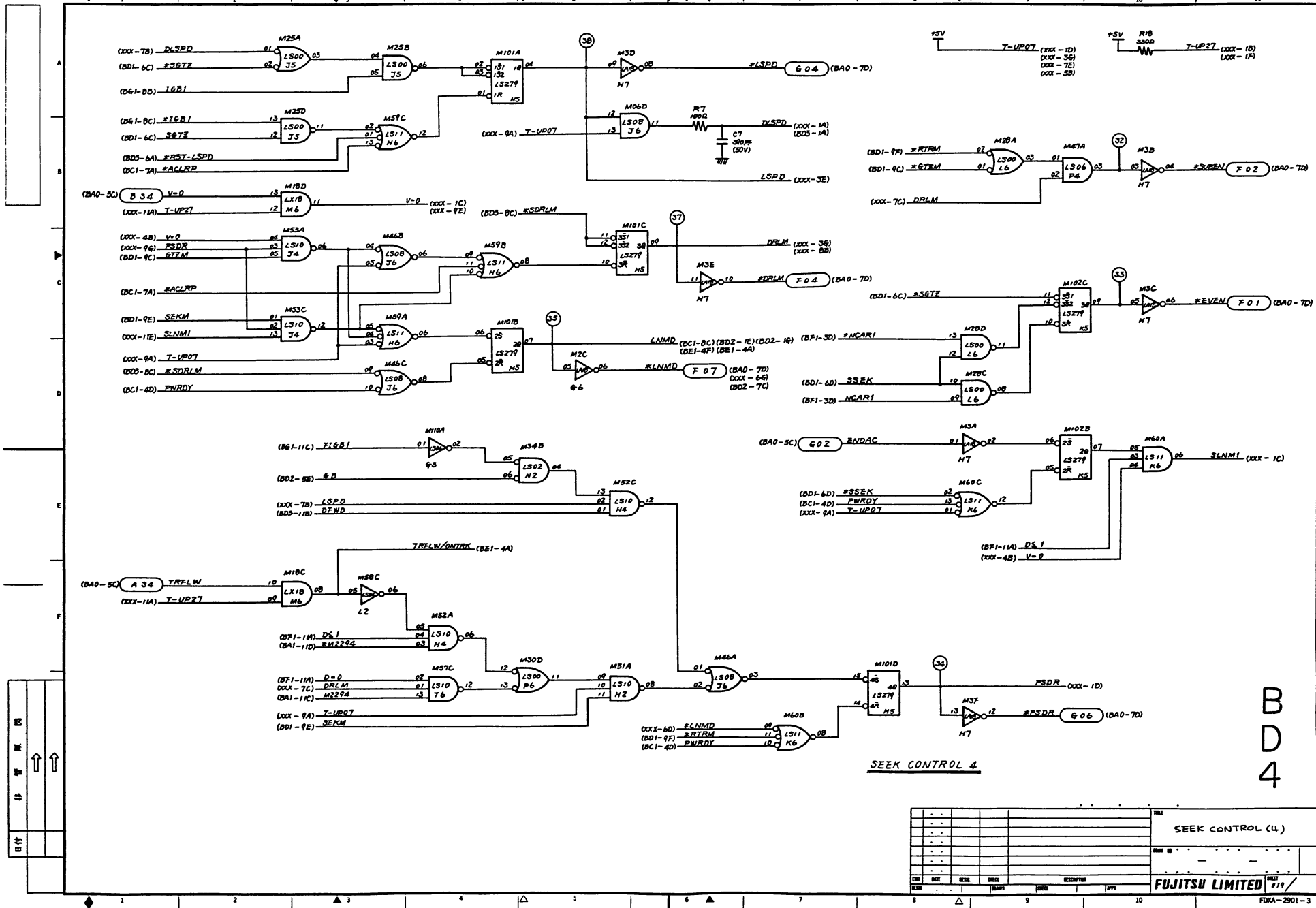


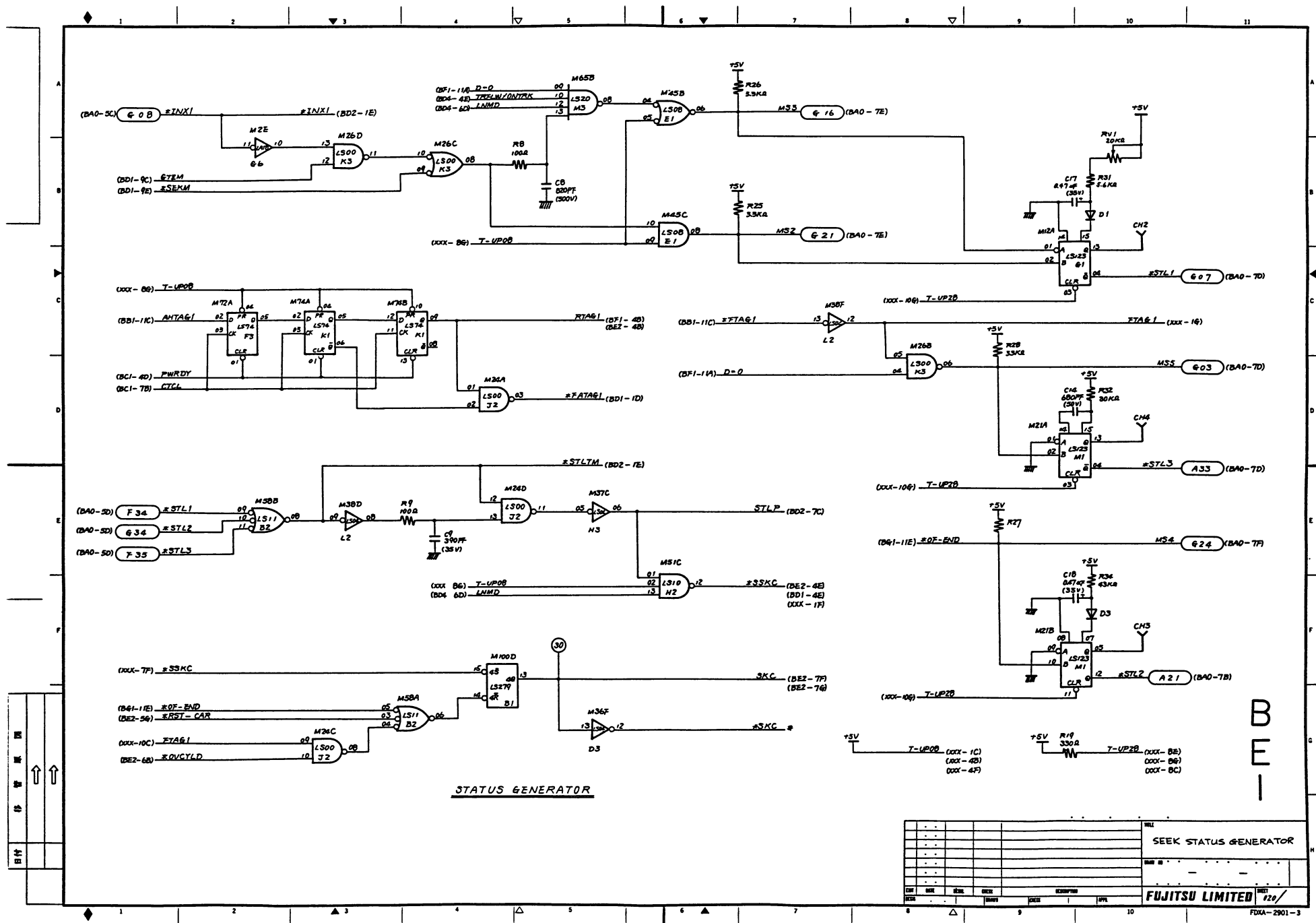
LED DRIVER

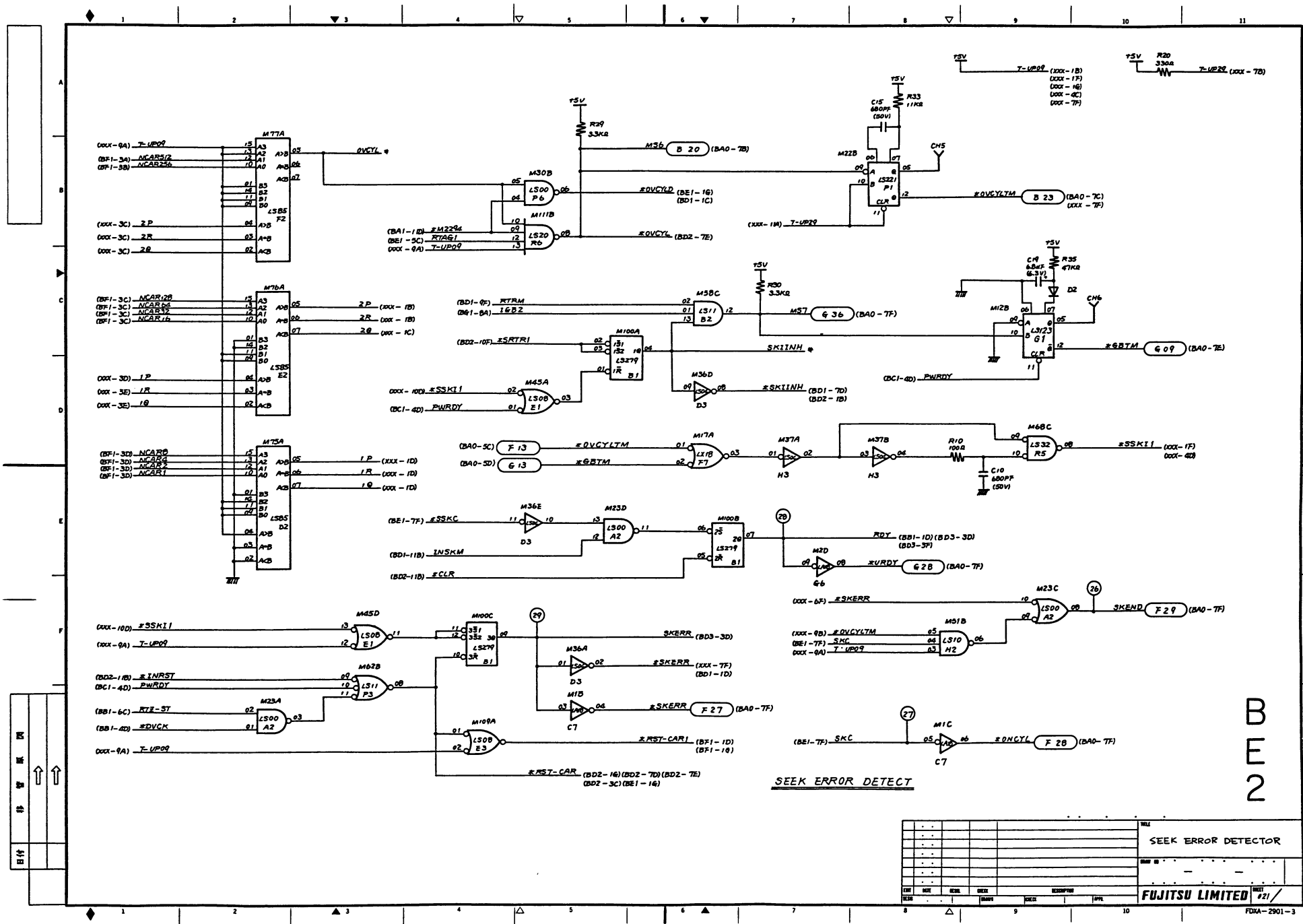


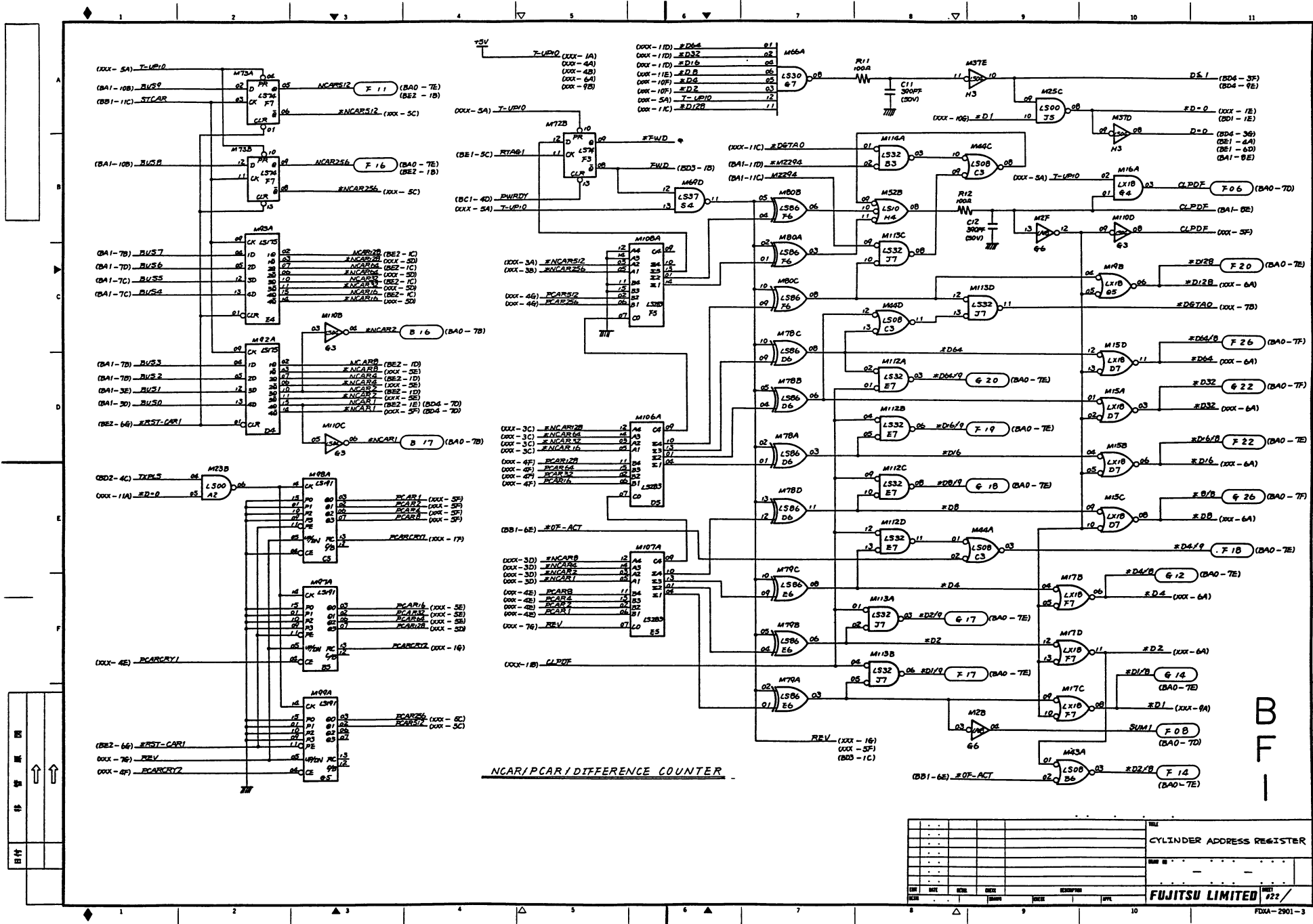
EDC

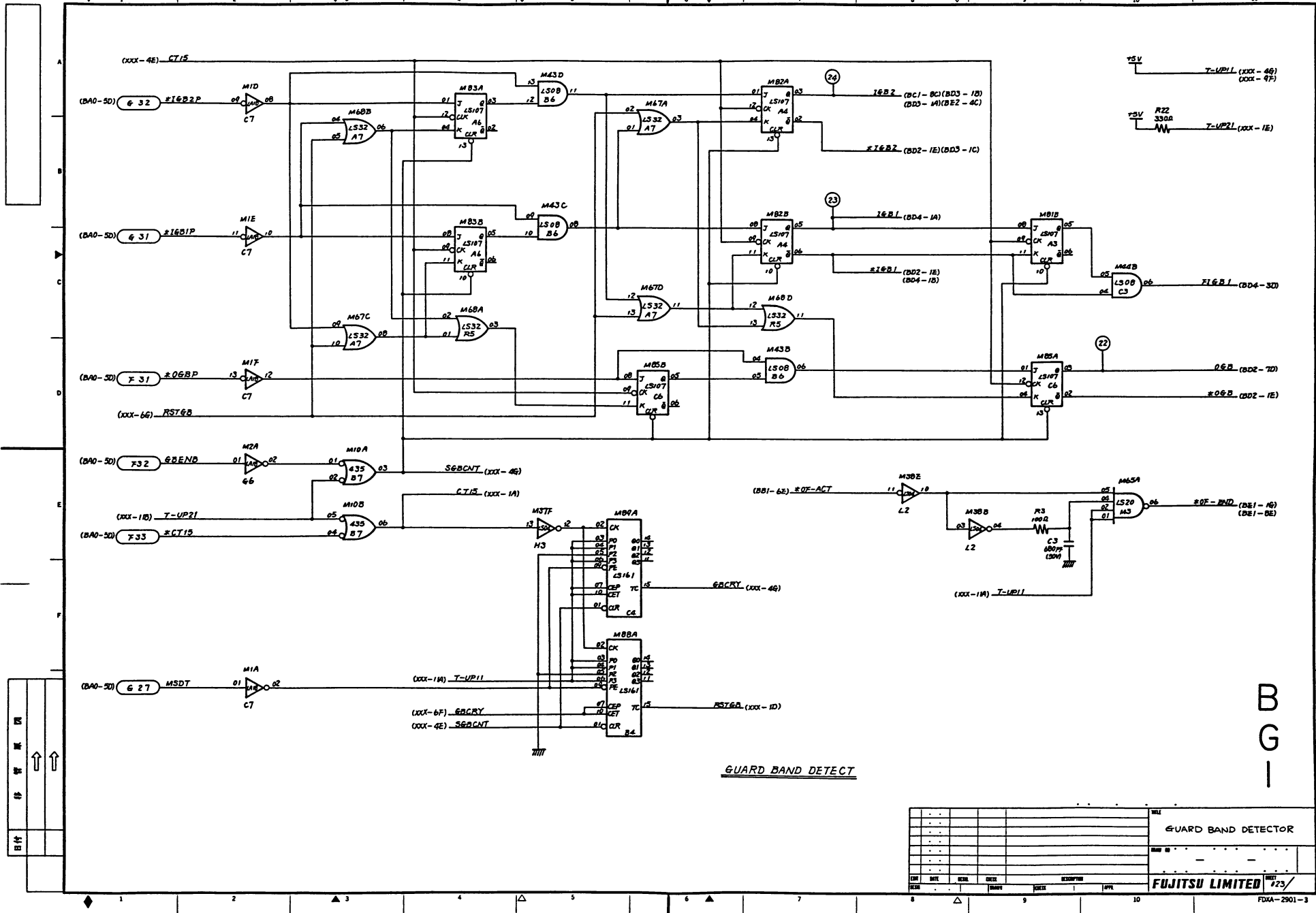
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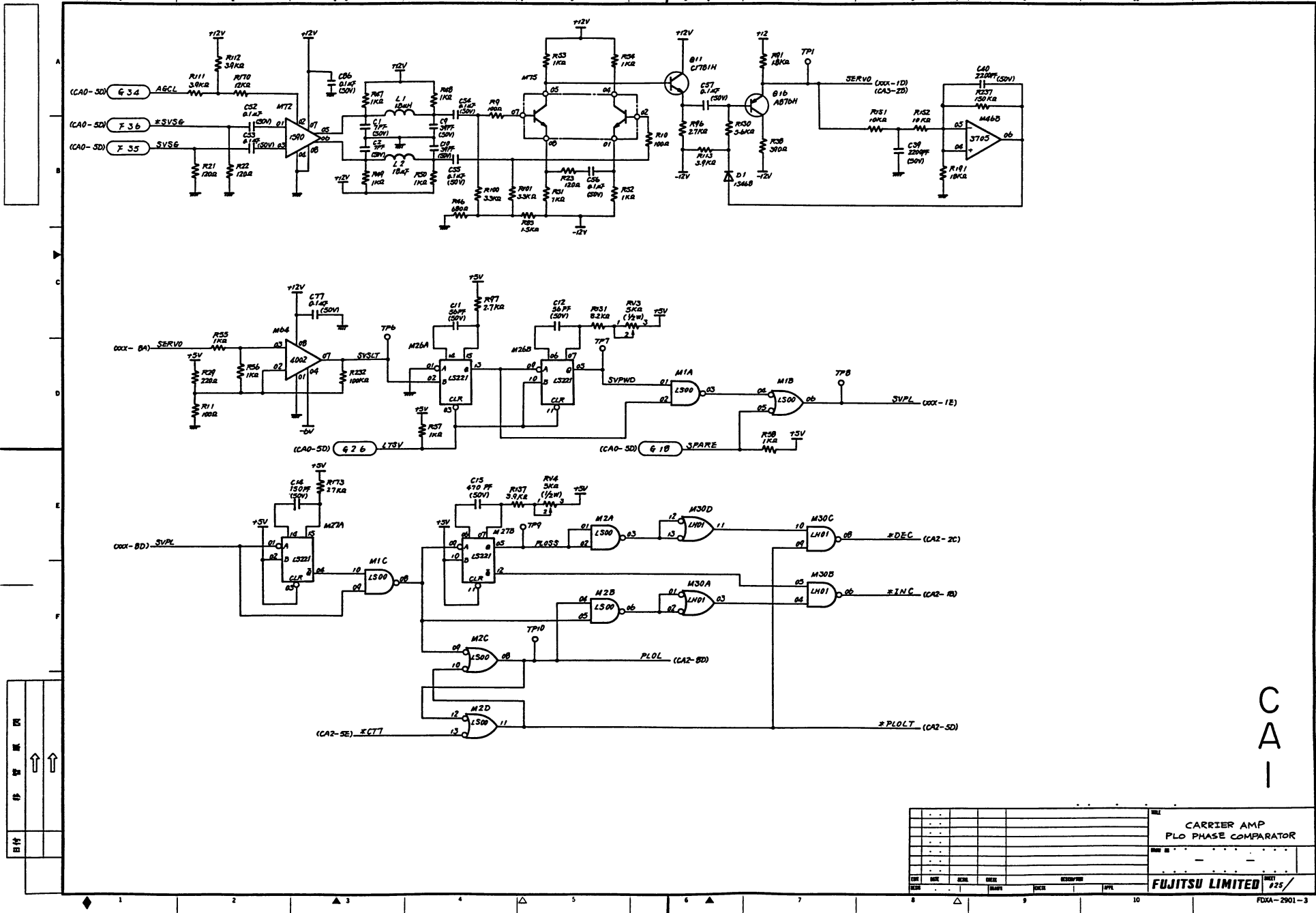




[illegible][illegible][illegible]

CAO

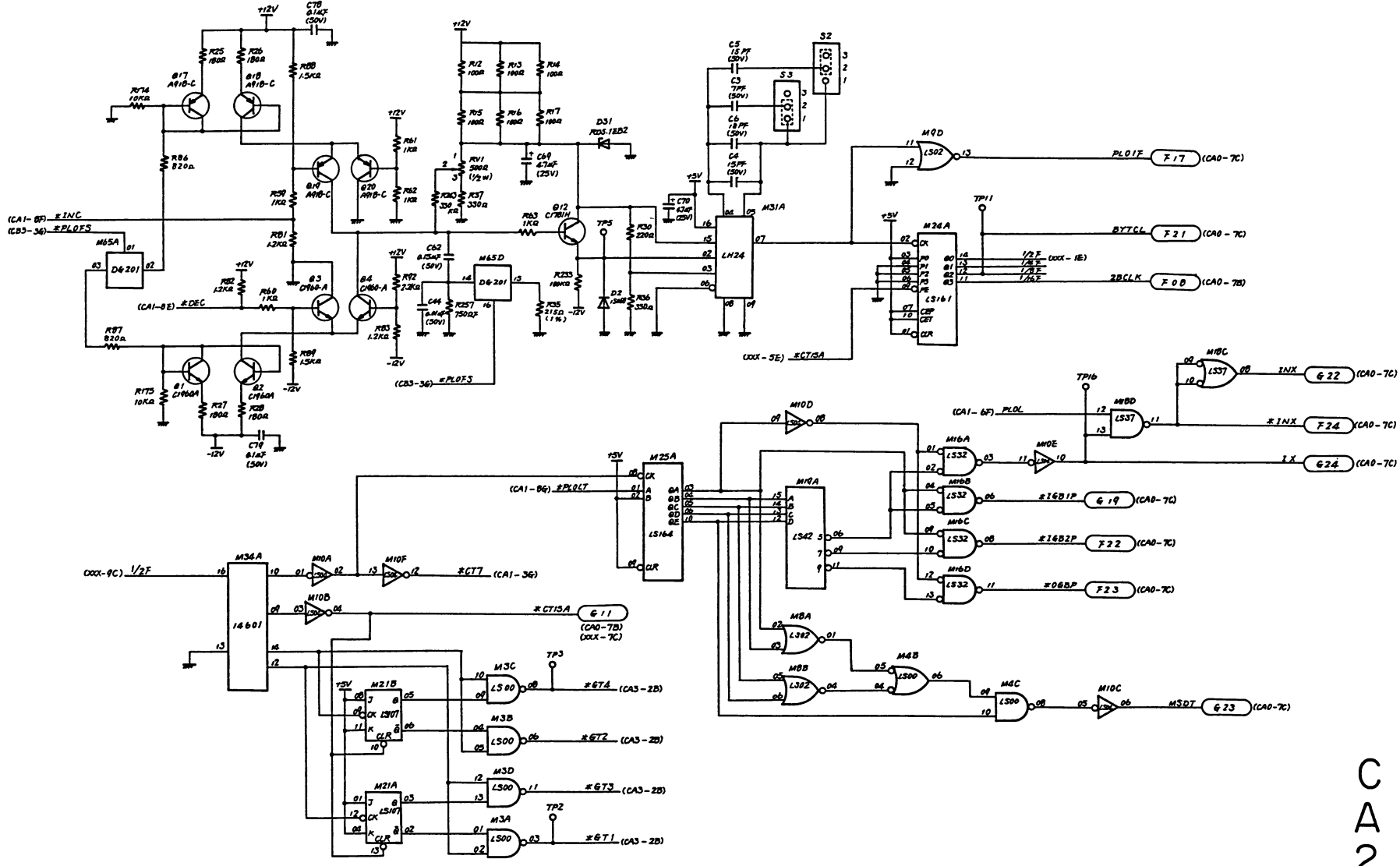
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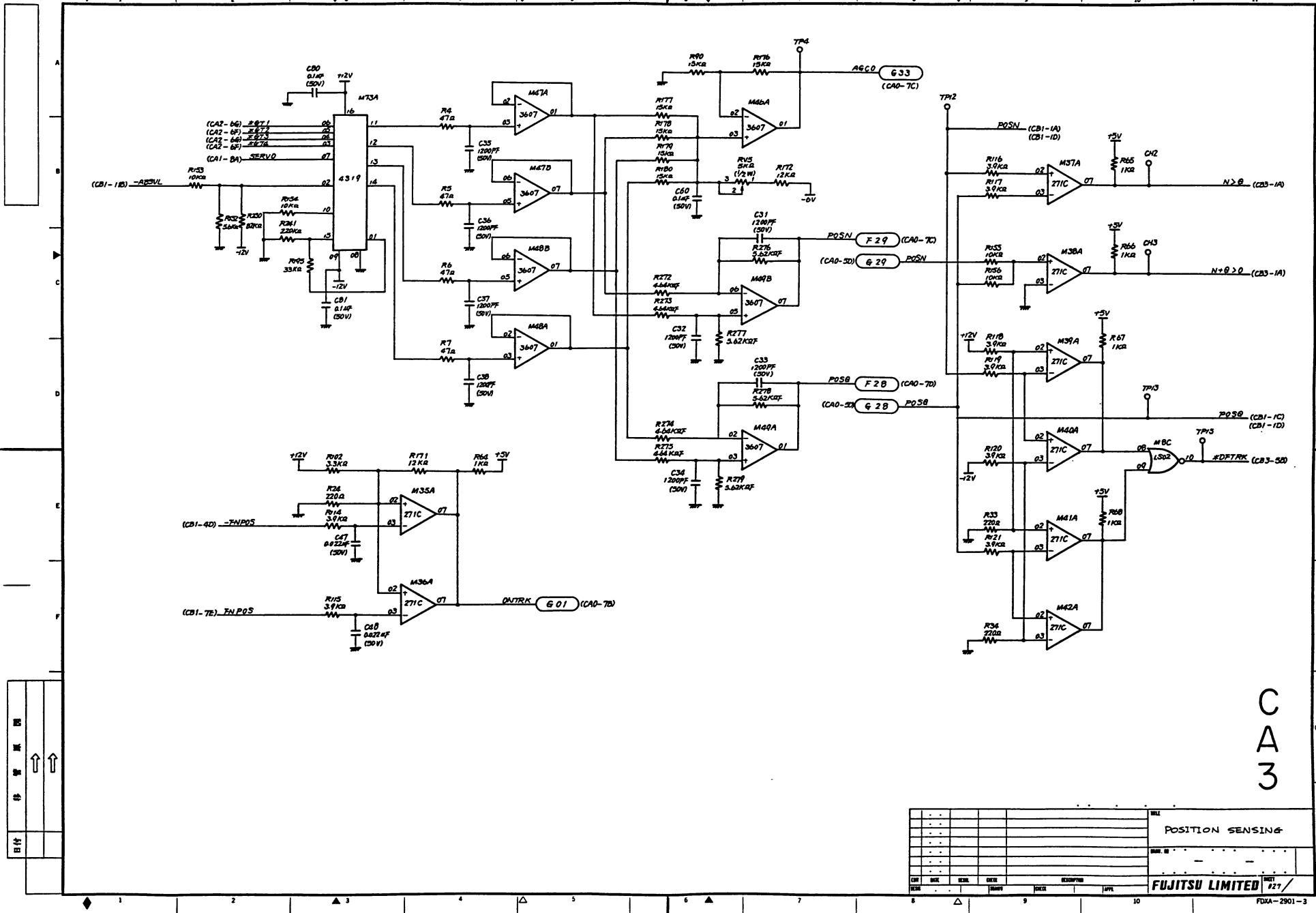
CA2



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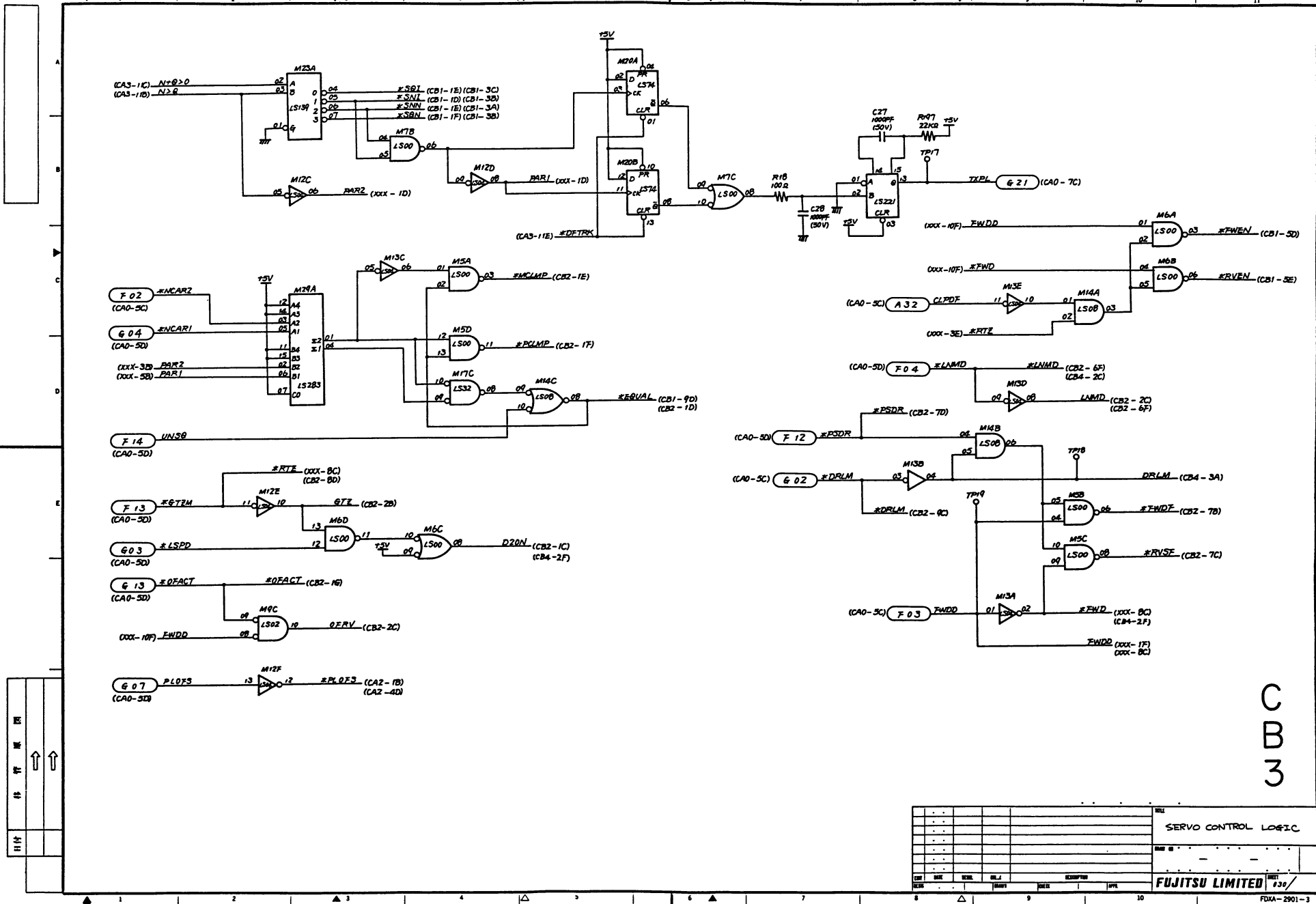
FUJITSU LIMITED

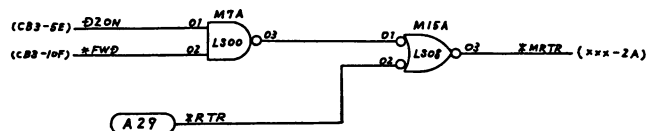
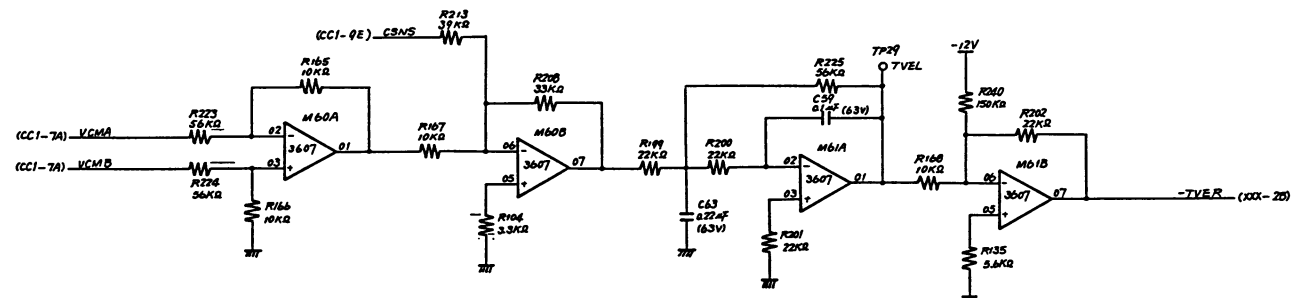
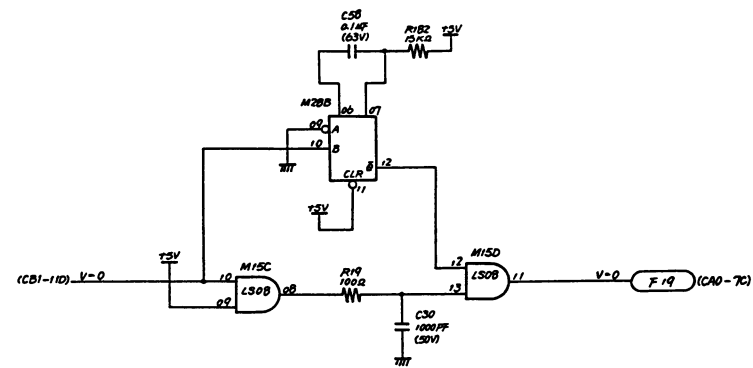
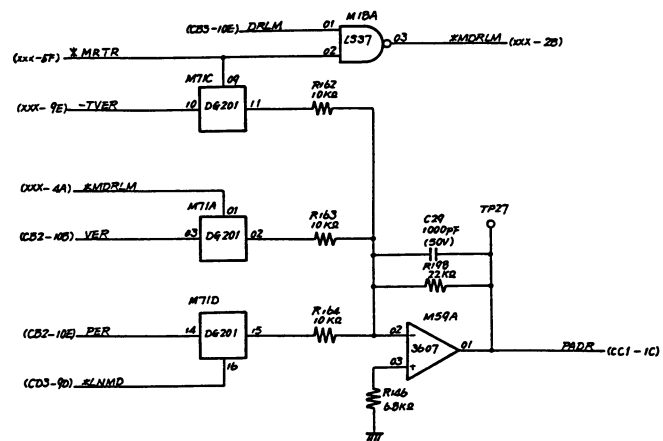
FDXA-2901-3





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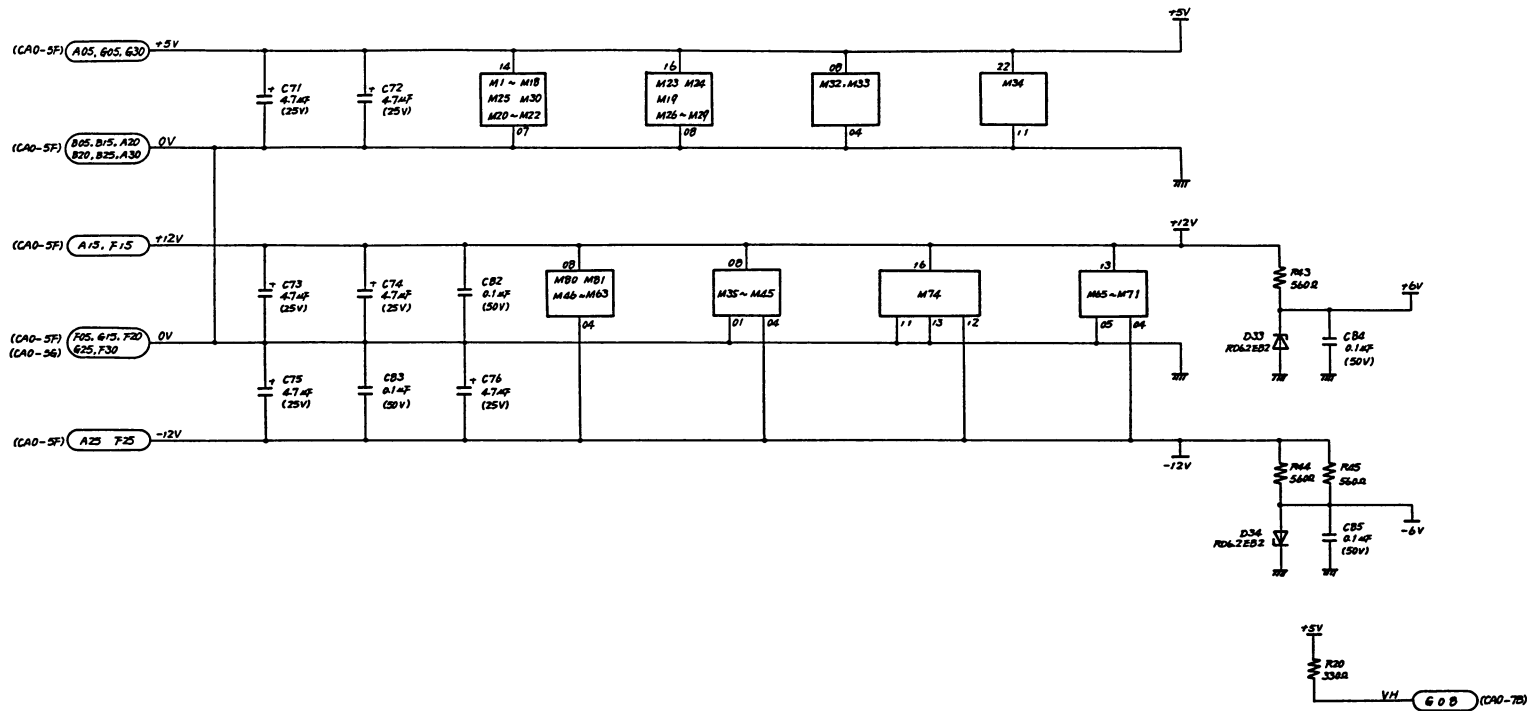
POWER DRIVE MPX

FUJITSU LIMITED

FDXA-2901-3



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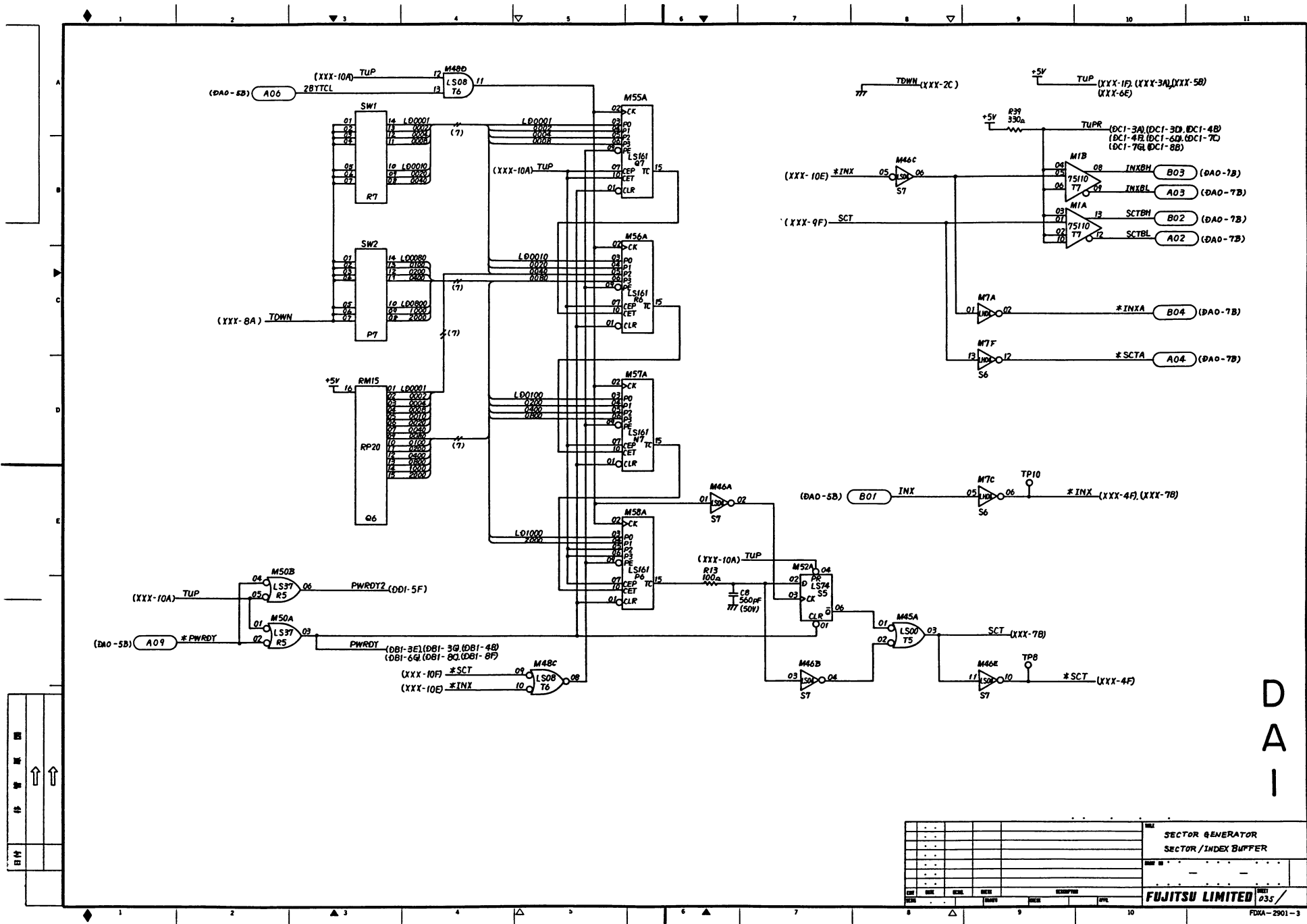
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DATE	REV	NO.	REV	DESCRIPTION	DATE	REV	DESCRIPTION
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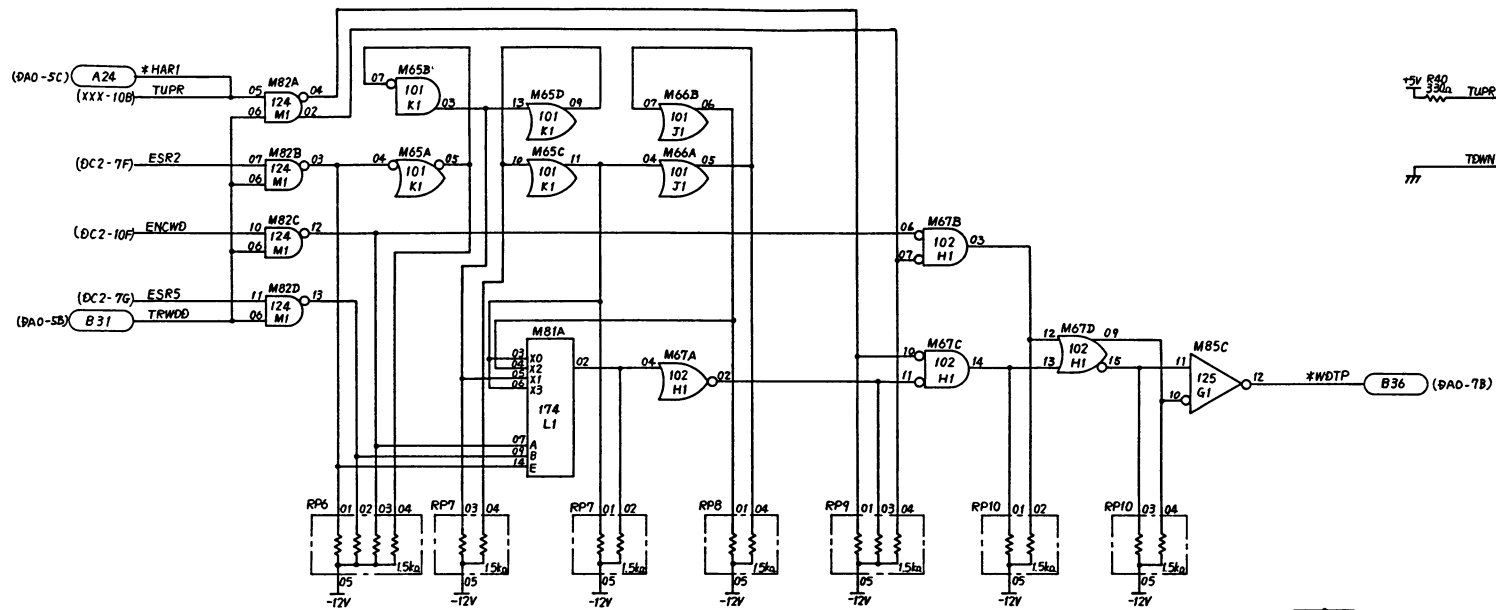


FDXA-2901-3

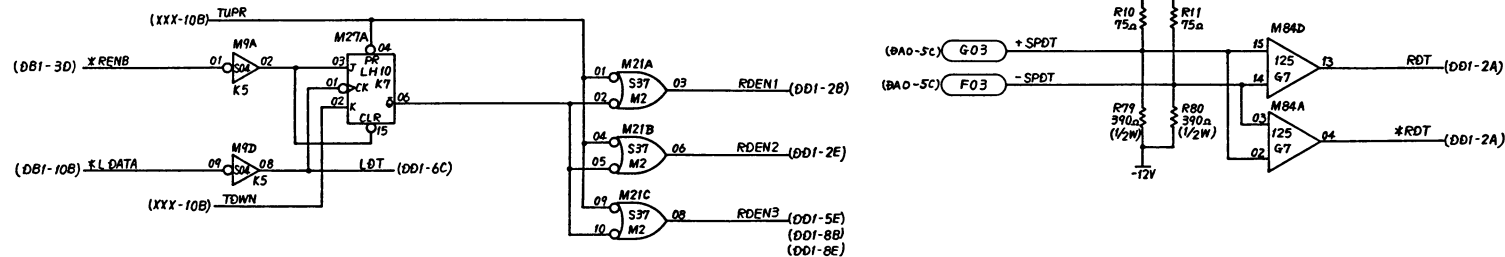


FDXA-2901-3

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5V 500
 TUPR (XXX-2B), (XXX-3E)
 (DC2-2F), (DC2-5B)
 (DC2-5G), (DC2-7D)
 (DC2-7E), (DC2-9F)
 TDWV (XXX-3F)



DC3

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WRITE COMPENSATION

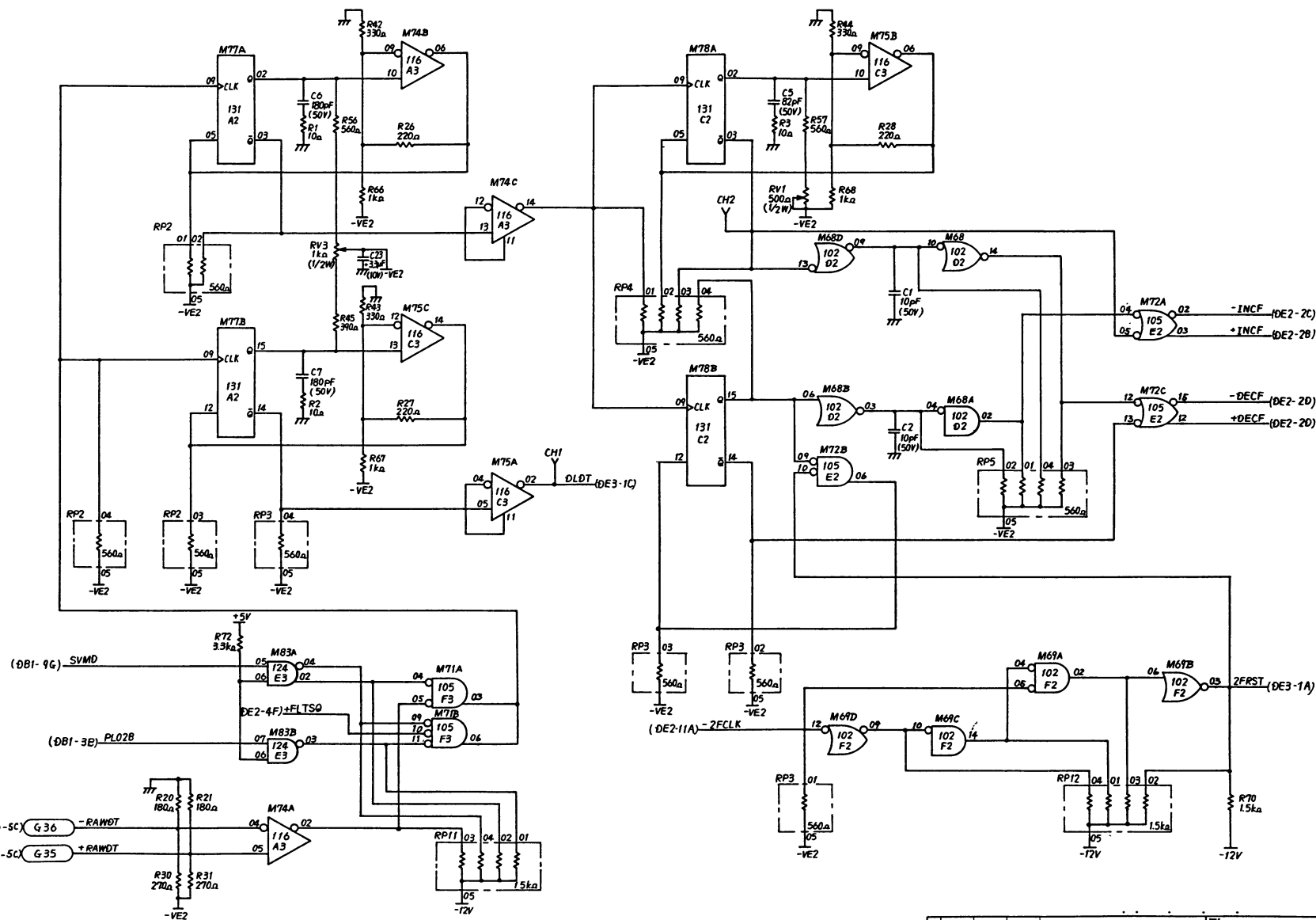
FUJITSU LIMITED 039

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FUJITSU LIMITED 041/

FDXA-2901-3



FUJITSU LIMITED		042 /
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(DE1-10F)-2F8T

(DE2-11A)-2FCLK

(DE2-11C)-2FCLKB

(DE1-50)QD0T

(DE2-46)+VF0FS

01 RP17
05 1.5ka
-12V

04 RP14
05 1.5ka
-12V

03 RP14
05 1.5ka
-12V

03 RP15
05 1.5ka
-12V

03 RP18
05 1.5ka
-12V

(DA0-SF) A05

(DA0-SF) G05

(DA0-SF) G30

A20, A30
B05, B15, B25
F05, F01, F24
F30
G15, G25

(DA0-SF) A25

(DA0-SF) F25

C31-C44

3.3μF
(10V)

M1

M2

M7-M24, M43,

M45-M54, M63,

M64, M68

M25-M42

M44, M55-M62

C20-C22

4.7μF
(25V)

C45

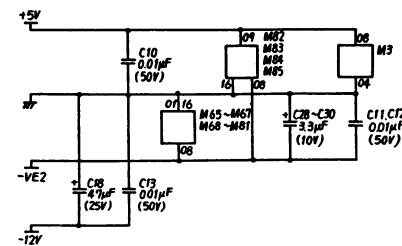
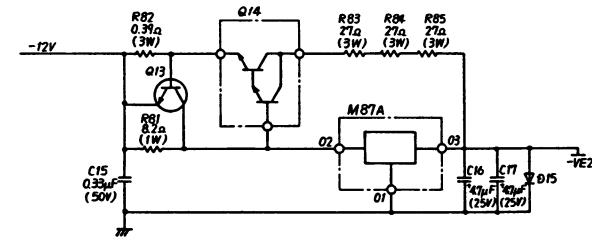
3.3μF
(10V)

-VE2

+5V

-12V

+VF02F G08 (DA0-7C)
-VF02F F08 (DA0-7C)
+SPDT G07 (DA0-7B)
-SPDT F07 (DA0-7B)



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FUJITSU LIMITED 043/

FDXA-2901-3

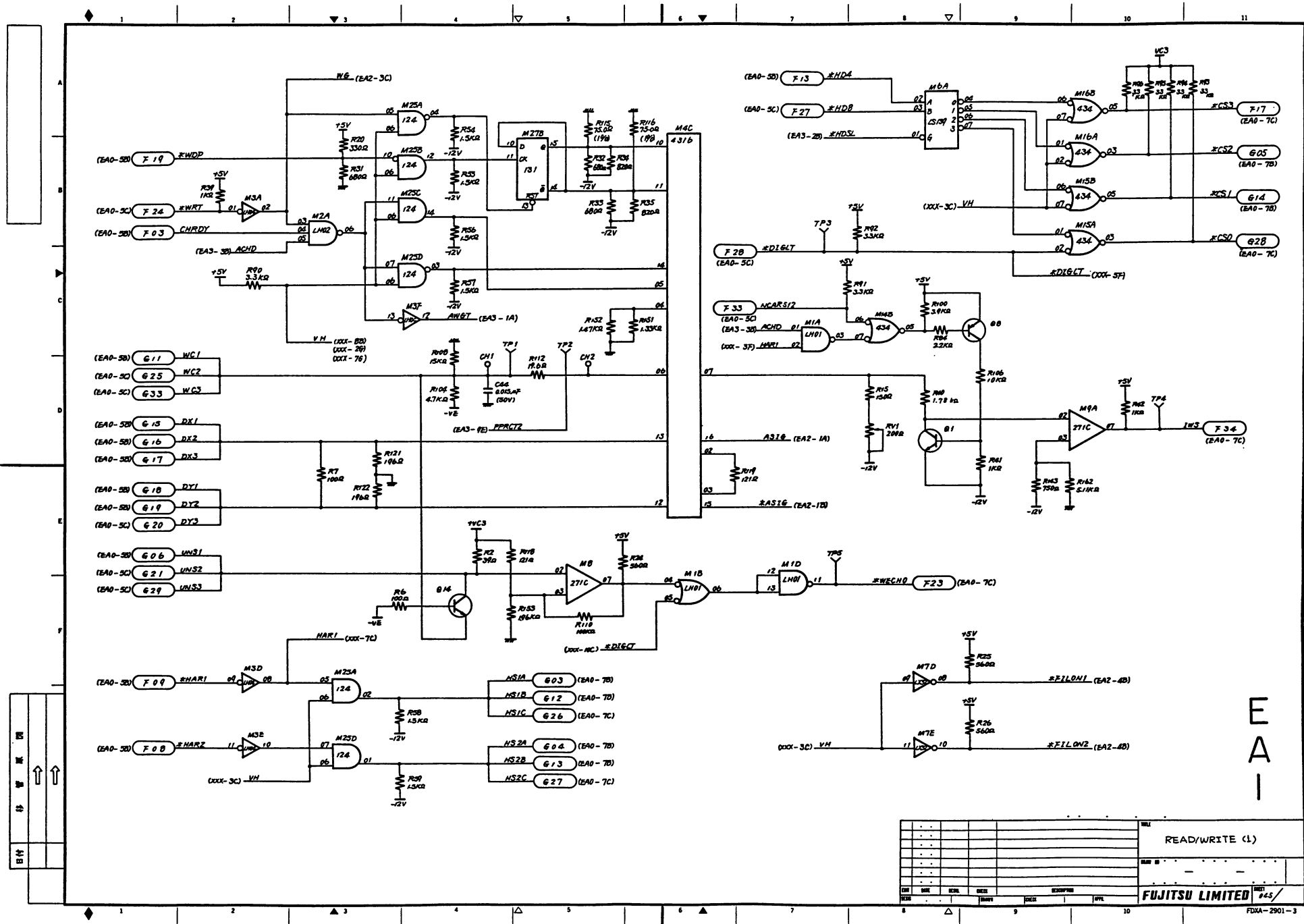
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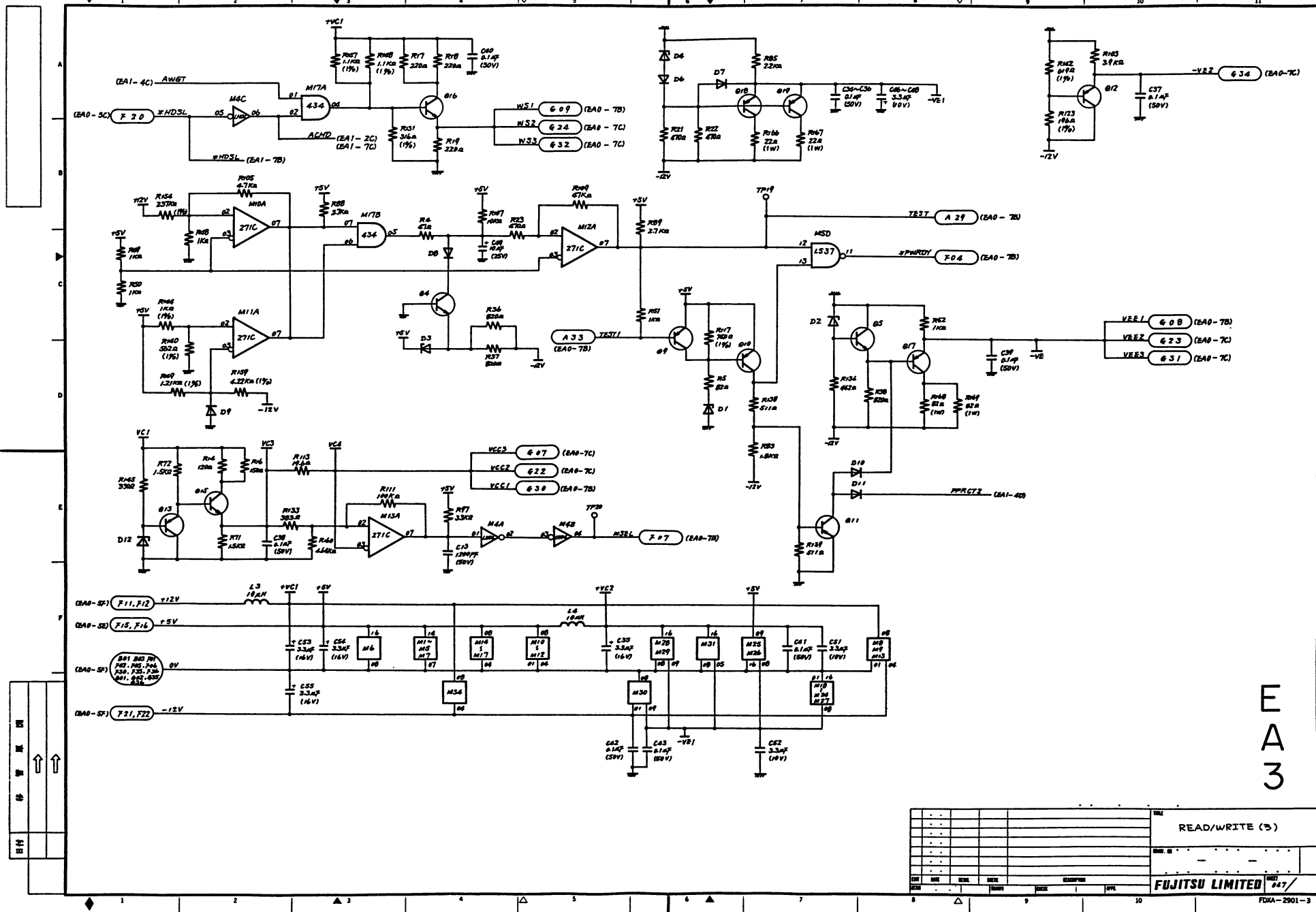
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(PA3) - (C3)	7837	A36	7837	A-C	
(PA1) - (D3)	7837	A36	7837	A-C	
(PA1) - (E3)	7837	A36	7837	A-C	
(PA1) - (F3)	7837	A36	7837	A-C	
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(PA1) - (J3)	7837	A36	7837	A-C	
(PA1) - (K3)	7837	A36	7837	A-C	
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(PA1) - (M3)	7837	A36	7837	A-C	
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(PA1) - (X3)	7837	A36	7837	A-C	
(PA1) - (Y3)	7837	A36	7837	A-C	
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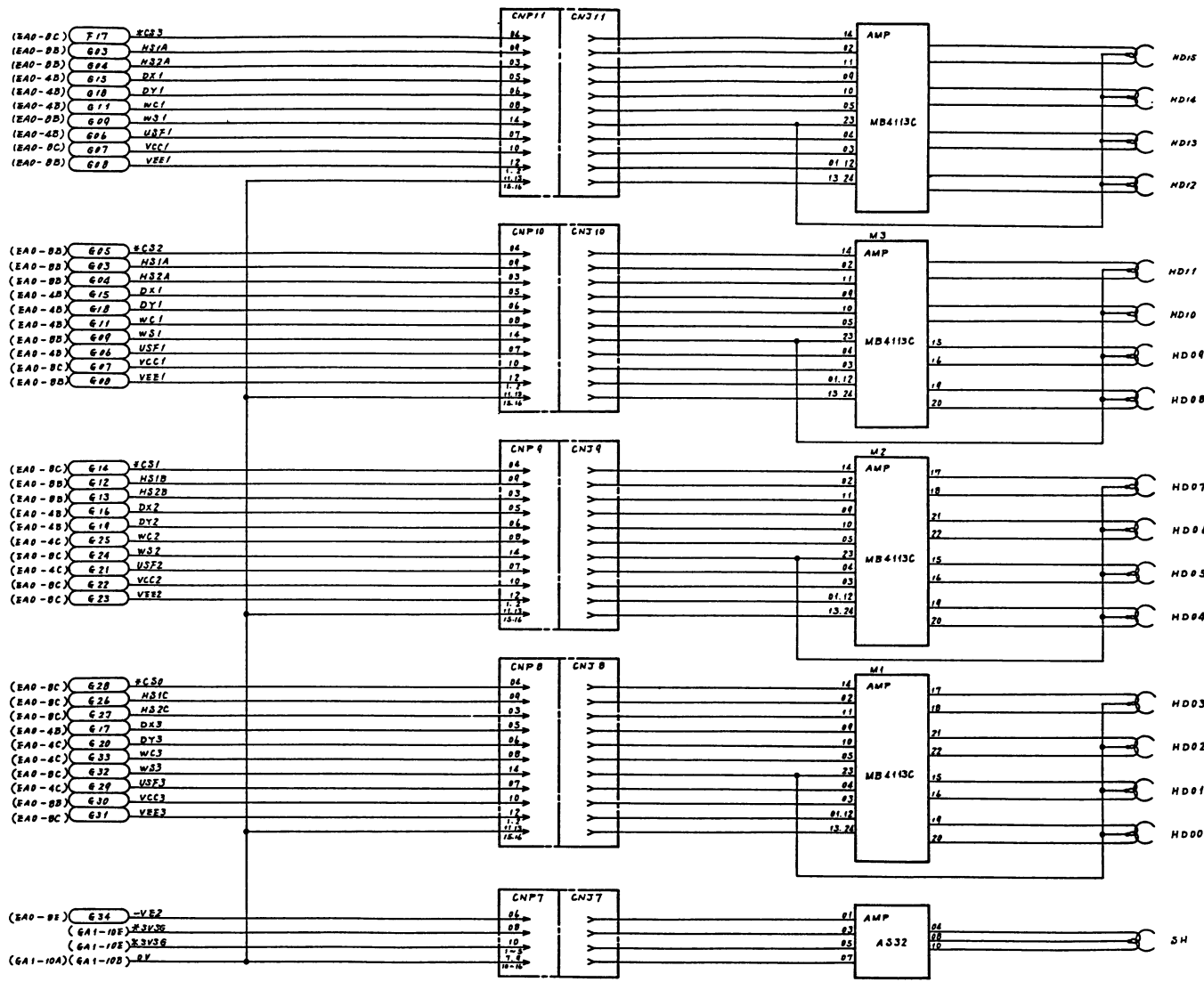
READ/WRITE (3)			
Fujitsu Limited			
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READ/WRITE (4)

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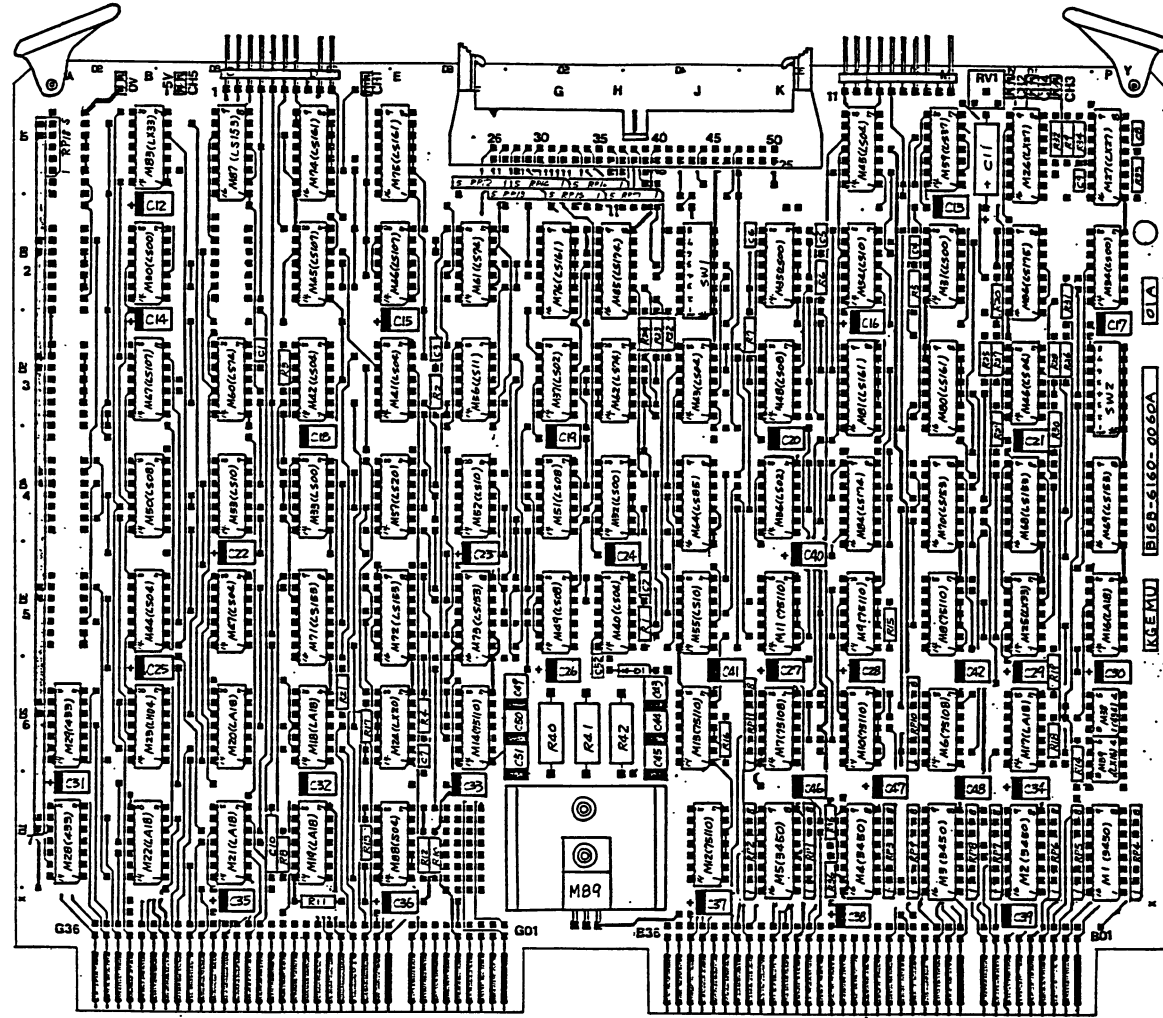


FAI

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DRAWN BY			
CHECKED BY			
DATE			
REVISION			
Fujitsu Limited			

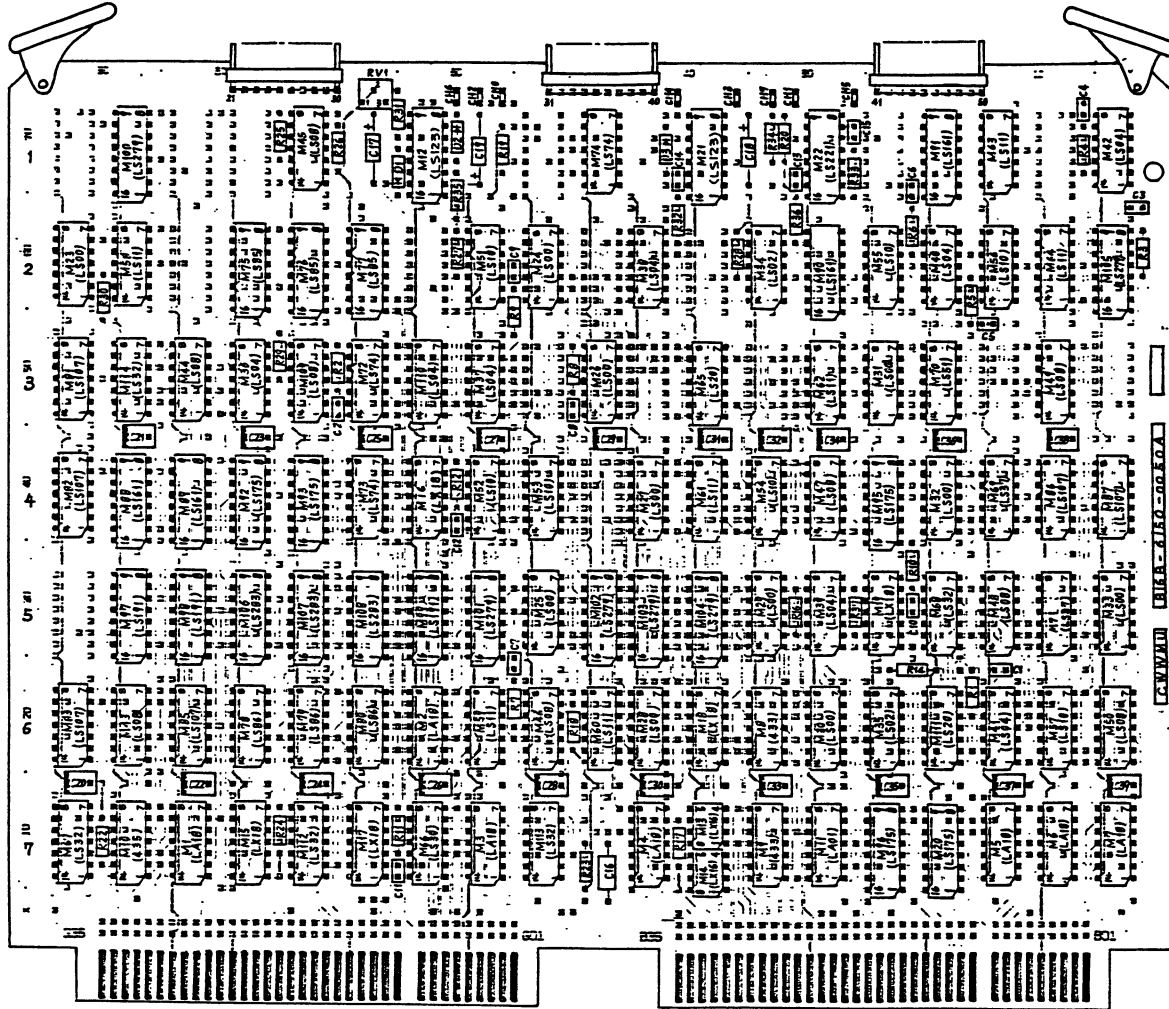


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KGE MU									
KGE MU PCB ASSEMBLY									
FUJITSU LIMITED 052/									

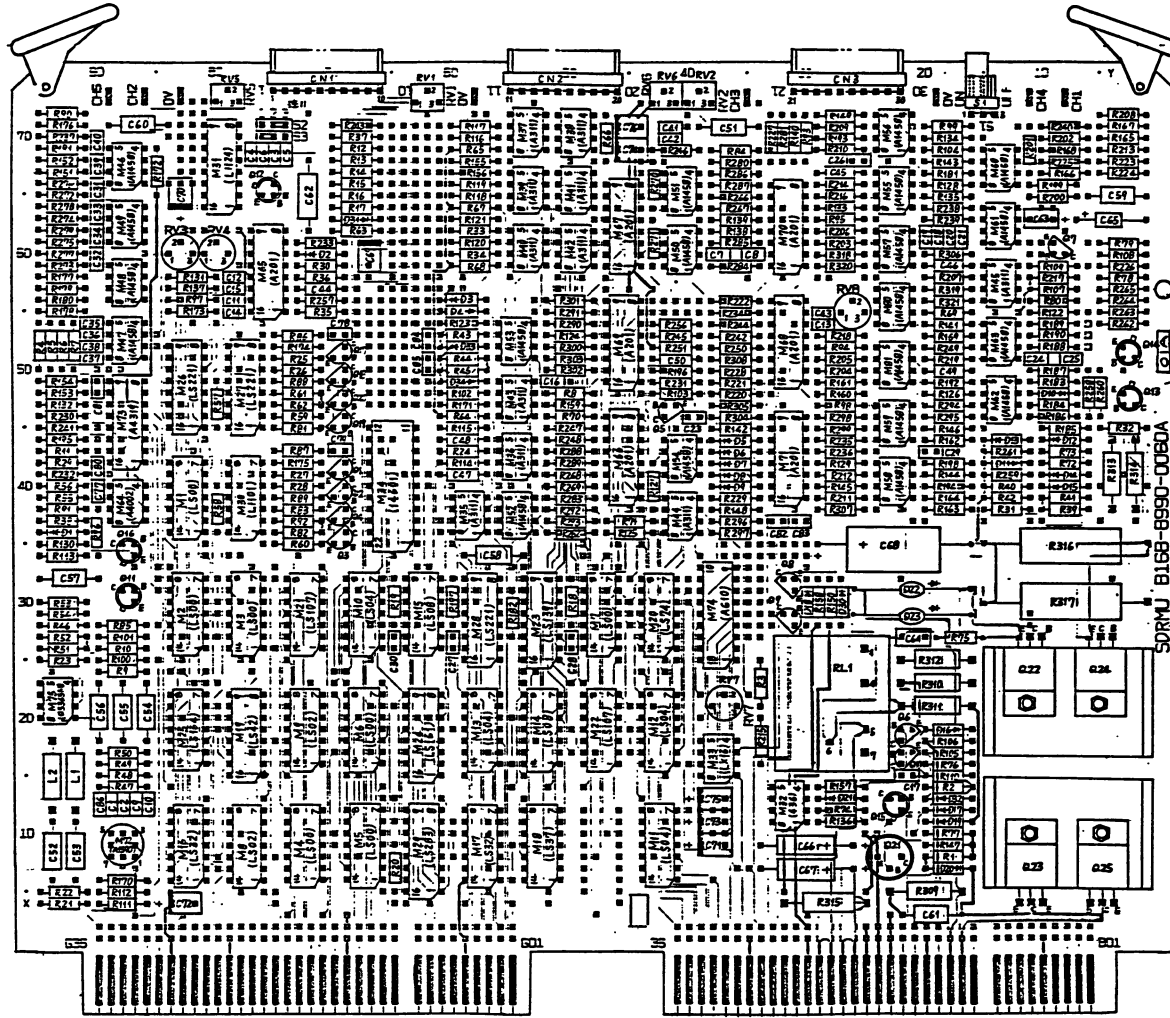
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FUJITSU LIMITED	

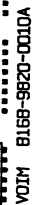
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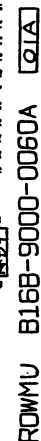
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REV. 11	REV. 12	REV. 13	REV. 14	REV. 15	REV. 16	REV. 17	REV. 18	REV. 19	REV. 20
REV. 21	REV. 22	REV. 23	REV. 24	REV. 25	REV. 26	REV. 27	REV. 28	REV. 29	REV. 30
REV. 31	REV. 32	REV. 33	REV. 34	REV. 35	REV. 36	REV. 37	REV. 38	REV. 39	REV. 40
REV. 41	REV. 42	REV. 43	REV. 44	REV. 45	REV. 46	REV. 47	REV. 48	REV. 49	REV. 50
REV. 51	REV. 52	REV. 53	REV. 54	REV. 55	REV. 56	REV. 57	REV. 58	REV. 59	REV. 60
REV. 61	REV. 62	REV. 63	REV. 64	REV. 65	REV. 66	REV. 67	REV. 68	REV. 69	REV. 70
REV. 71	REV. 72	REV. 73	REV. 74	REV. 75	REV. 76	REV. 77	REV. 78	REV. 79	REV. 80
REV. 81	REV. 82	REV. 83	REV. 84	REV. 85	REV. 86	REV. 87	REV. 88	REV. 89	REV. 90
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FUJITSU LIMITED 054

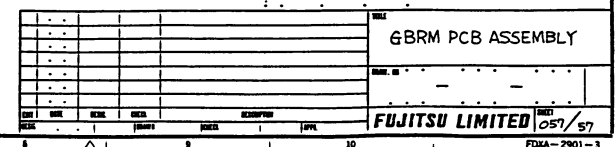


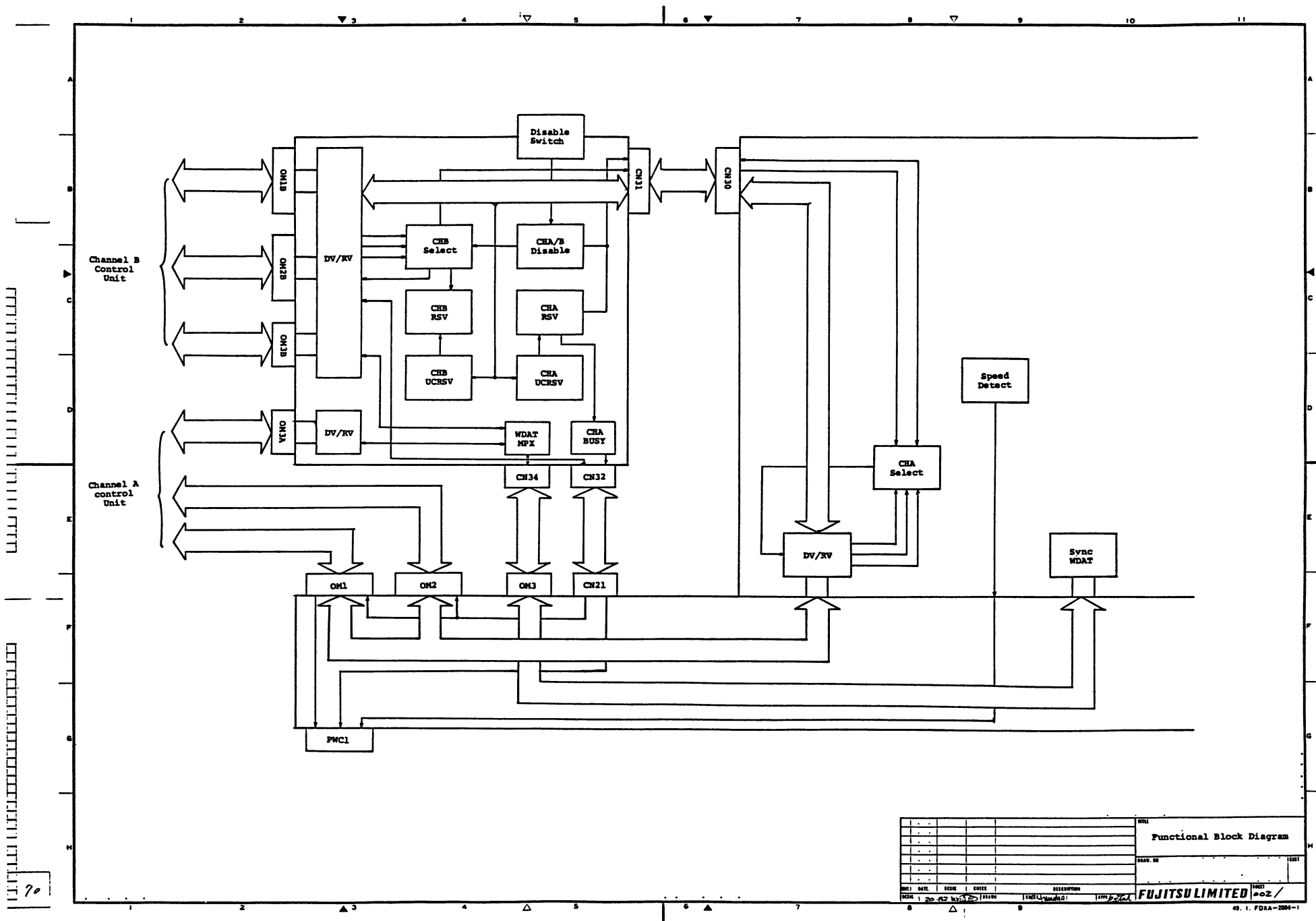
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FUJITSU LIMITED

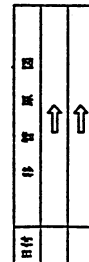


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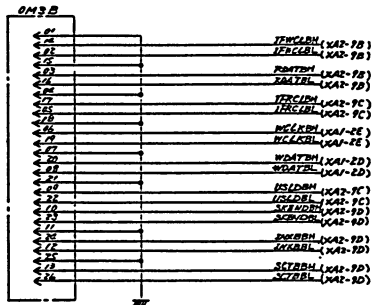
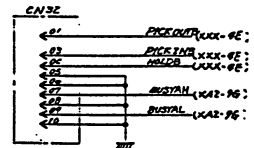
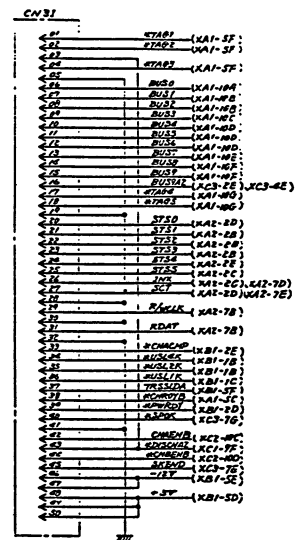
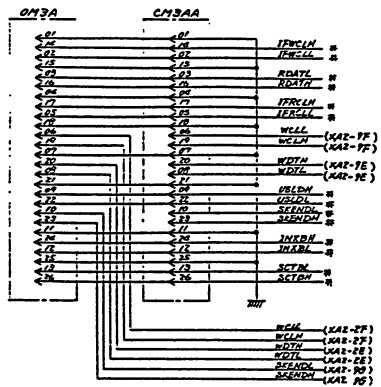
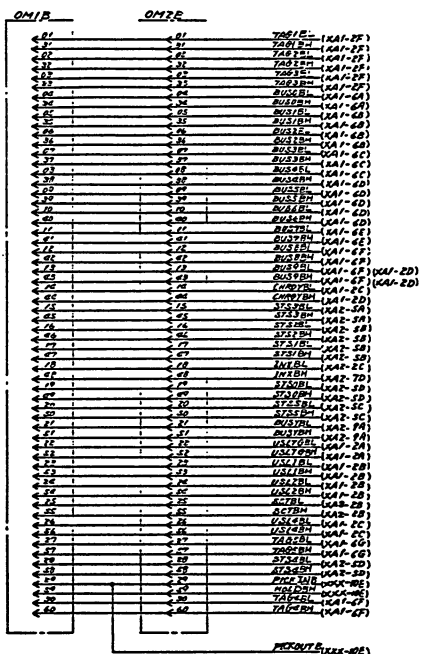




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2000.08	2000.08	2000.08	2000.08	Fujitsu Limited	

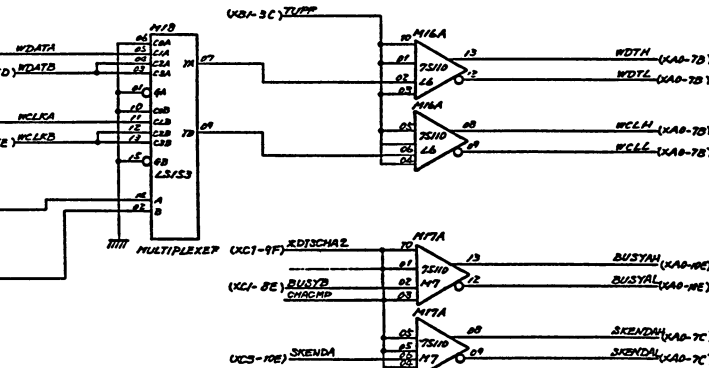
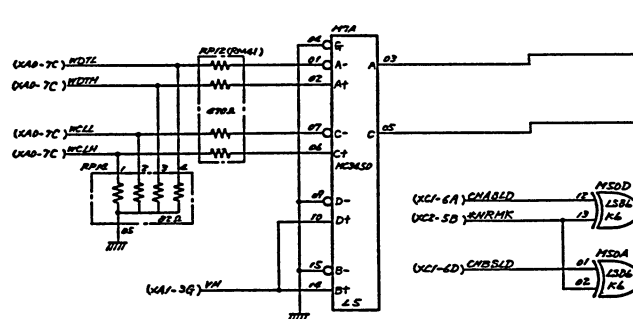


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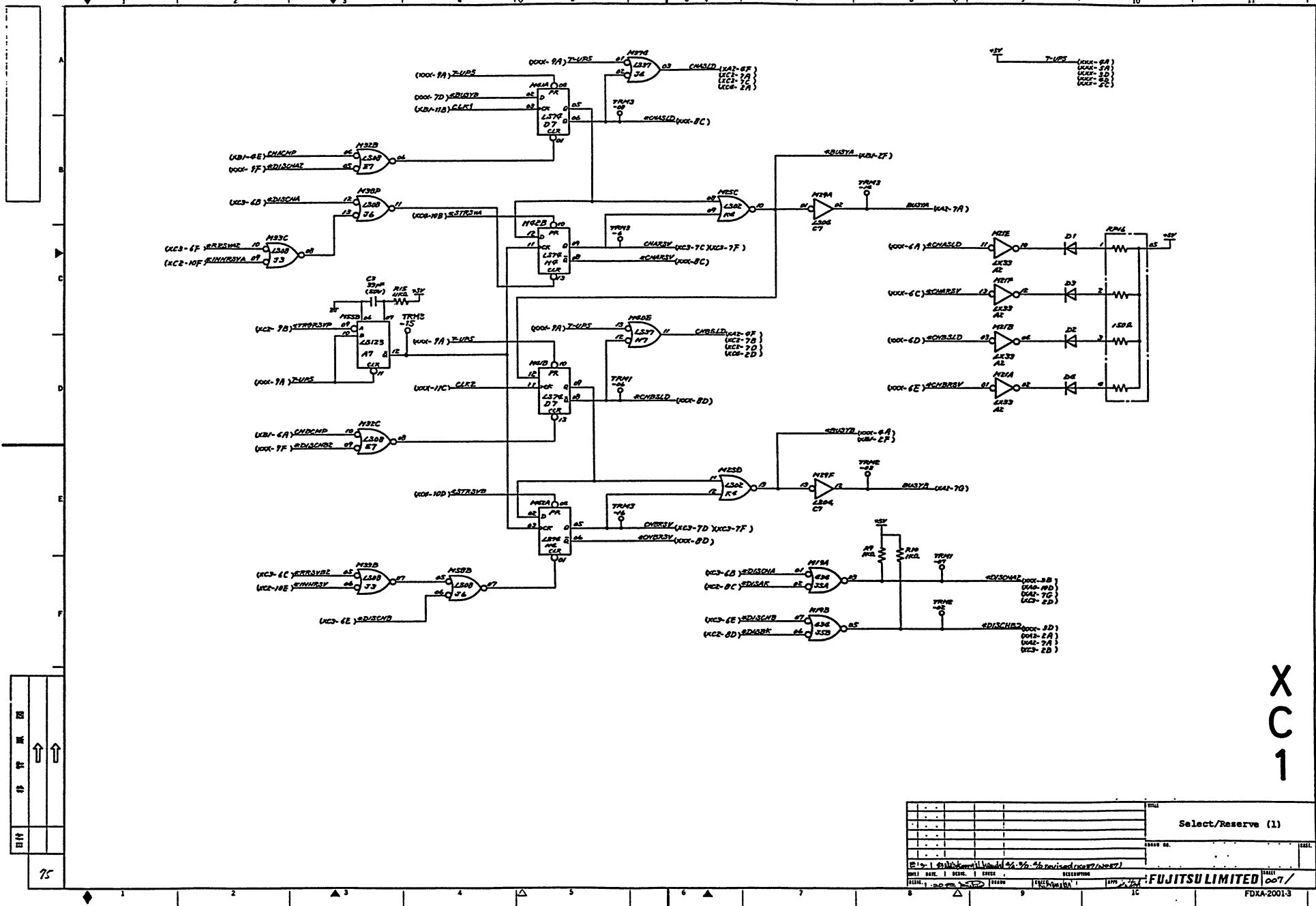
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FUJITSU LIMITED					
FDXA-2001-3					



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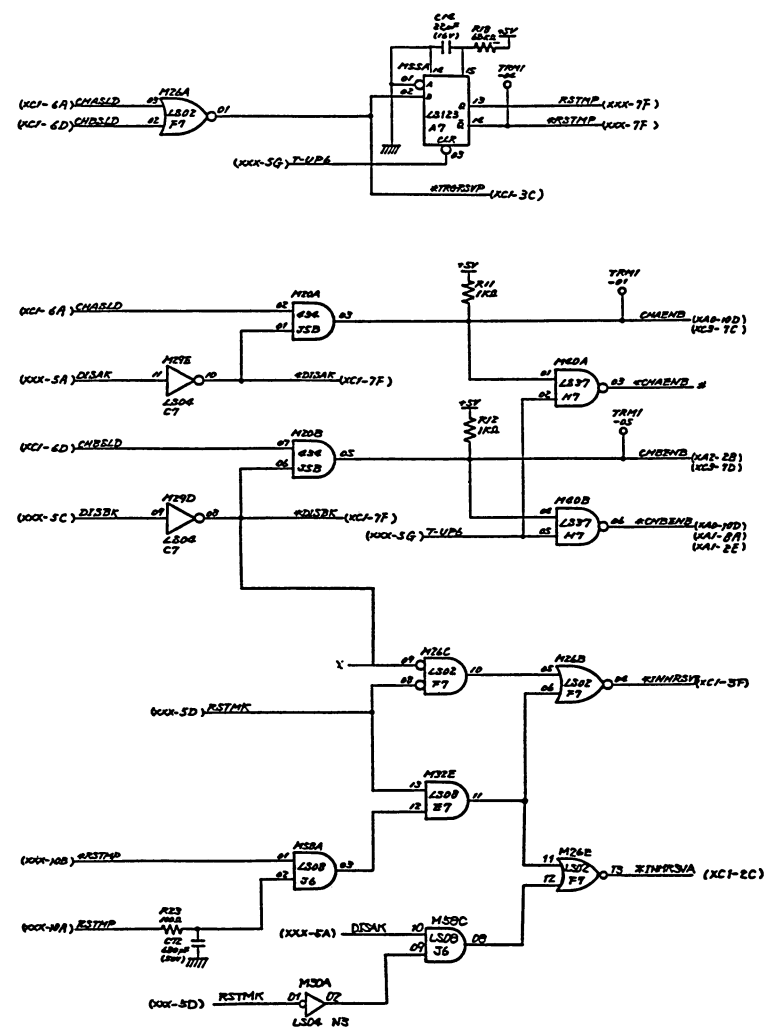
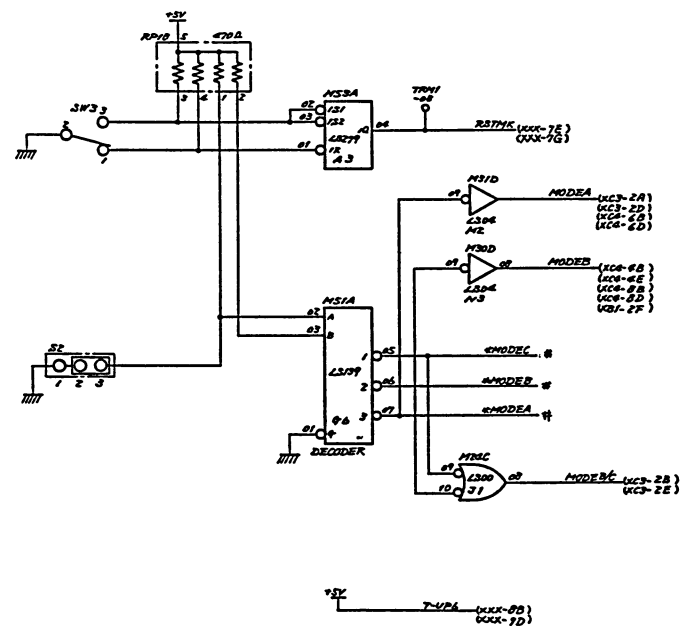
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74



XC1

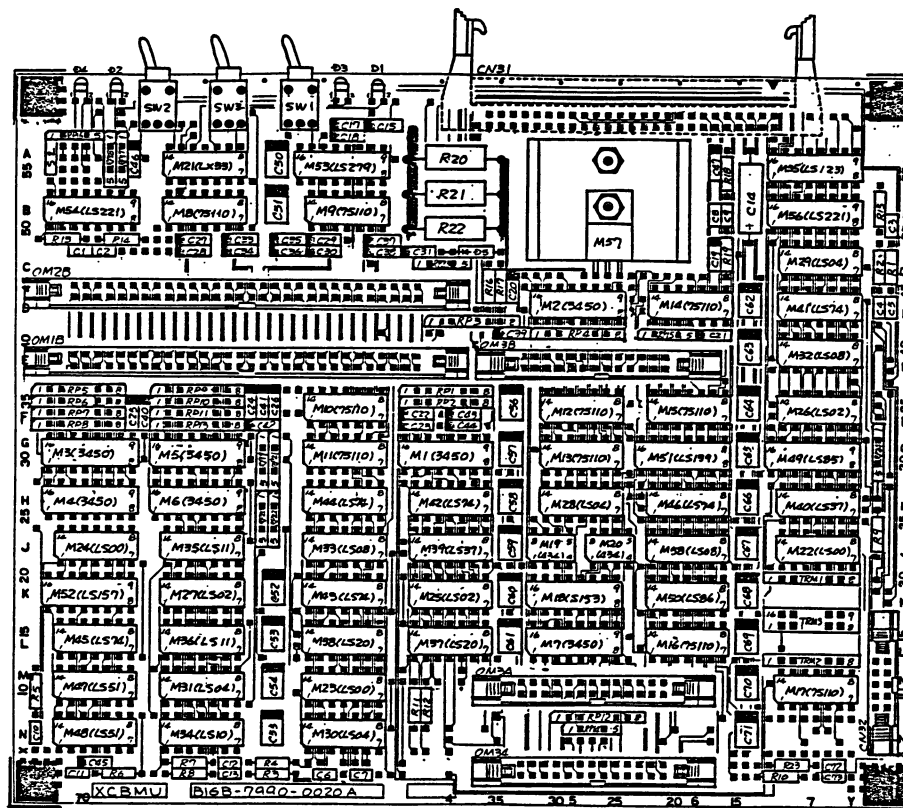
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REVISION			
FUGITSU LIMITED			
FDXA-2001-3			



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										READ. NO.	
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日本富士通株式会社 (46 revised pages/new) UNIT, DATE, NAME, ORDER, RESERVATION 富士通株式会社 東京 日本 1984/04/04										FUJITSU LIMITED 1441 008 / FDXA-2001-3	

78



Cross-call B (XCBM) PCB Assembly Drawing			
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CHECKED BY: []			
DATE: []			
FUGITSU LIMITED			

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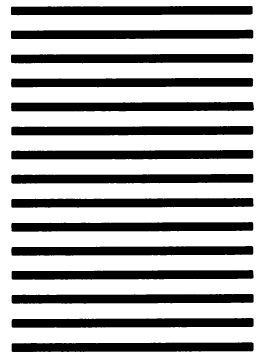
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